**Title:** Performance Enhancement Strategies for Design and Test Optimization of Analog and Mixed-Signal Circuits.

**Abstract:**

There has been an increasing demand for analog circuits, which can be attributed to the ever-increasing number of Internet of Things (IoT) devices and advancements in consumer electronics. This surge in demand is coupled with an industry-wide push for smaller chip designs that maintain or even enhance performance metrics. As the volume of analog circuits increases, cost-efficient and time-efficient testing schemes become crucial. Additionally, there is a pressing need for novel analog circuit architectures and design techniques that uphold desired performance metrics while minimizing chip area. These trends reflect the industry's drive to innovate and optimize, ensuring high performance in increasingly compact and integrated systems.

Multi-site testing, which involves the parallel testing of multiple chips by multiple test sites on an Automatic Test Equipment (ATE), has emerged as a key strategy to reduce test costs by decreasing test time and increasing throughput. However, as the number of test sites increases, maintaining uniformity between them becomes challenging, leading to site-induced errors and subsequent site-to-site variations—discrepancies in test results obtained from different sites on the same ATE. Significant variations can result in test escapes, yield loss, and inaccurate trimming of fabricated circuits. This dissertation explores various techniques to identify issue test sites— suffering from significant site-induced errors. Additionally, it presents an algorithm to decompose wafer-level measurements obtained from the ATE into distinct components, facilitating the identification of the different sources of spatial variation observed on the wafer.

The reduction in the area of analog circuits poses significant challenges for digital-to-analog converters (DACs), which are expected to maintain a linear relationship between their digital input codes and corresponding analog outputs. This linearity, along with other crucial properties, is often compromised by the area reduction due to degraded matching. Given that DACs are frequently used in safety-critical applications, periodic linearity tests and in-field calibration become essential. This thesis proposes a set of novel DAC architectures, which are altered versions of traditional designs to reduce the area overhead while maintaining performance. Additionally, it presents in-field DAC linearity algorithms and straightforward digital calibration techniques tailored for these compact DACs.

A critical performance affecting property in analog circuits is that of matching between pairs of analog components like transistors. In addition to matching to ensure the minimization of errors due to process gradients, stress and process gradients must also be considered. In this dissertation, an algorithm is presented to generate layout patterns to minimize any variant of gradient effects on a pair of analog components and ensure good matching.