Name & Std. No.:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**PRELAB:**

*Complete the prelab and make sure you have your designs and circuit diagrams ready before the lab session. You may refer to your text book, Chapter 6.*

**Q1.** Design a simple counting device (Section 2.0).

Number of States: \_\_\_\_\_\_\_\_\_\_

Number of State Variables: \_\_\_\_\_\_\_\_

**State Table: State-Assigned Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| A | A | B | 0 |
| B | B | C | 1 |
| C | C | D | 2 |
| D | D | E | 3 |
| E | E | F | 4 |
| F | F | A | 5 |

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| 000 | 000 | 001 | 000 |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

Canonical SOP Expressions for Next State Logic:

Simplified Next State Logic Expressions:

Circuit Diagram:

**Q2.** Design a simple counter (Section 3.0).

Number of States: \_\_\_\_\_\_\_\_\_\_

Number of State Variables: \_\_\_\_\_\_\_\_

**State Table: State-Assigned Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| A | A | B | 0 |
| B | B | C | 2 |
| C | C | D | 4 |
| D | D | A | 5 |

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

Canonical SOP Expressions for Next State Logic:

Simplified Logic Expressions:

Circuit Diagram:

**Q3.** Design an up/down counter (Section 4.0).

Number of States: \_\_\_\_\_\_\_\_\_\_

Number of State Variables: \_\_\_\_\_\_\_\_

State-Assigned Table:

Canonical SOP Expressions for Next State Logic and Output Logic:

Simplified Logic Expressions:

Circuit Diagram:

**LAB:**

**2.0 A Simple Counting Device**

How does the **clock\_generator** module produce a signal with a period of about 2.68 seconds?

Hardware results demonstrate a functional design: \_\_\_\_\_\_\_\_\_\_

**3.0 A Simple Counter**

Hardware results demonstrate a functional design: \_\_\_\_\_\_\_\_\_\_