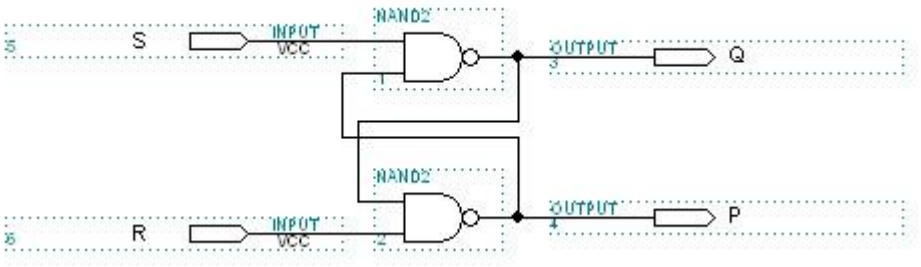
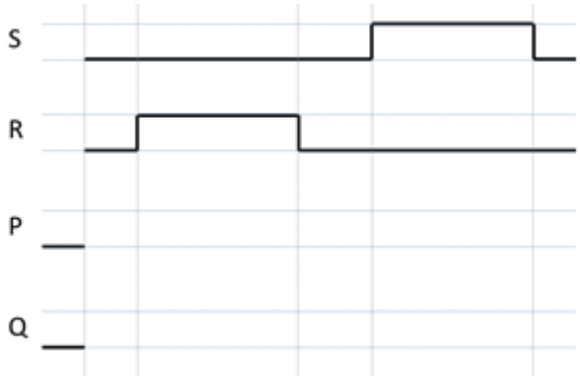
Cpr E 281 HW08

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Latches and Flip-Flops
Assigned Date: Ninth Week
Due Date: Oct. 27, 2014

P1. (20 points) In the circuit below, two NAND gates are used to construct a latch. (Notice that NOR gates are used in the lecture.) For the inputs S and R given below, draw a timing diagram (similar to Fig. 5.4(c) in textbook) for Q and P of the circuit above. You may assume the NAND gates have no delay.





P2. (10 points) Describe what the circuit in P1 above does (i.e., how Q and P are changed) when:

(a) R = 0, S = 0;
(b) R = 0, S = 1;
(c) R = 1, S = 0;
(d) R = 1, S = 1;

P3 (10 points) Show that the gated SR latches in Fig. 5.5(a) and Fig. 5.6 are functionally equivalent by transforming the design in Fig. 5.5(a) into the one in Fig. 5.6 using the rules of Boolean algebra. Please show your transformation process step by step using a sequence of circuit diagrams.

P4. (15 points) Draw the timing diagram for a negative-edge-triggered D flip-flop with Preset and Clear functionalities for the following input signal combinations. This flip-flop can be seen in Fig. 5.12. The signal values for Clock, D, Preset, and Clear vary as shown below. Assume each signal is held constant from one time step to the next. Assume gate delays to be zero. Assume the initial value of Q to be 0.

Draw the waveforms for Clock, D, Preset_n, and Clear_n where Preset_n is the NOT of Preset and Clear_n is the NOT of Clear. Finally, show the output Q.

Time	**CLOCK**	**D**	**Preset**	**Clear**
0	0	1	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	0	0
4	1	1	0	1
5	1	1	0	0
6	0	1	0	0
7	0	0	0	1
8	0	0	0	0
9	1	0	0	0
10	0	0	0	0
11	0	1	0	0
12	0	1	1	0
13	0	0	0	0
14	1	0	0	0
15	0	0	0	0

P5. (10 points) Repeat P4 when input D is inverted for all times steps.

P6. (10 points) Repeat P4 for a positive-edge triggered D flip-flop with Preset and Clear. This flip-flop can be seen in Fig. 5.13.

P7. (15 points) Problem 5.1 in the textbook.

P8. (10 points) Given a 100-MHz clock signal, derive a circuit using D flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.