Cpr E 281 HW 10

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Thirteenth Week
Due Date: Nov. 17, 2014

P1. (10 points) Design a modulo-6 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1,… The counter counts the clock pulses if its enable input w is equal to 1, otherwise it does not increment its count. Use D flip-flops in your circuit and include the state diagram, state-assigned table, next-state expressions and output expressions all clearly labeled. Let y_2, y_1, and y_0 be the current state values.

P2. (10 points) Repeat Problem 1 using JK flip-flops. Work through the entire design process rather than simply converting the D flip-flops to JK flip-flops. Use the same state diagram.

P3. (10 points) Repeat Problem 1 using T flip-flops. Work through the entire design process rather than simply converting the D flip-flops to T flip-flops. Use the same state diagram.

P4. (10 points) Consider the state machine specified by the following state transition table.

Current		Input	Next	
X	Y	I	X	Y
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

(a) Draw the state transition diagram of the machine.
(b) Write two next-state expressions for X and Y that will implement the transitions of the state machine. Make your expressions as simple as possible, and use XOR gates and NOT gates only.
(c) Implement the state machine using D flip-flops, XOR gates, and NOT gates.
(d) Suppose the machine is initially in 00 (i.e., X=0 and Y=0). Indicate for each input sequence below, the state the machine is in after the last digit has been read in. Assume the digits are read in from left to right.
    a. 11111
    b. 1001110000101100
    c. 436 1s followed by 325 0s

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P5. (10 points) Deduce the purpose of a state machine with the next state logic and output logic given below. Let X, Y, and Z be the values of the three D flip-flops, X_{next}, Y_{next}, and Z_{next} be the next state expressions, and ABC be the three-bit output of the circuit.
(a) Construct the state assigned table from the expression.
(b) Draw the state diagram from the table.
(c) Explain in one sentence the functionality of the circuit.

$X_{next} = X'YZ + XY' + XZ'$
$Y_{next} = Y'Z + YZ'$
$Z_{next} = Z'$
$A = X'$
$B = Y$
$C = Y + Z$

P6. (10 points) A state machine has one input P in addition to the clock input and one output Q. The value of Q is 1 if the total number of 1's in the sequence of input P is either a multiple of 2 or a multiple of 3. Otherwise, the output value Q is 0. Draw a state transition diagram for the state machine using as few states as possible.

P7. (10 points) A state machine has one input P in addition to the clock input and one output Q. The value of Q is 1 if the total number of 1's and the total number of 0's in the sequence of input P are both even. Otherwise, the output value Q is 0. Draw a state transition diagram for the state machine using as few states as possible.

P8. (10 points) Draw a state transition diagram for:
(a) A state machine that reads in a sequence of binary digits, one at a time, and stops when it has read in a total of five 1s (need not be consecutive). To "stop" the machine, merely have it loop repeatedly in a final state.
(b) A state machine that stops when it has read in at least three consecutive 1s followed by a 0.

P9. (20 points) Design a three-bit counter-like circuit controlled by the input w. If w=0, then the counter subtracts 1 from its contents (acting like a normal down-counter). If w=1, then the counter adds 2 to its contents, wrapping around if the count has to become 8 or 9. Thus if the current state is 6 (or 7) and w=1, then the next state is 0 (or 1). Use D flip-flops in your circuit. Let y_2, y_1, and y_0 be the current state values.
(a) Draw a state diagram for the machine.
(b) Construct a state assignment table including the next state and output.
(c) Write the simplified expressions for the next state and output logic.