## **ModelSim SE 6.1b Tutorial**

- 1. Start ModelSim
- 2. Create a new project
  - Click on File, then New, then choose Project on the drop down menu
  - Enter your project name, in this case the project is called "and2gate"
  - Choose your project location, this project is stored at "C:\Temp\Projects\and2gate"
  - The default library name should be *work*.
  - Click OK button

Project Name		
and2gate		
Project Location		
C:/Temp/Projects/an	d2gate	Browse.
Default Library Nar	me	

- 3. You will be asked if want to create the project directory.
  - Click *OK* button

Creat	te Project	×
?	The project directory does not exist. OK to create the directory	y?
	OK Cancel	

4. Next you will be presented with the Add Items to Project Dialog. While you can use this dialog to create new source files of add existing ones, we will not be using this option for the tutorial. We'll add source files later so just click on the *Close* button



5. You now have a project by the name of "and2gate".



- 6. Now we want to add a new file to our project.
  - Click on File, choose Add to Project, and choose New File...
  - Choose *Verilog* as the file type
  - In the *File name:* box enter the desired file name, in this case the file is named "and2gate.v"
  - Click on the *OK* button

File Name	
and2gate.v	Browse.
Add file as type	Folder

7. The "and2gate.v" file has been added to your project.



8. Double-click on the and2gate.v to show the file contents. You are now ready to specify the and2gate module's functionality.

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- 9. We compete the and2gate specification as shown below..
  - The line "`timescale 1ns/ 1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units within the simulator. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator. *Note:* Be sure to use the correct ` character. The ` is the not the single quotation mark (') and is typically located on the same key as the ~. If you have errors in your file, this may be the culprit.
  - The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
  - Be sure to save the changes to the and2gate.v file by clicking on *File* and choosing *Save*.



10. We also want to add a testbench and again follow Steps 6 - 9 to add "and2gate\_tb.v". Then we add the functionality of the testbench module as shown below.

ModelSim SE 6.1b		
File Edit View Format Compile Simulate Add	Tools Window Help	timescale 1ns / 1ps
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and2gate.v ? Verilog U U8/21	1 `timescale 1ns / 1ps	
UL anuzgate_t0.v veniog i 00/21	2	wire F_t;
	<pre>3 module and2gate_tb();</pre>	
	4 reg A_t, B_t;	and2gate and2gate 1(A t B t F t)
	5 wire F_t;	
	$\frac{6}{7}$	
	8 andzgate andzgate_I(A_t, b_t, r_t),	initial
	9 initial	hegin
	10 begin	bogin
	11	
	12 // case 0	// case 0
	13 A_t<=0; B_t<=0;	A $t \le 0$ B $t \le 0$
	$ = 14 \qquad = 15 \qquad$	$\frac{1}{141} \frac{1}{160} \frac{1}{100} \frac{1}$
	16 // case 1	$\#1$ \$display( $F_l = \%0$ , $F_l$ );
	17 A t<=0; B t<=1;	
	<pre>18 #1 \$display("F t = %b", F t);</pre>	// case 1
	19	
	20 // case 2	$A_l <= 0; B_l <= 1;$
	21 A_t<=1; B_t<=0;	#1 \$display("F_t = %b", F_t);
	22 #1 \$display("F_t = %b", F_t);	
	23	
	25 A $t \le 1$ : B $t \le 1$ :	// case 2
	26 #1 \$display("F t = %b", F t);	$A_t <= 1; B_t <= 0;$
	27	#1 \$display("E t = %b" E t):
	28 end	
•	29 endmodule	
1 (##) Project III Literary		// case 3
	n anuzgate.v n anuzgate_0.v	A t<=1: B t<=1:
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- 11. After saving both "and2gate.v" and "and2gate\_tb.v", we want to check the syntax of both files.
  - Click on the *Compile* Menu and select *Compile* All
  - If the syntax was correct, a checkmark will appear next to each file
  - If the syntax was incorrect, the window at the bottom will list the individual errors.

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- 12. Now it's time to simulate the design.
  - Click on the *Simulate* menu and choose *Start Simulation*
  - Expand the selection for the work library by click on the + symbol on the left.
  - Select and2gate\_tb and click OK button

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🖃 📶 work	Library	C:/Temp/Projects/and2gate/work
and2gate	Module	C:/Temp/Projects/and2gate/and2gate
and2gate_tb	Module	C:/Temp/Projects/and2gate/and2gate
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		•
Design Unit(s)		Resolution
work.and2gate_tb		default

- 13. Next we create a simulation waveform window.
  - Click on File menu, choose New, then choose Windows, then choose Wave
  - Add the signals that would like to monitor by dragging the signal from the middle pane to the waveform window as shown below



- 14. We can simulate the design.
  - Enter 5 ns as the length of time we would like to simulate for in the Run Length box and click the Run icon as shown below.



15. Our simulation is complete. The simulation waveforms appear and we can check the and2gate module's functionality. Further, the \$display statements included in the testbench appear in the lower window.

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Project : and2gate Nov: 5 ns Delta: 0	sim:/and2gate_tb - Limited Visibility Region 0 ps to 5547 ps

**\$display statements appear here**