Cpr E 281 HW03

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

NAND/NOR Gates and Synthesis
Assigned Date: Third Week
Due Date: Feb. 3, 2014

P1. (10 points) Problem 2.11 in the textbook.

P2. (10 points) Problem 2.21 in the textbook. Show all steps.

P3. (10 points) Draw a circuit diagram for the function in P2 using NAND gates only.

P4. (10 points) A full adder is a circuit which adds three bits X, Y, Z together and returns two bits C and S to represent the total as a 2-bit binary number C S. C is the MSB and S is the LSB. For example, if X=1, Y=1, Z=0, the total should be 2, or 10_2 in binary. Hence C=1 and S=0. Write the truth tables for the functions C and S.

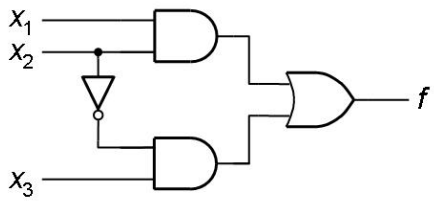
P5. (10 points). Write the functions C and S from P4 in short hand notation using (a) min terms and (b) max terms. Also write functions C and S in canonical sum-of-products (SOP) and canonical product-of-sums (POS) forms.

P6. (10 points) Obtain the simplest SOP expressions for the functions C and S in problem P5 and draw their respective circuit diagrams.

P7. (10 points) Let L(A,B,C,D) be a four-way light control with four switches A,B,C, and D.
(a) Write the truth table for the function L.
(b) Write the canonical sum-of-products expression for the function L.
(c) Write the canonical product-of-sums expression for the function L.

P8. (10 points) Show how to implement a NOT function using: (a) 2-input NAND, (b) two input NOR, and (c) a two input multiplexer. For part (a) and part (b), you should use a different way from what has been shown in class (connecting both terminals to the input signal). Note that you are allowed to connect constant voltages (i.e., logic values 0 or 1) to the gates.

P9. (10 points) By applying DeMorgan's Theorem directly to the following circuit, convert it into one that uses only:
(a) NAND gates and NOT gates.
(b) NOR gates and NOT gates.



P10. (10 points) Please write down the number of transistors required to implement the following circuits in CMOS technology.

(a) The function C in P6. (Assuming functions C and S are implemented independently.)
(b) The function S in P6. (Assuming functions C and S are implemented independently.)
(c) The original circuit in P9.
(d) The circuit in P9(a).
(e) The circuit in P9(b).