Cpr E 281 HW 12

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Fifteenth Week
Due Date: Dec. 7, 2015

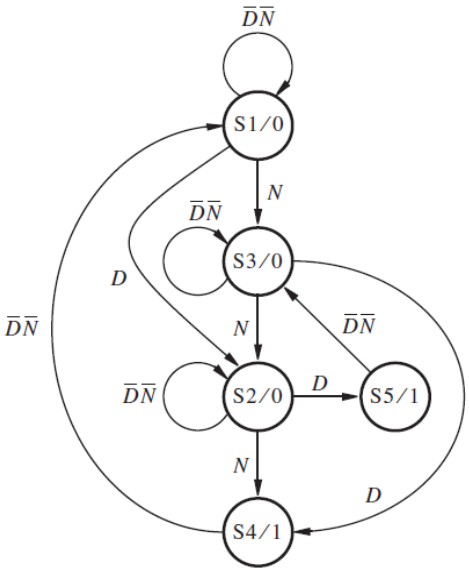
P1. (20 points) You are required to design a device to test one's reaction. The device has two inputs, G and R. G is controlled by the operator of the device, and R is controlled by the person under test. The device also has a single output, Z, which is equal to 0 when the device is not being used. The operator will push and then release G, which will turn a green light ON and then OFF. Once the person under test observes the green light coming ON, he/she is supposed to push and release R before the green light is turned OFF. In this case, the output Z becomes 1 until G is released. If the person under test fails to push *and* release R before the green light turns OFF, Z will not change.

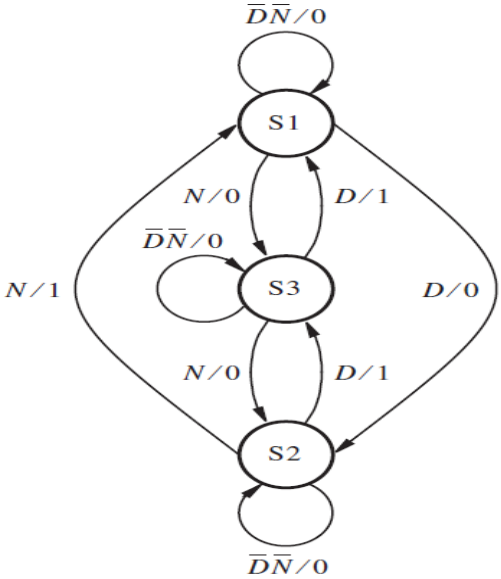
(a) Draw the state transition diagram of a Moore-type machine which describes the behavior of the device.

(b) For the following input sequence, find out the state and the output of the machine in part (a) after each clock edge:

- At 1st clock edge, GR = 00
- At 2nd clock edge, GR = 10
- At 3rd clock edge, GR = 11
- At 4th clock edge, GR = 01
- At 5th clock edge, GR = 00
- At 6th clock edge, GR = 10
- At 7th clock edge, GR = 10
- At 8th clock edge, GR = 11
- At 9th clock edge, GR = 10
- At 10th clock edge, GR = 11
- At 11th clock edge, GR = 10
- At 12th clock edge, GR = 00

P2. (20 points) Represent each FSM shown below in form of an ASM chart.





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P3. (15 points) Section 6.5in the textbook presents a design for the serial adder. Drive a similar circuit that functions as a serial subtractor which produces the difference of operands A and B. (Hint: Use the rule for finding 2's complement in Section 3.3.1 to generate the 2's complement of B).

P4. (15 points) Derive a minimal state table for an FSM that acts as a three-bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit p = 1 if and only if the number of 1s in the three-bit sequence is odd.

P5. (10 points) We found earlier that trying all possible state assignments in order to find the best implementation is impractical. Determine the number of possible state assignments for an FSM that has n states for which $k = log_2 n$ state variables are used. Assume for simplicity that n is a power of 2.

P6. (20 points) We would like to design a synchronous sequential circuit with two inputs A_1 and A_0, and one output Z. The two inputs are interpreted as a two-bit unsigned integer A_1A_0. Assume the input combination $A_1A_0 = 11$ will never happen. In other words, the inputs represent an integer from 0 to 2. The circuit will produce an output of 1 if the sum of the last two inputs in the input sequence is 2. Draw the state diagram of a Moore-type FSM for the circuit. Draw your diagram as clearly as possible.