PRELAB!
Read the entire lab, and **complete** the prelab questions (Q1-Q2) on the answer sheet **before** coming to the laboratory.

1.0 Objectives
In the previous lab you learned how to program digital circuits on an FPGA using Quartus II. You also learned how each circuit is related to a truth table and a logic expression. In this lab you will design two circuits and in the process, tackle one way of performing design entry: schematic capture. Other methods such as truth table and Verilog will be covered in future labs.

2.0 Setup
Create a folder **/home/*username*/CPRE281/Lab02**, and two sub-folders in this folder named **/Lab02/lab2step1** and **/Lab02/lab2step2**. You will be saving your work and running your circuits in this lab from these two directories.

3.0 Circuit 1
You will derive the truth table, logic expression, and circuit diagram for the circuit described below.
NOTE: when a logic variable has a value of 1, we say that it is "asserted".

Description:

You are to construct a logic circuit with $inputs = \{A, B, C\}$ and $output = \{F\}$.
The logic is such that F is asserted only when A or B are asserted and C is not. First complete the truth table in the answer sheet, and then use it to construct a canonical sum-of-products (SOP) expression of the output F.

You are now ready to build the circuit. Quartus II has logic gates and other basic logic functions available under the name of **primitives**. In this step in the lab, you will learn how to use logic gates to make your design in schematic capture mode.

You will need to create a new *.qpf* file and name it lab2step1. To do this select **File -> New Project Wizard…**

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Click the **Next >** button then make the following settings:

Working directory:	**/home/*username*/CPRE281/Lab02/lab2step1**
Name of project:	**lab2step1**
Name of top level design:	**lab2step1**

Then click the **Next >** button two times. On page [3 of 5], under the *Device family* choose **Cyclone II**. Under *Available devices* select the part number of the Cyclone II FPGA that is on the DE2 board – **EP2C35F672C6**. Then click the **Next >** button two more times and if your *Summary* looks correct click **Finish**.

Now, create a new .bdf file and add it to the project. To do this select **File -> New**. Under **Design Files** choose **Block Diagram/Schematic File**. Then select **File -> Save As…** Set the file name to **lab2step1.bdf** and ensure that the box for **add file to current project** is **checked** before saving.

You should have a valid logic expression using AND, OR, and NOT gates. You will now start building the circuit, one logic gate at a time.

- Double click in an open space on the schematic to bring up the **Symbol** window.
- In the *Libraries* menu expand c:/altera/10.0/quartus/libraries/ -> primitives -> logic. A list of gates will appear in the menu that you will need to create your project.
- Select the logic gate you want and hit the **OK** button. The gates are named by gate type and number of inputs to the gate, so a three-input AND gate is named **and3** and so forth. Remember that your overall circuit has three inputs and one output.
- Don't forget to label the input and output pins with their respective variable names just like you did in Lab01.
- Circuit elements can be moved around in the design by clicking and dragging them. When you have placed all gates where you want them, you can wire them together with the **Orthogonal Node Tool**.

Thus far you have used the cursor as an arrow. This has allowed you to move around the design, and move circuit elements. Clicking on the Orthogonal Node Tool, the symbol of the upper tool bar will change the cursor's function. The Orthogonal Node Tool is used to connect logic gates and other circuit elements together. You can also use this tool function by touching the cursor to the output or input of circuit element and dragging it to another element.

When you are done connecting your circuit, perform compilation. This prepares your design to be programmed into the FPGA to verify your digital circuit using hardware. You will need to assign your inputs and outputs to the proper pins on the FPGA as you did in the previous lab. To make it easier for the TA to verify everyone's design use the following input and output devices:

LOGICAL PIN NAME	HARDWARE DEVICE	FPGA PIN
A	SW[2]	PIN_P25
B	SW[1]	PIN_N26
C	SW[0]	PIN_N25
F	LEDG[7]	PIN_Y18

When you are done with your design, have the lab instructor verify it, and mark his/her initials in your answer sheet. Close all *lab2step1* files in Quartus II.

4.0 Circuit 2
The problem used in this step will be revisited in future labs also to illustrate how designs can be created in different ways. Create a new *.qpf* file and name it lab2step2. Save this file under **/CPRE281/Lab02/lab2step2.** Also create a new *.bdf* file named **lab2step2.bdf** and add it to the project.

Description:
A farmer owns two barns; one north of a creek and the other south of the creek. The farmer has a Cabbage, a Goat, and a Wolf. The Farmer needs to put each item in a barn every night. If the Cabbage and Goat are in the same barn, the Goat will eat the Cabbage. If the Wolf and the Goat are in the same barn, the Wolf will eat the Goat. The Farmer is worried and you have to design an alarm circuit that will let him know if two items can safely be placed in a barn.

For this circuit, you have three $inputs = \{Cabbage, Goat, Wolft\}$ and one $output = \{Alarm\}$.

If an input is in the north barn, it gets assigned a logic 1, and if it is in the south barn it gets assigned a logic 0. The output Alarm, asserts if there are two items in a barn that should not be kept together. Start by completing the truth table given in the answer sheet and use the truth table to construct a canonical sum-of-products (SOP) expression.

Follow the same steps described in the previous section. Again, use the following input and output devices:

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LOGICAL PIN NAME	HARDWARE DEVICE	FPGA PIN
Cabbage	SW[2]	PIN_P25
Goat	SW[1]	PIN_N26
Wolf	SW[0]	PIN_N25
Alarm	LEDG[7]	PIN_Y18

When you are done with your design, have the lab instructor verify it, and mark his/her initials in your answer sheet. Close all *lab2step2* files in Quartus II.

5.0 Complete
You are done with this lab. Ensure that all lab files are closed, exit Quartus II, log off the computer, and hand in your answer sheet. **Don't forget to write down your name, student ID, and your lab section number**.