Cpr E 281 LAB06
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 6 Answer Sheet

Name and Std ID:_____ **Lab Section:**_____

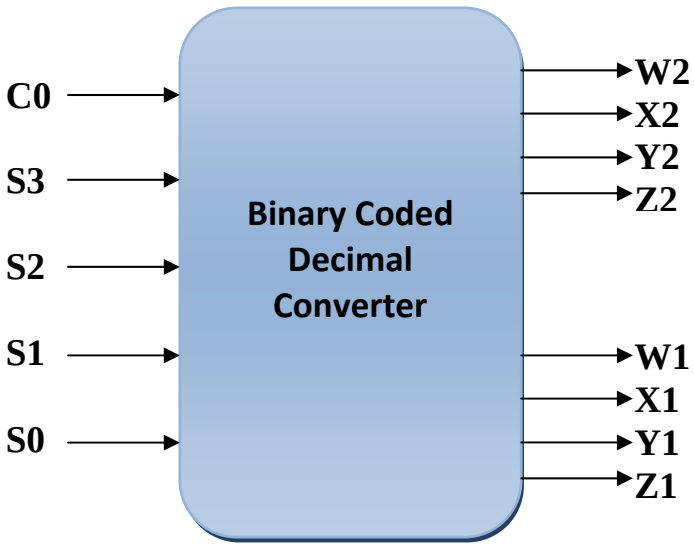
Date:_____

PRELAB:

Q1. Add the following numbers then write them in decimal:

Binary numbers to add a3 a2 a1 a0 + b3 b2 b1 b0	Binary result C0 S3 S2 S1 S0	Decimal conversion D2 D1 (Z2 Y2 X2 W2) (Z1 Y1 X1 W1)
1001 + 0111	10000	16
1011 + 1001		
1110 + 0101		
0010 + 1110		
1101 + 1011		

Q2. Consider the five-bit binary result (Co, S3, S2, S1, S0) representation in the table above. We would like to represent each combination as its equivalent in two decimal digits, each of which can be represented in binary as shown in the following table. Finish filling the following truth table.



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C0	S3	S2	S1	S0	Decimal		Z2	Y2	X2	W2	Z1	Y1	X1	W1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	1
0	0	0	1	0	0	2	0	0	0	0	0	0	1	0
0	0	0	1	1	0	3	0	0	0	0	0	0	1	1
0	0	1	0	0	0	4	0	0	0	0	0	1	0	0
0	0	1	0	1	0	5	0	0	0	0	0	1	0	1
0	0	1	1	0	0	6	0	0	0	0	0	1	1	0
0	0	1	1	1	0	7	0	0	0	0	0	1	1	1
0	1	0	0	0	0	8	0	0	0	0	1	0	0	0
0	1	0	0	1	0	9	0	0	0	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0	1	0	0	0	0
0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
0	1	1	0	0	1	2	0	0	0	1	0	0	1	0
0	1	1	0	1	1	3	0	0	0	1	0	0	1	1
0	1	1	1	0	1	4	0	0	0	1	0	1	0	0
0	1	1	1	1	1	5	0	0	0	1	0	1	0	1
1	0	0	0	0	1	6	0	0	0	1	0	1	1	0
1	0	0	0	1										
1	0	0	1	0										
1	0	0	1	1										
1	0	1	0	0										
1	0	1	0	1										
1	0	1	1	0										
1	0	1	1	1										
1	1	0	0	0										
1	1	0	0	1										
1	1	0	1	0										
1	1	0	1	1										
1	1	1	0	0										
1	1	1	0	1										
1	1	1	1	0										
1	1	1	1	1										

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Q3. Find the logic expressions for Z2, Y2, X2, W2, Z1, Y1, X1, W1 as function of C0, S3, S2, S1 and S0:

Z2 =

Y2 =

X2 =

W2 =

Z1 =

Y1 =

X1 =

W1 =

Q4. Write the verilog code for the Binary Coded Decimal Converter from **Section 3.3** using the assign statement.

Example:

```
module
        input …
        output …
        assign …
endmodule
```

TA Initials: _____

LAB:

Hardware demonstrates a good design. TA Initials: _____