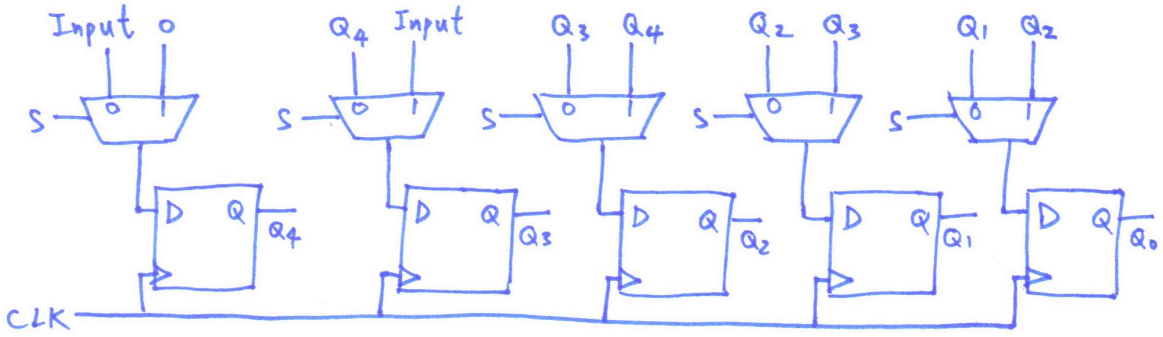
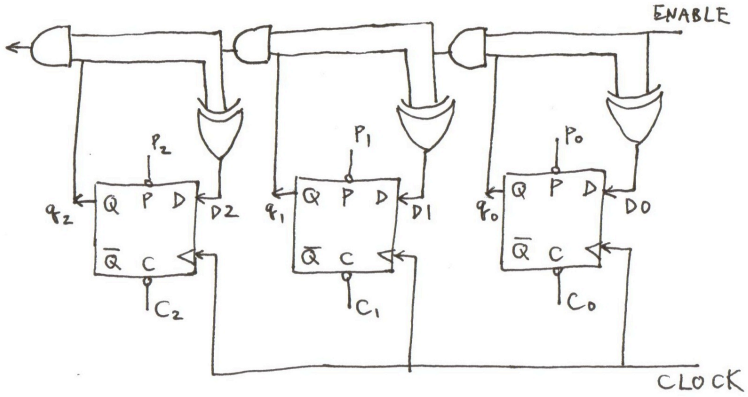
Recitation #9 Solutions

1. The circuit is given below:



2. (a) 3-bit up synchronous up-counter with enable:



All clear and preset signals should be set to 1, i.e., C2=C1=C0=P2=P1=P0=1.

(b) Clear and preset signals should be set as follows:

q2	q1	q0	C2	C1	C0	P2	P1	P0
0	0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1
1	0	1	0	0	0	1	1	1
1	1	0	d	d	d	d	d	d
1	1	1	d	d	d	d	d	d

C2=C1=C0=(q2'+q0')
P2=P1=P0=1

(c) Clear and preset signals should be set as follows:

q2	q1	q0	C2	C1	C0	P2	P1	P0
0	0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	1	0	1	0	1	0
1	0	0	d	d	d	d	d	d
1	0	1	0	0	0	1	1	1
1	1	0	d	d	d	d	d	d
1	1	1	d	d	d	d	d	d

C2=C0=q2', C1=q2'(q1'+q0')
P2=P0=(q1'+q0'), P1=1

3. (a) Clear and preset signals should be set as follows:

q2	q1	q0	C2	C1	C0	P2	P1	P0
0	0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	0	0	0	1	1	1
1	1	1	d	d	d	d	d	d

C2=C1=C0=(q2'+q1')
P2=P1=P0=1

(b) Ideally, all flip-flops will be forced to 0 at the same time when q2=1, q1=1 and q0=0 (or 1). However, if the flip-flops switch at different speeds, one of q2 and q1 may be changed to 0 while the other may still be 1. Then the C signals may be changed to 1 before all flip-flops are cleared.

4. The idea of a 4-bit ring counter is described in Ch. 5.11.2 and Fig. 5.28 in textbook. The following modification is needed to make it a 6-bit ring counter. First, the 3-bit counter should be converted to a modulo-6 counter by clearing it after 101 is detected. Second, only Q0, Q1, …, Q5 of the 3-to-8 decoder are treated as outputs of the 6-bit ring counter. Q6 and Q7 are ignored.