



CprE 281: Digital Logic

Instructor: Alexander Stoytchev

<http://www.ece.iastate.edu/~alexs/classes/>

Registers

CprE 281: Digital Logic
Iowa State University, Ames, IA
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Administrative Stuff

- **The second midterm is next Friday.**
- **Homework 8 is due next Monday.**

Administrative Stuff

- **Midterm Exam #2**
- **When: Friday October 30 @ 4pm.**
- **Where: This classroom**
- **What: Chapters 1, 2, 3, 4 and 5.1-5.7**
- **The exam will be open book and open notes (you can bring up to 3 pages of handwritten notes).**

Midterm 2: Format

- The exam will be out of 130 points
- You need 95 points to get an A
- It will be great if you can score more than 100 points.
 - but you can't roll over your extra points ☹️

Midterm 2: Topics

- **Binary Numbers and Hexadecimal Numbers**
- **1's complement and 2's complement representation**
- **Addition and subtraction of binary numbers**
- **Circuits for adders and fast adders**

- **Single and Double precision IEEE floating point formats**
- **Converting a real number to the IEEE format**
- **Converting a floating point number to base 10**

- **Multiplexers (circuits and function)**
- **Synthesis of logic functions using multiplexers**
- **Shannon's Expansion Theorem**

Midterm 2: Topics

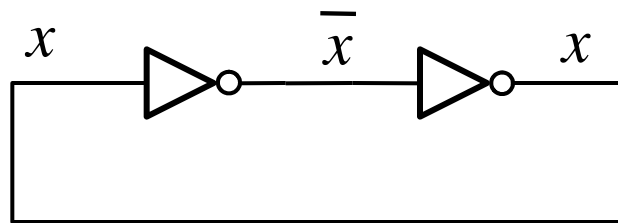
- **Decoders (circuits and function)**
- **Demultiplexers**
- **Encoders (binary and priority)**
- **Code Converters**
- **K-maps for 2, 3, and 4 variables**

- **Synthesis of logic circuits using adders, multiplexers, encoders, decoders, and basic logic gates**
- **Synthesis of logic circuits given constraints on the available building blocks that you can use**

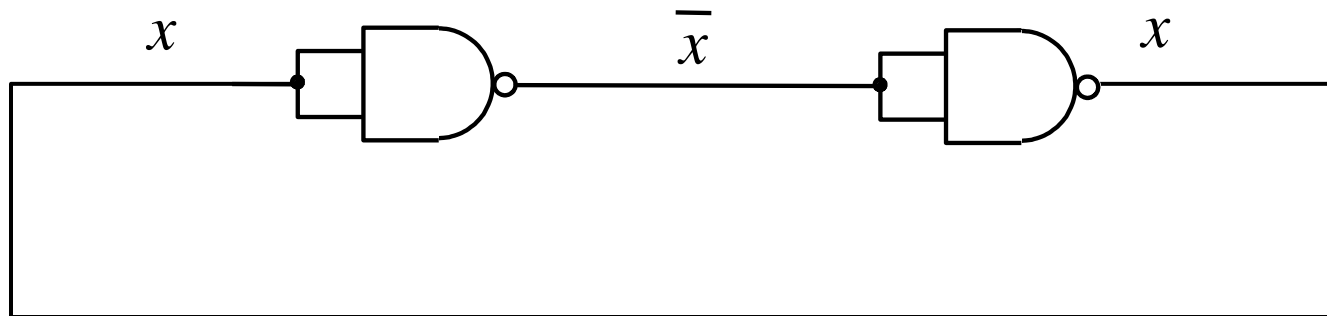
- **Latches (circuits, behavior, timing diagrams)**
- **Flip-Flops (circuits, behavior, timing diagrams)**

Review of Flip-Flops

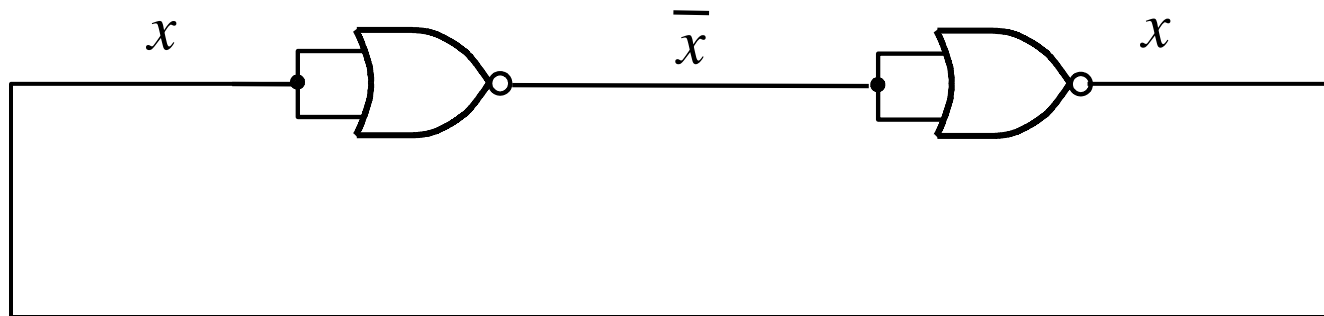
A simple memory element with NOT Gates



A simple memory element with NAND Gates

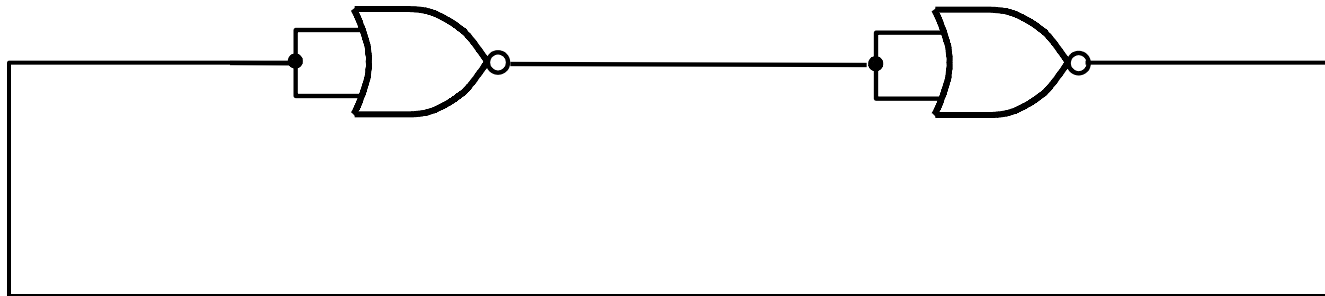


A simple memory element with NOR Gates

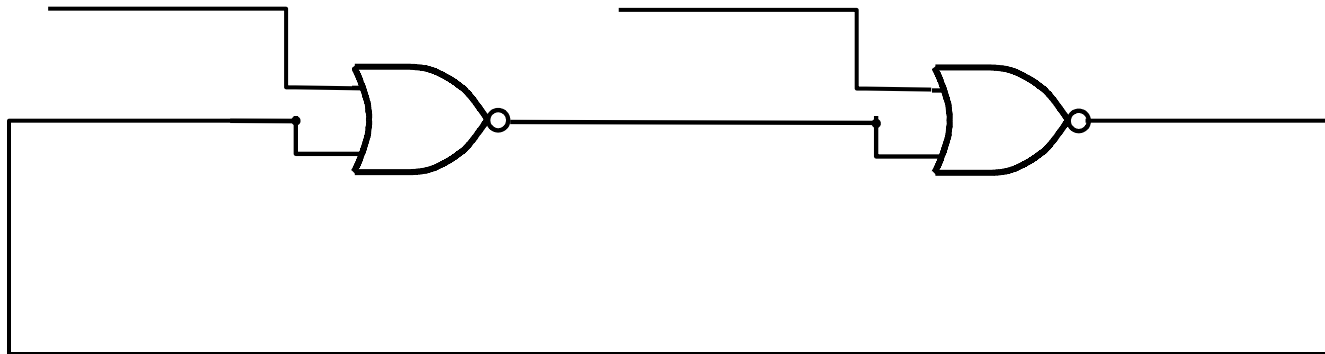


Basic Latch

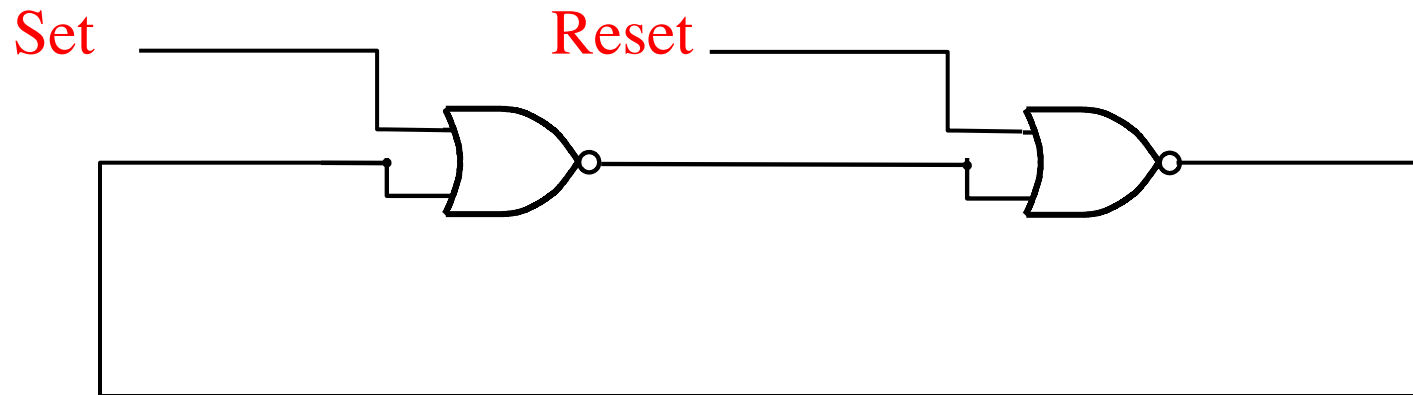
A simple memory element with NOR Gates



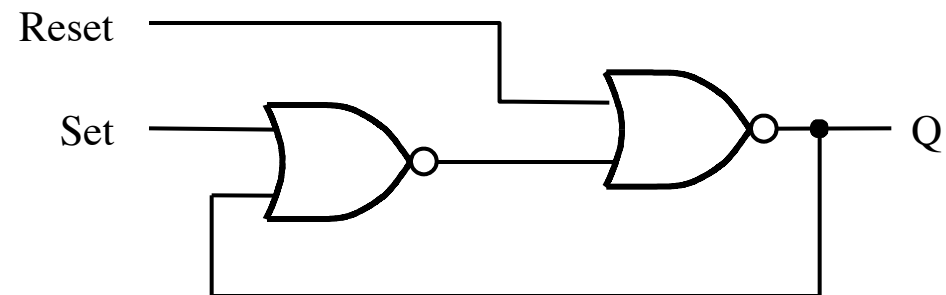
A simple memory element with NOR Gates



A simple memory element with NOR Gates

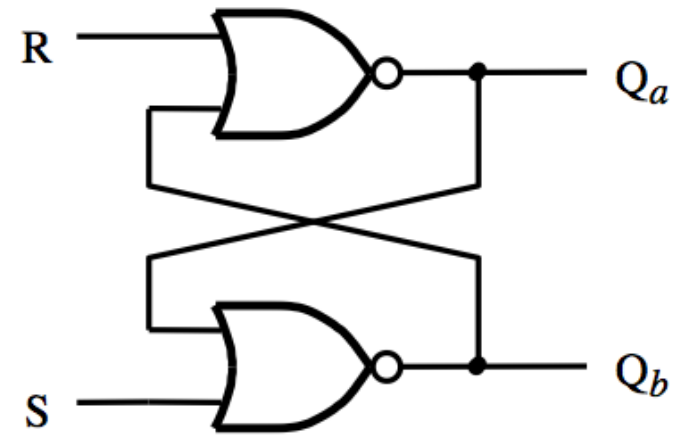
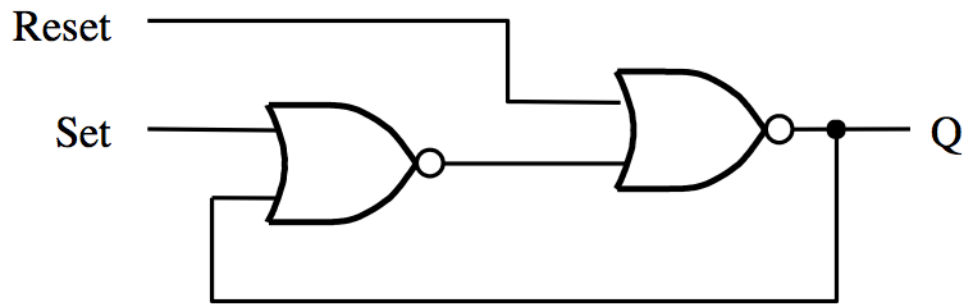


A memory element with NOR gates



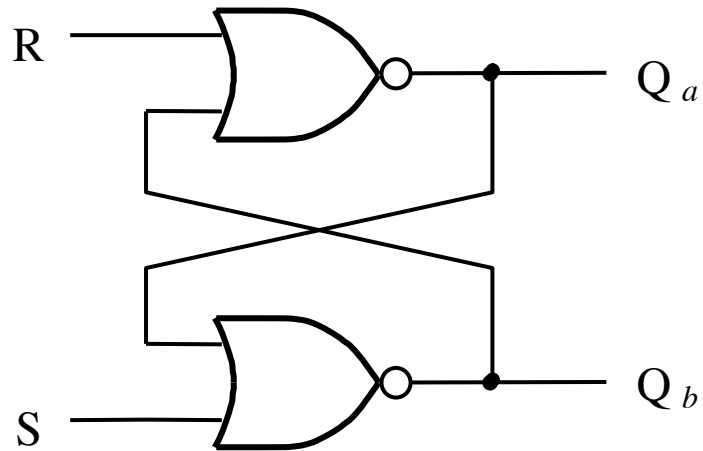
[Figure 5.3 from the textbook]

Two Different Ways to Draw the Same Circuit



[Figure 5.3 & 5.4 from the textbook]

SR Latch: Circuit and Truth Table



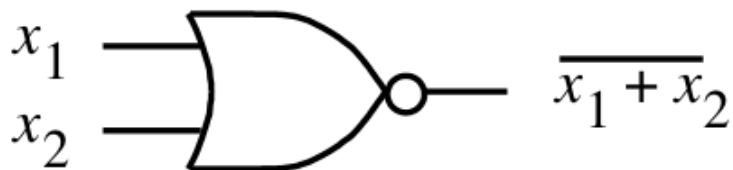
(a) Circuit

S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	(Undesirable)

(b) Truth table

[Figure 5.4a,b from the textbook]

NOR Gate

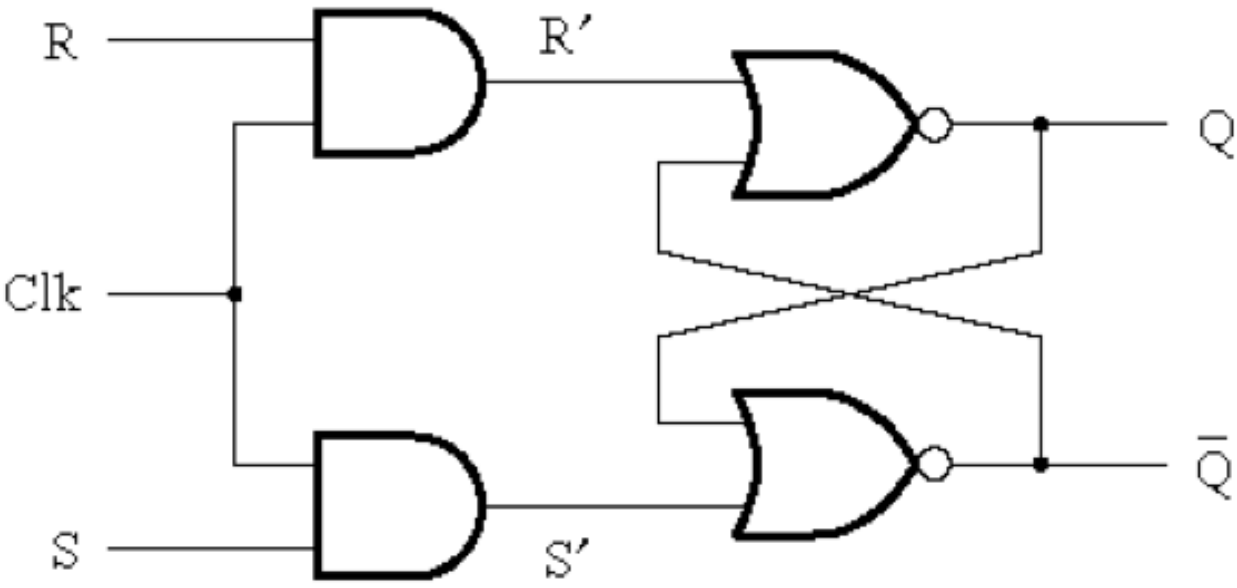


NOR Gate Truth table

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

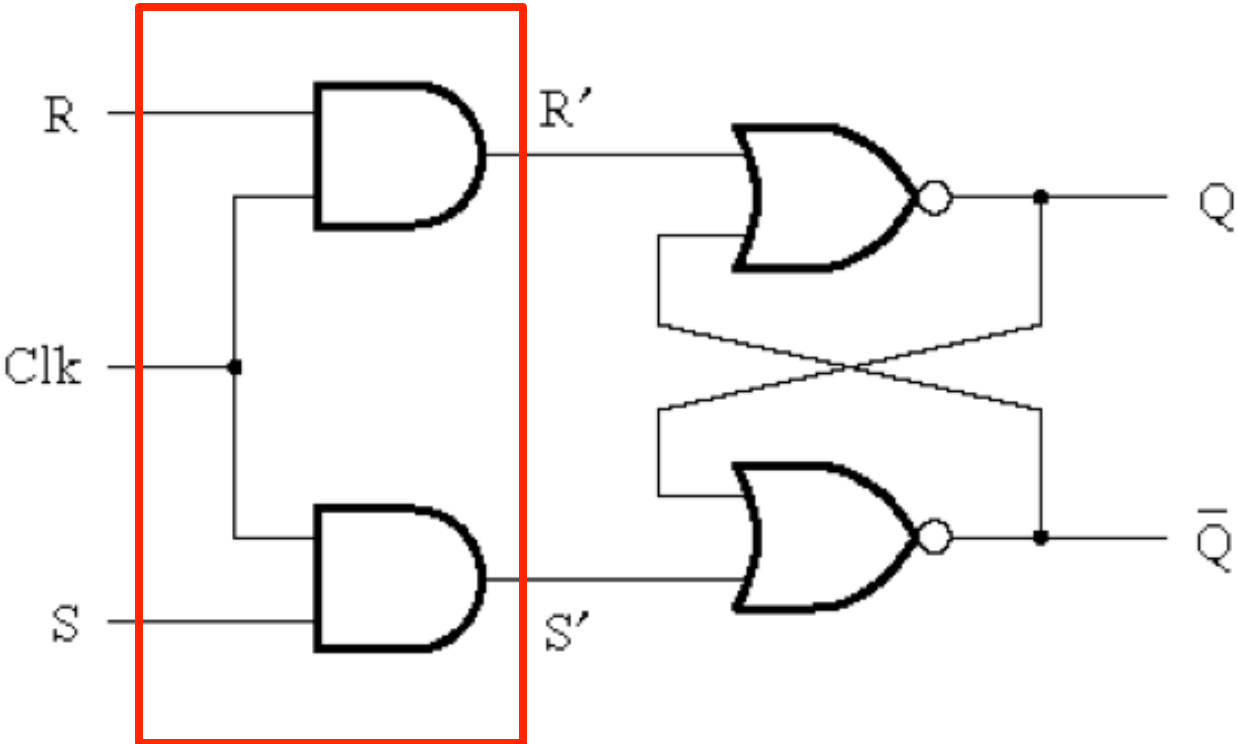
Gated SR Latch

Circuit Diagram for the Gated SR Latch



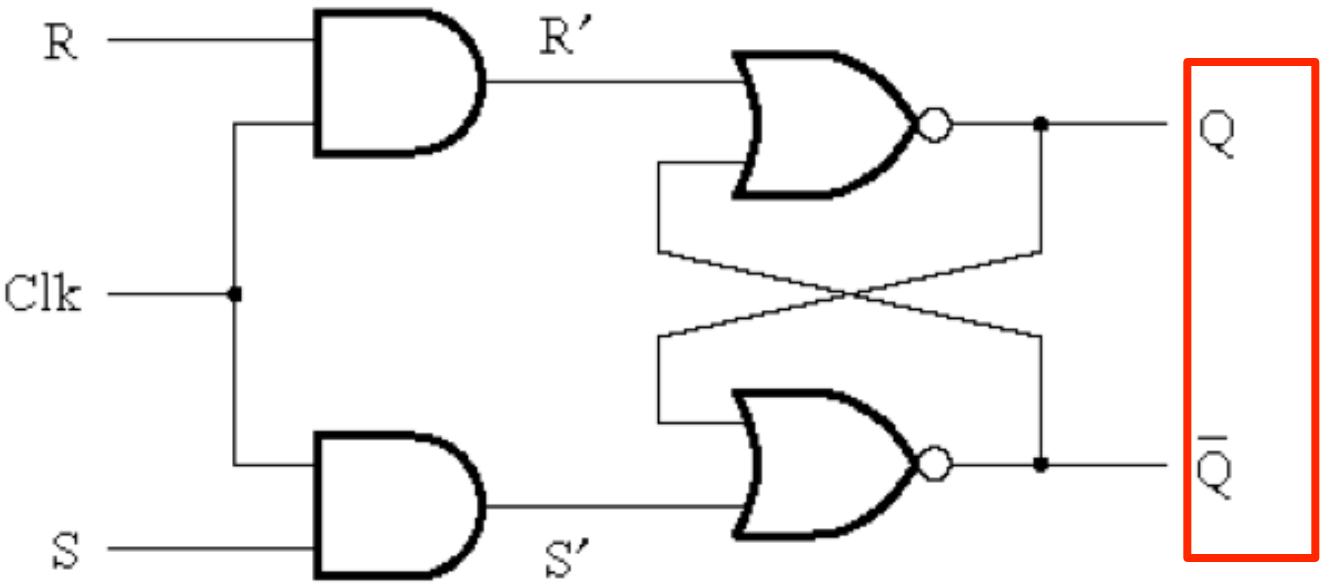
[Figure 5.5a from the textbook]

Circuit Diagram for the Gated SR Latch



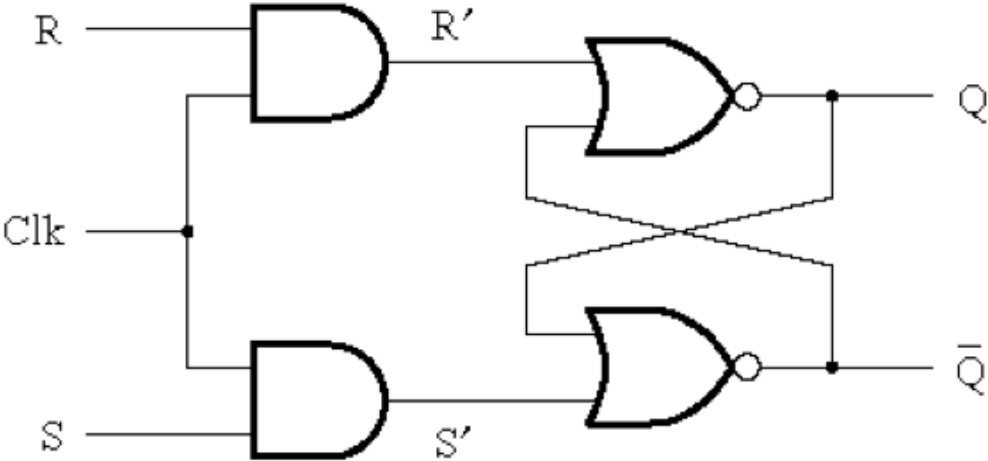
This is the “gate”
of the gated latch

Circuit Diagram for the Gated SR Latch

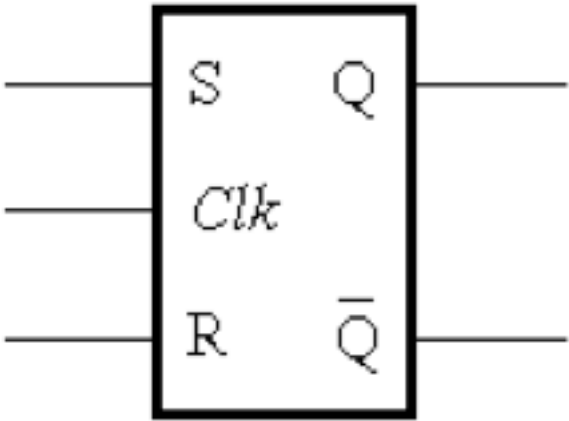


Notice that these are complements of each other

Gated SR Latch: Circuit Diagram, Characteristic Table, and Graphical Symbol

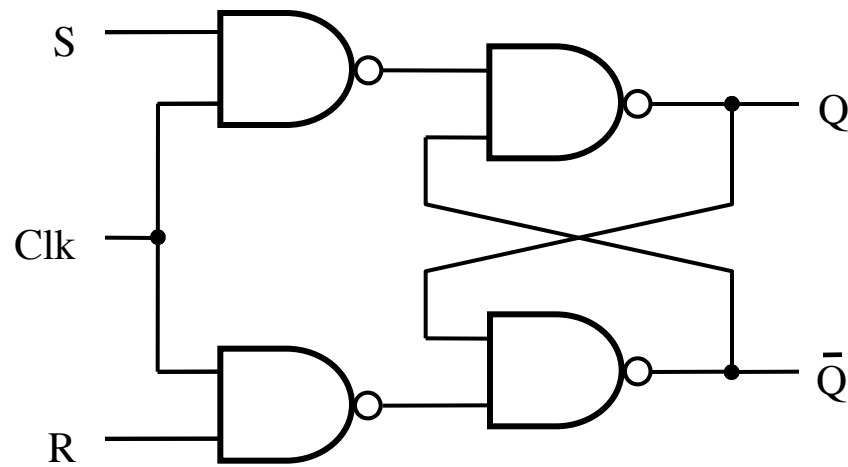


Clk	S	R	$Q(t + 1)$
0	x	x	$Q(t)$ (no change)
1	0	0	$Q(t)$ (no change)
1	0	1	0
1	1	0	1
1	1	1	x (Undesirable)



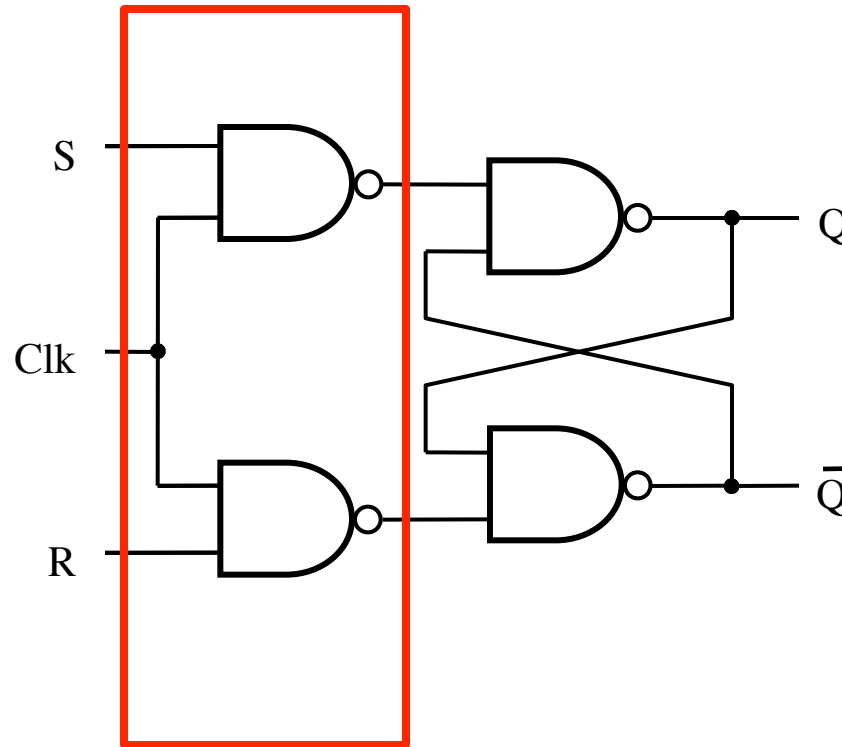
[Figure 5.5 from the textbook]

Gated SR latch with NAND gates



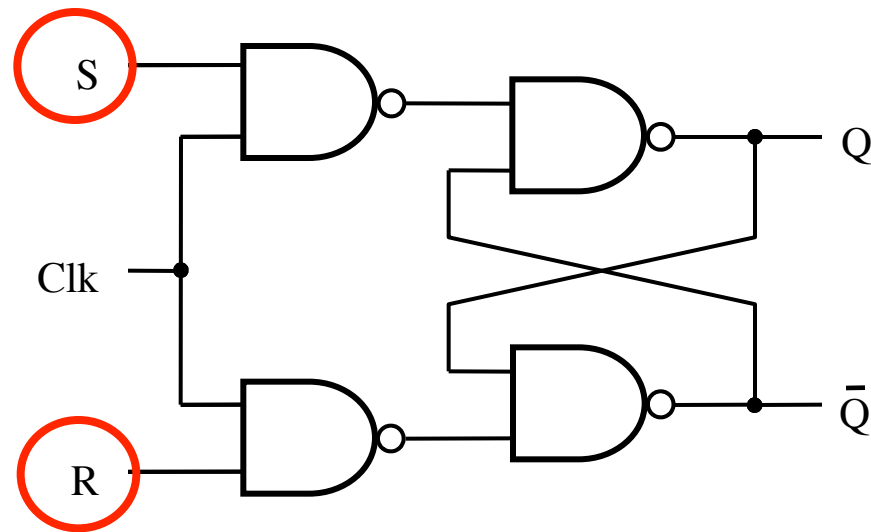
[Figure 5.6 from the textbook]

Gated SR latch with NAND gates



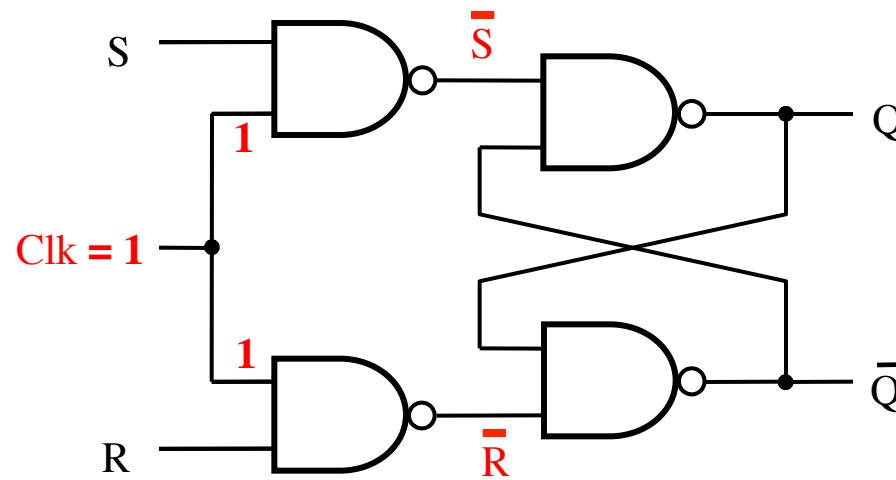
In this case the “gate” is constructed using NAND gates! Not AND gates.

Gated SR latch with NAND gates



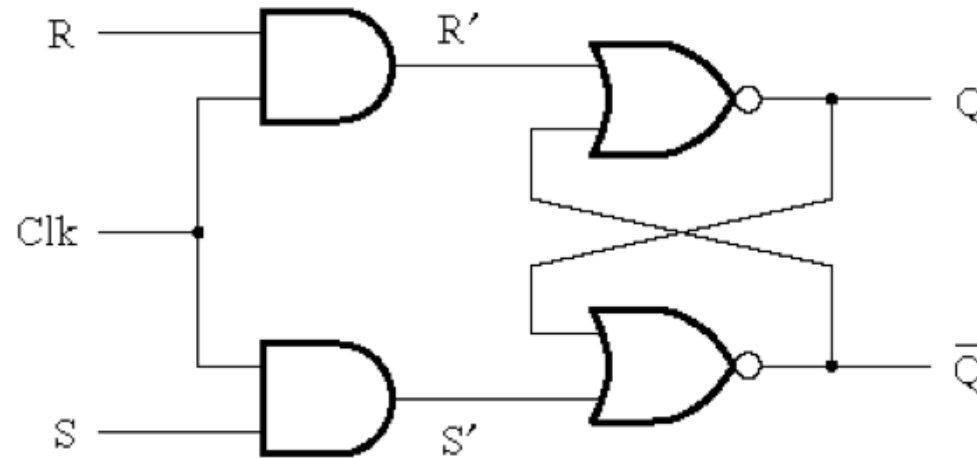
Also, notice that the positions of S and R are now swapped.

Gated SR latch with NAND gates

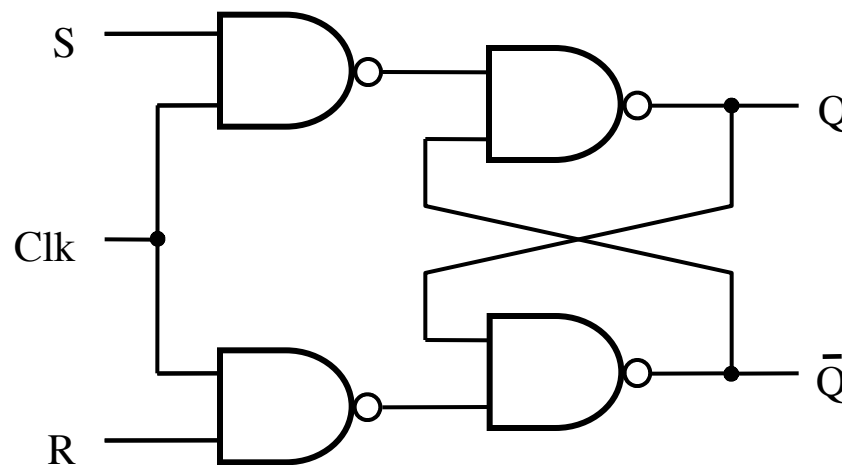


Finally, notice that when $\text{Clk}=1$ this turns into the basic latch with NAND gates, i.e., the $\bar{S}\bar{R}$ Latch.

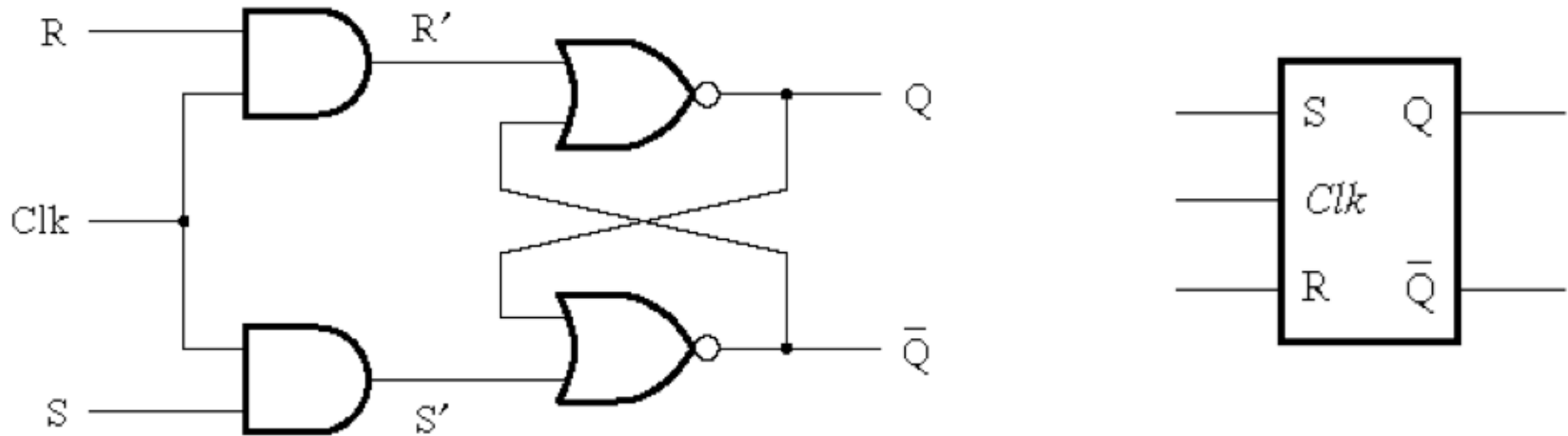
Gated SR latch with NOR gates



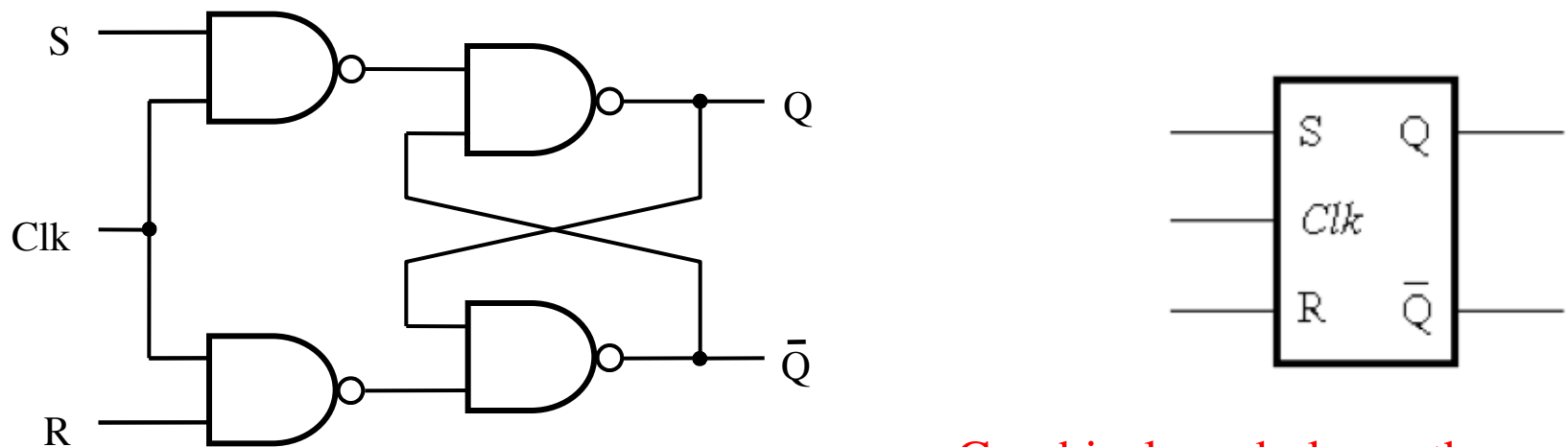
Gated SR latch with NAND gates



Gated SR latch with NOR gates

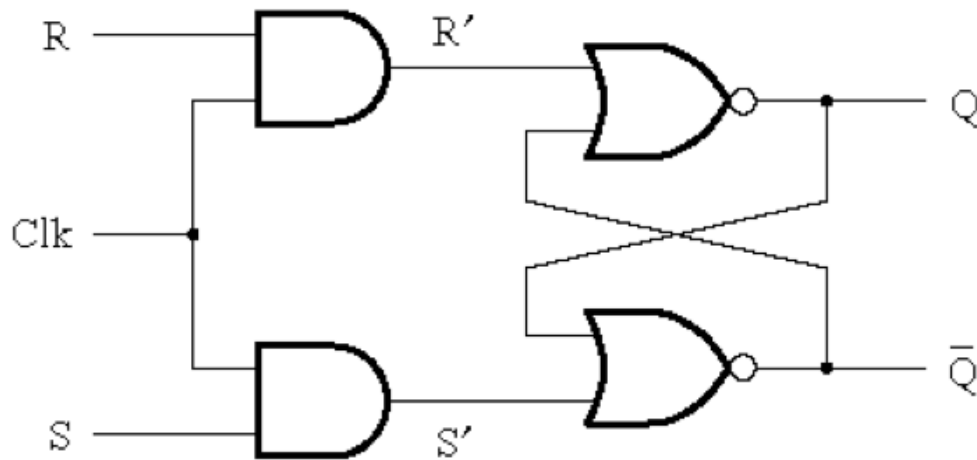


Gated SR latch with NAND gates



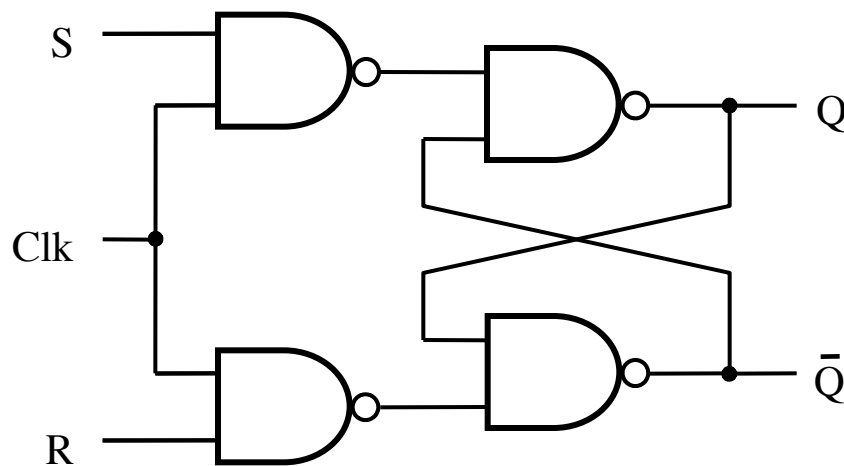
Graphical symbols are the same

Gated SR latch with NOR gates



Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x (undesirable)

Gated SR latch with NAND gates

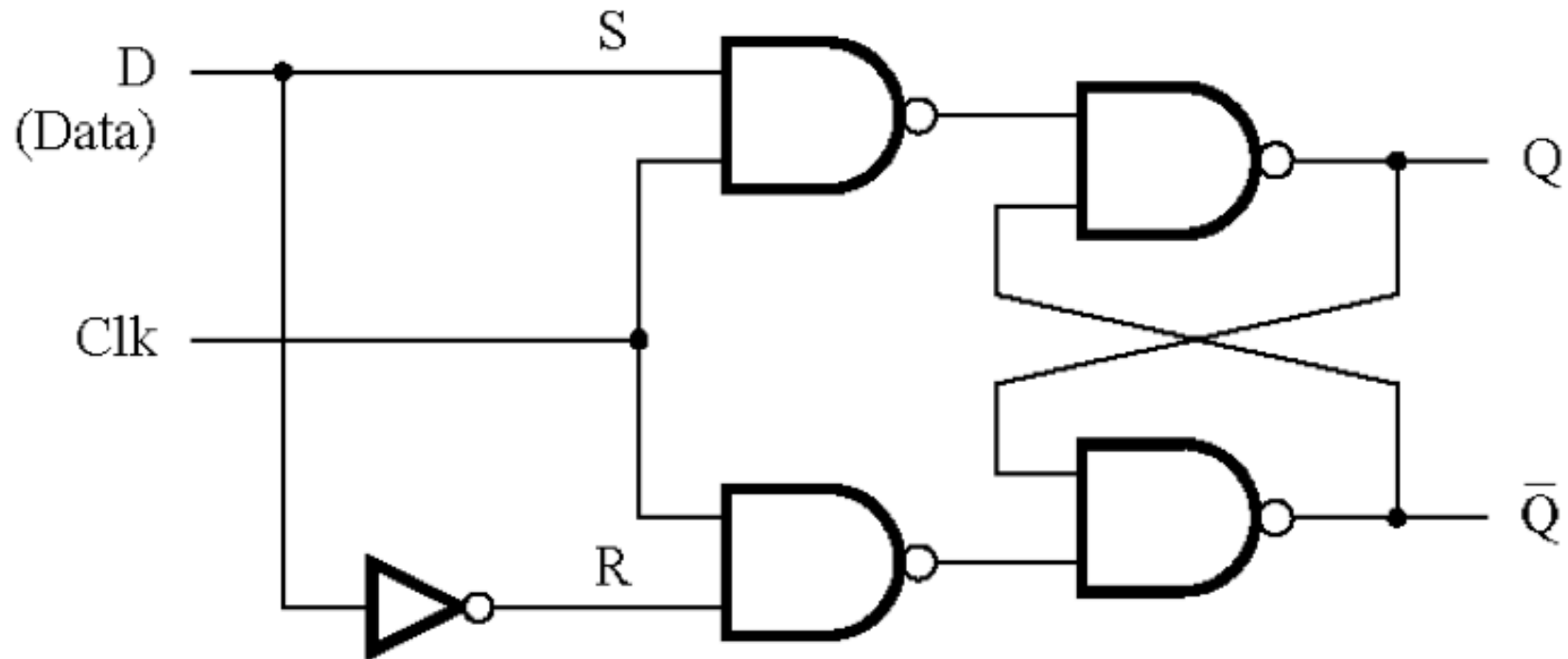


Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x (undesirable)

Characteristic tables are the same

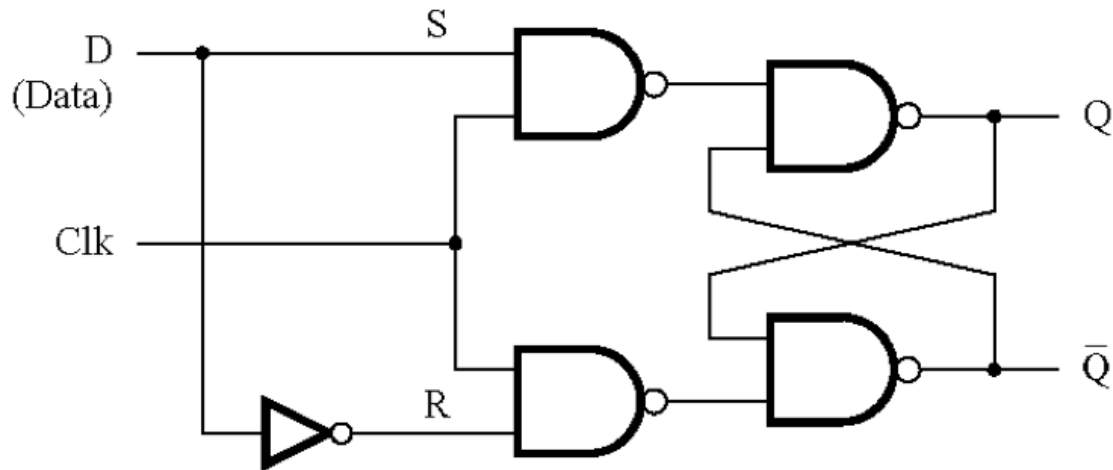
Gated D Latch

Circuit Diagram for the Gated D Latch



[Figure 5.7a from the textbook]

Gated D Latch: Circuit Diagram, Characteristic Table, and Graphical Symbol

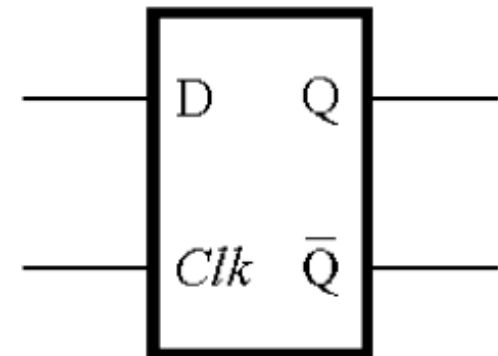


Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

Note that it is now impossible to have $S=R=1$.

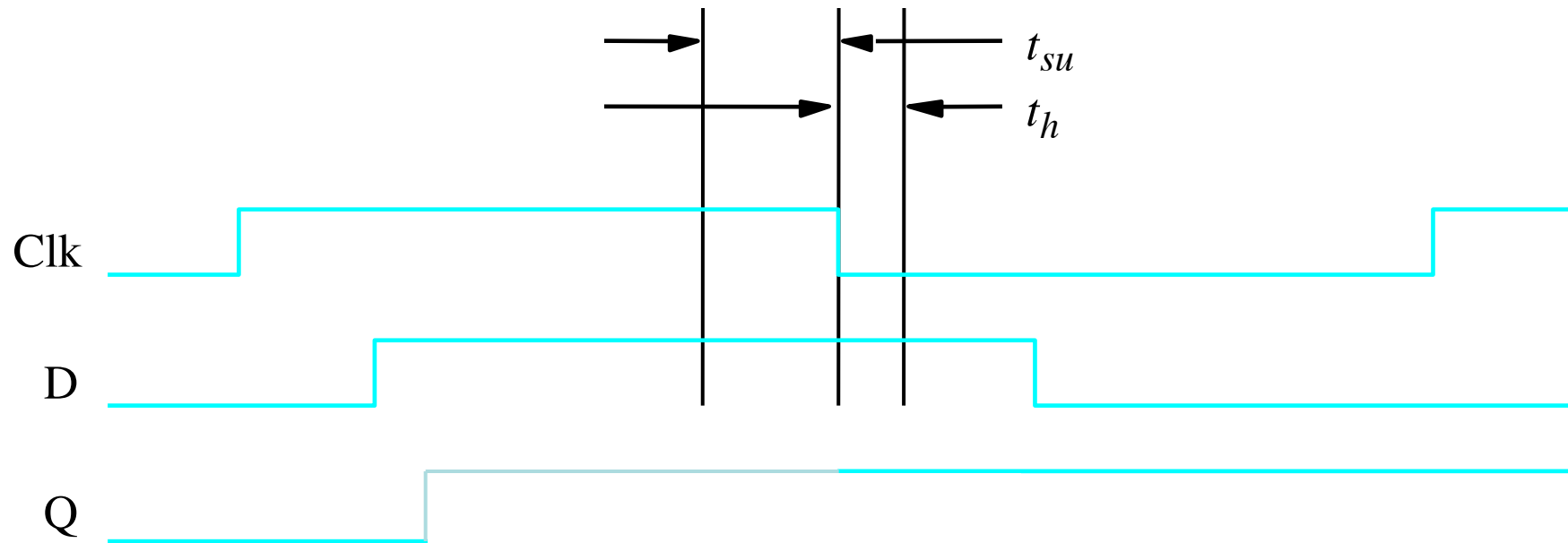
When $Clk=1$ the output follows the D input.

When $Clk=0$ the output cannot be changed.



[Figure 5.7a,b from the textbook]

Setup and hold times for Gated D latch



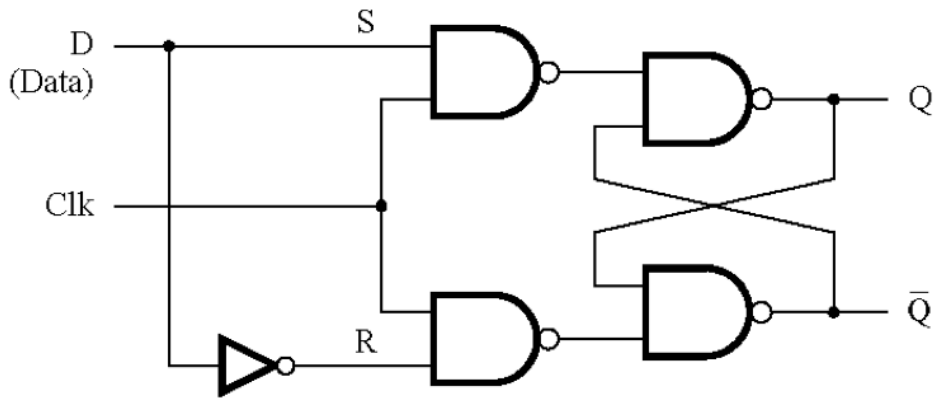
Setup time (t_{su}) – the minimum time that the D signal must be stable prior to the the negative edge of the Clock signal

Hold time (t_h) – the minimum time that the D signal must remain stable after the the negative edge of the Clock signal

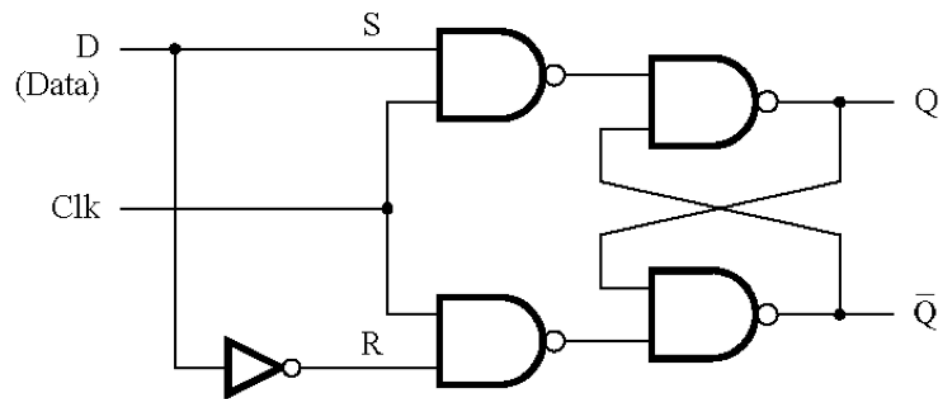
Master-Slave D Flip-Flop

Constructing a Master-Slave D Flip-Flop From Two D Latches

Master



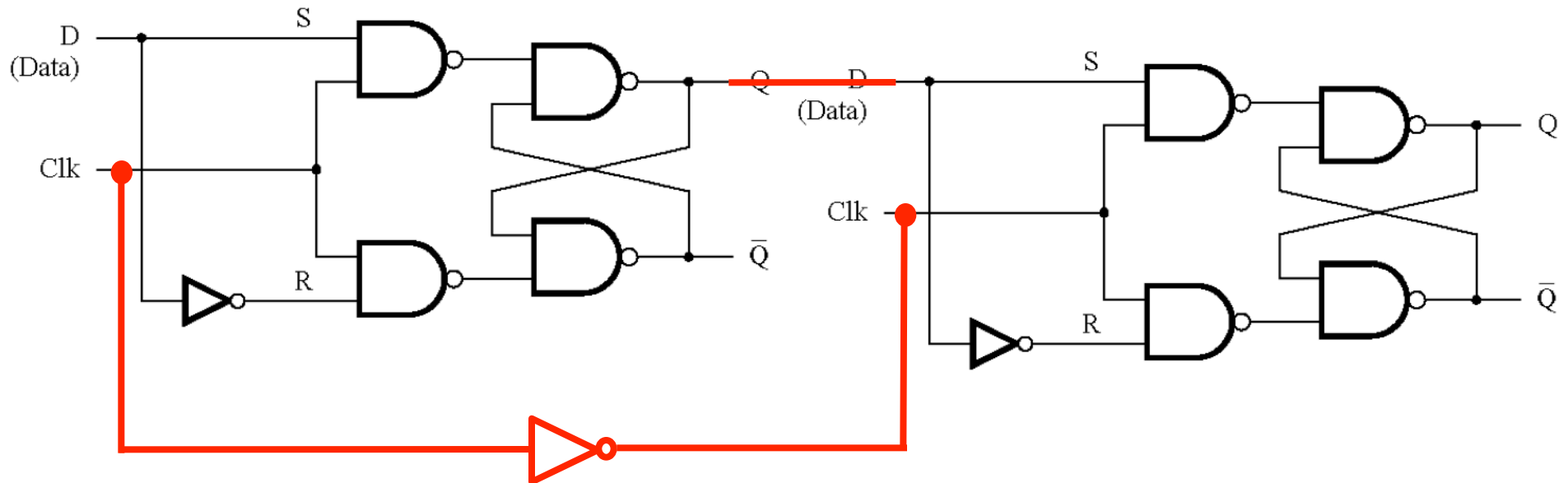
Slave



Constructing a Master-Slave D Flip-Flop From Two D Latches

Master

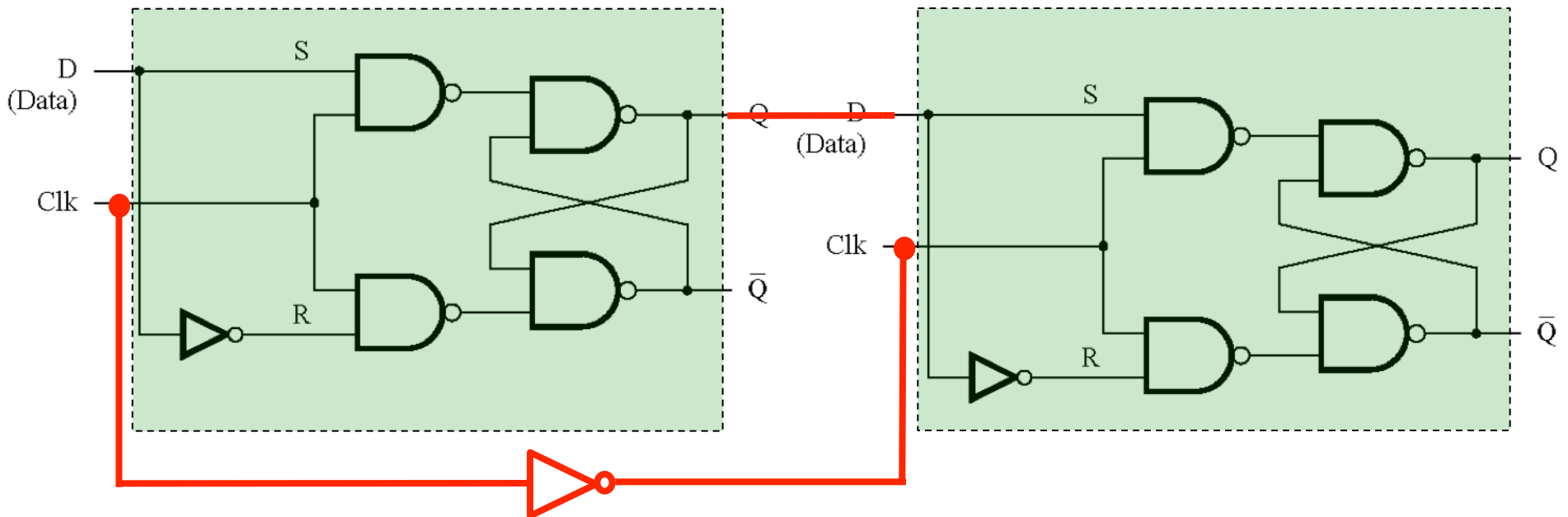
Slave



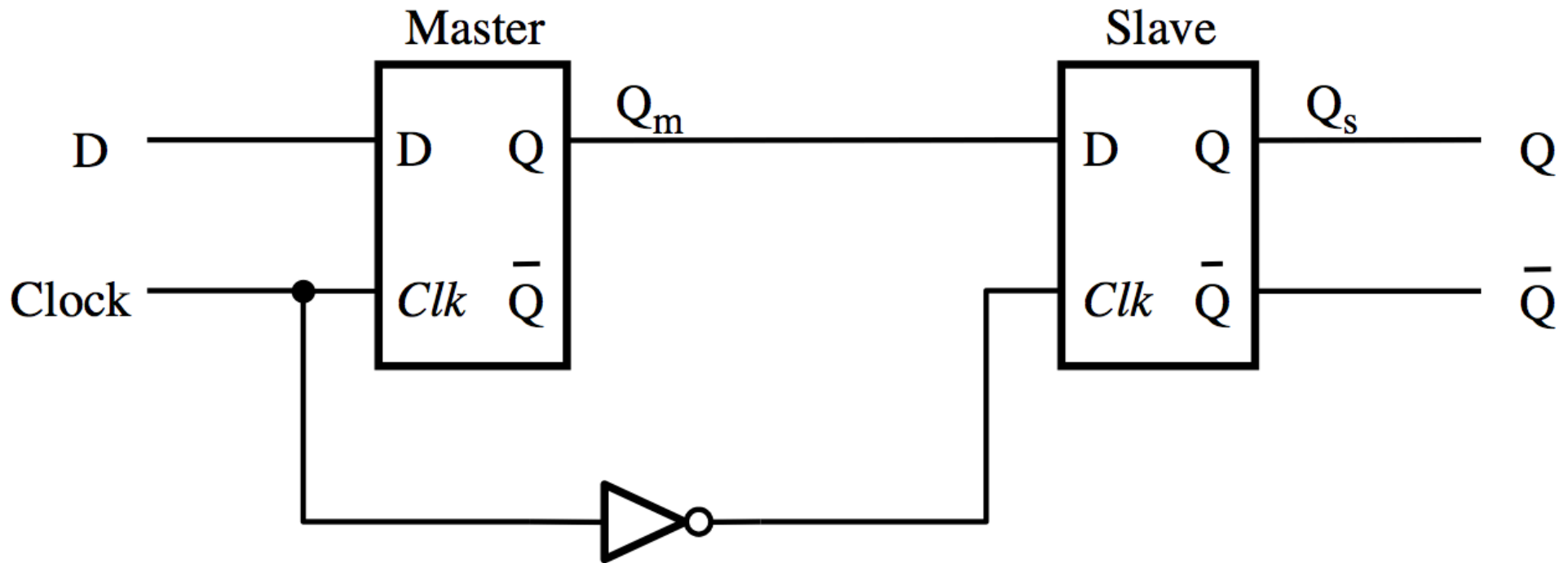
Constructing a Master-Slave D Flip-Flop From Two D Latches

Master

Slave



Constructing a Master-Slave D Flip-Flop From Two D Latches

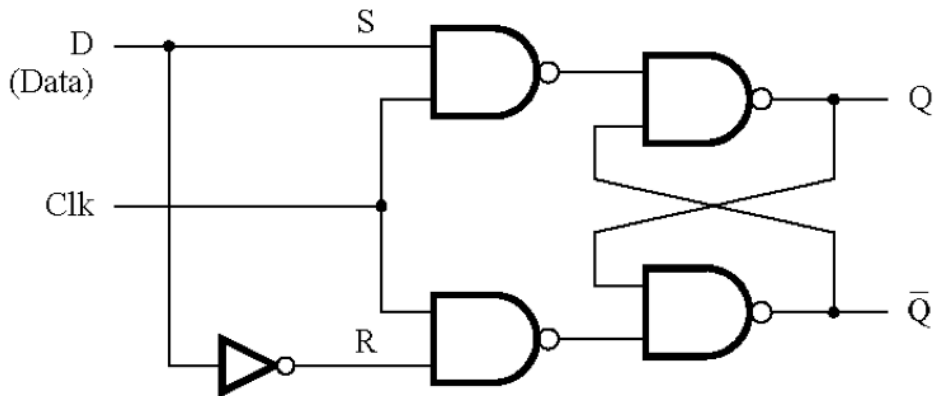


[Figure 5.9a from the textbook]

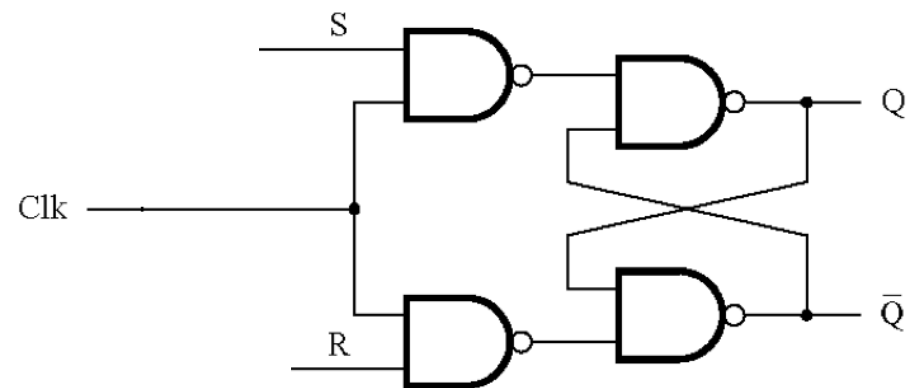
Constructing a Master-Slave D Flip-Flop From one D Latch and one Gated SR Latch

(This version uses one less NOT gate)

Master



Slave

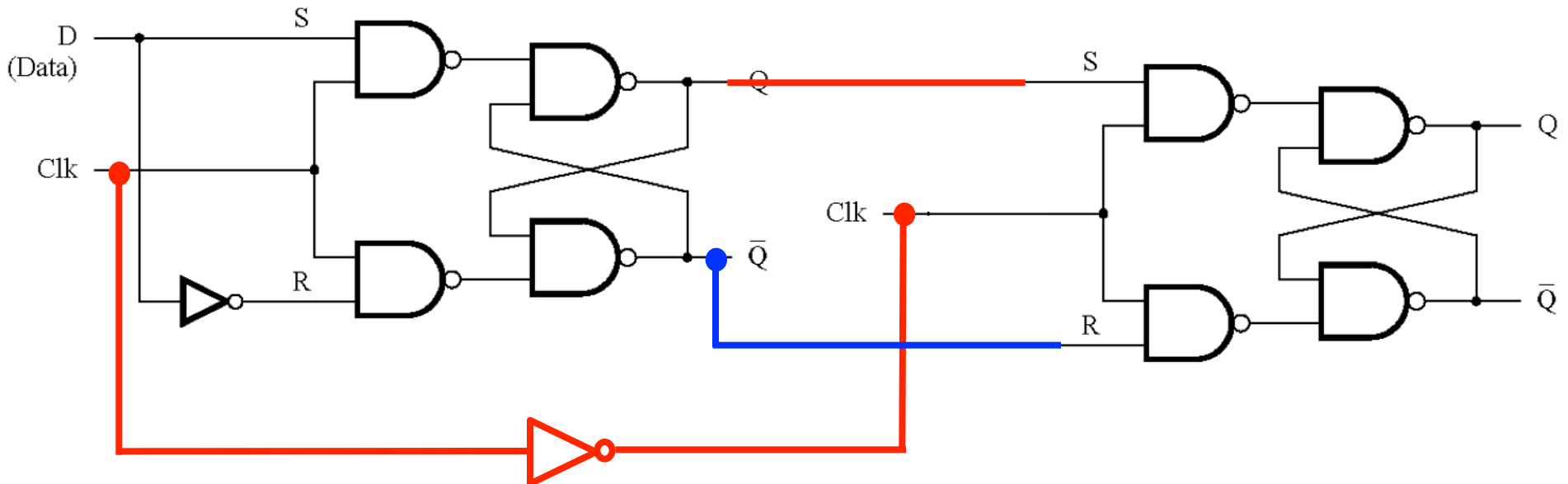


Constructing a Master-Slave D Flip-Flop From one D Latch and one Gated SR Latch

(This version uses one less NOT gate)

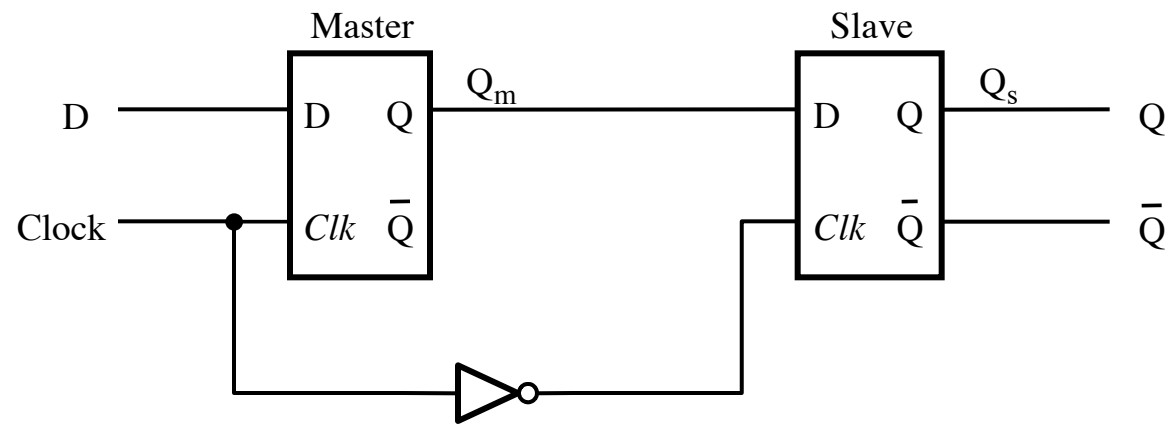
Master

Slave



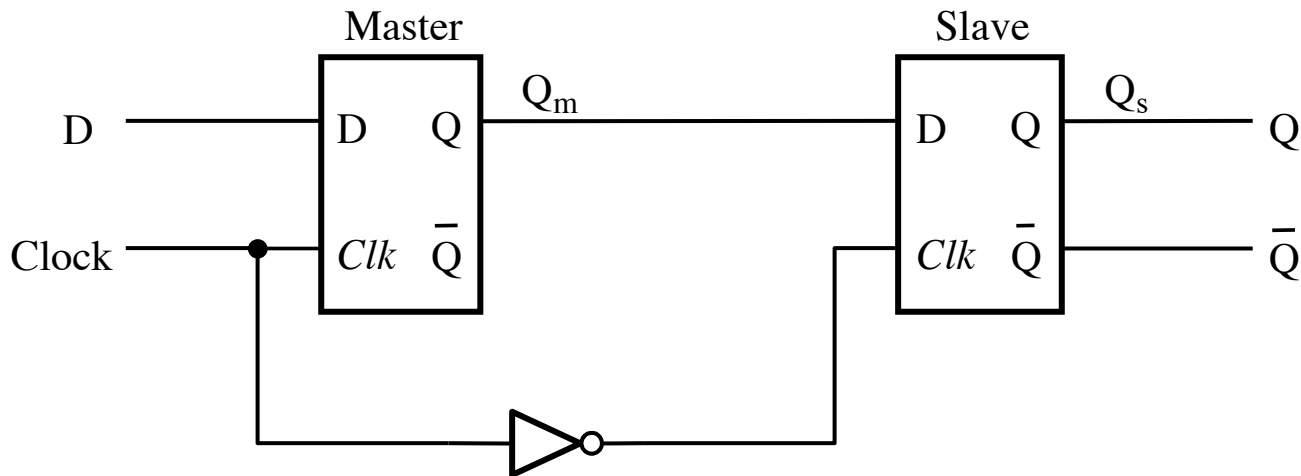
Edge-Triggered D Flip-Flops

Master-Slave D Flip-Flop

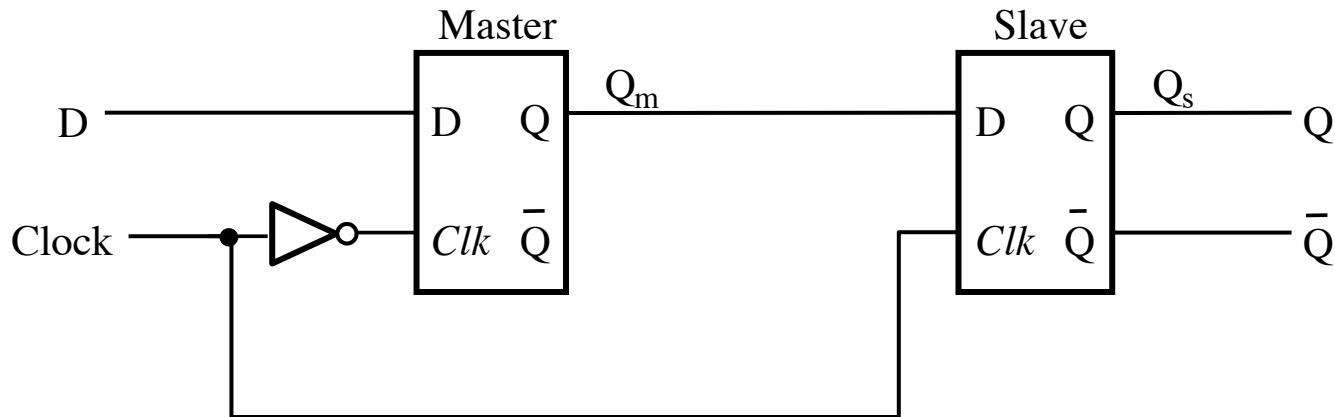


(a) Circuit

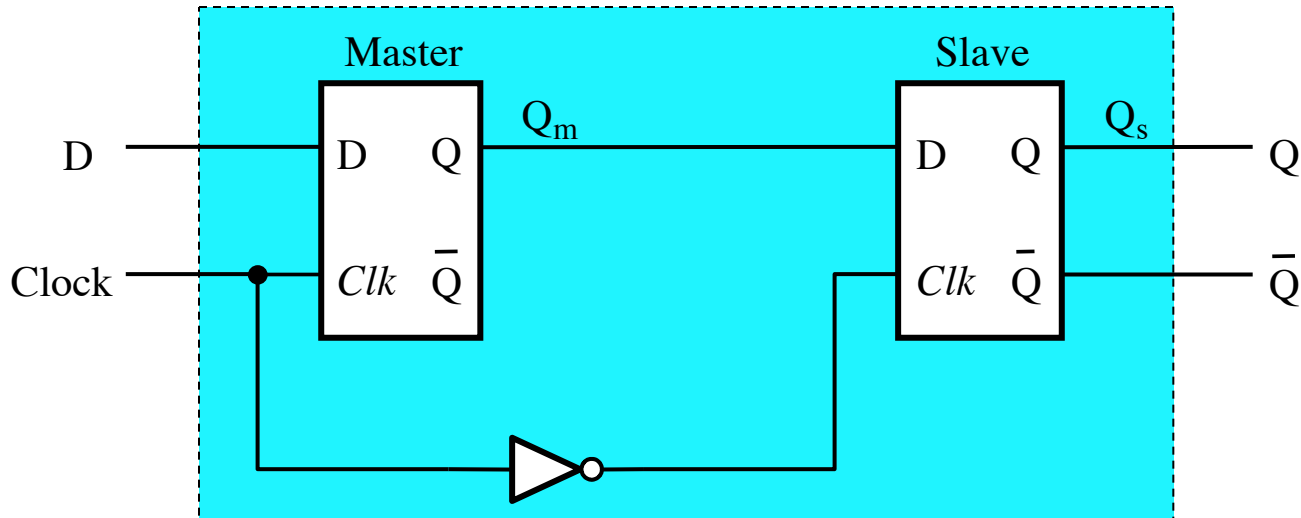
Negative-Edge-Triggered Master-Slave D Flip-Flop



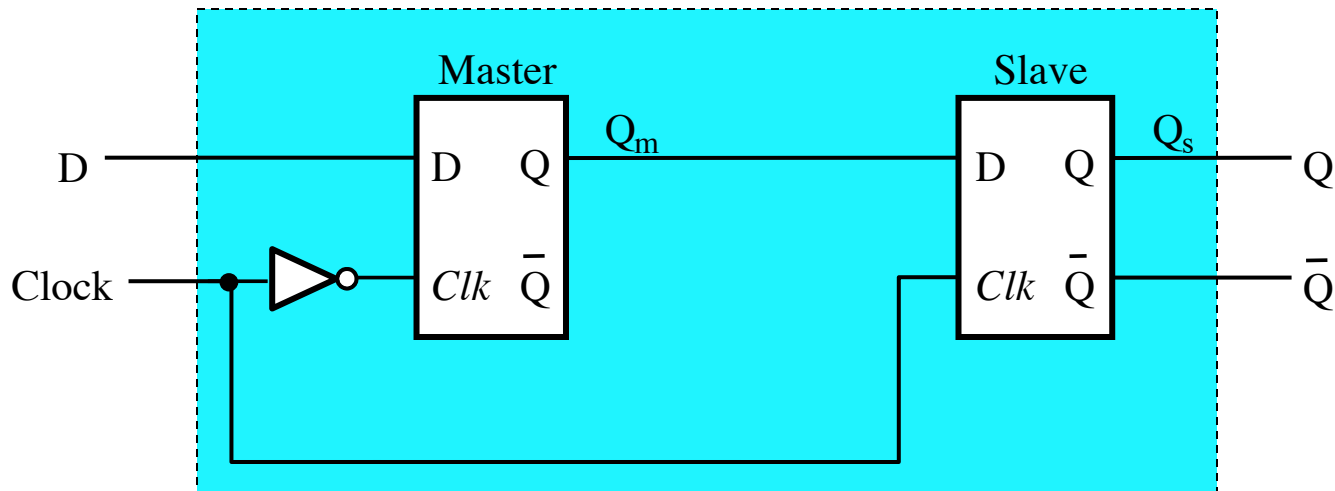
Positive-Edge-Triggered Master-Slave D Flip-Flop



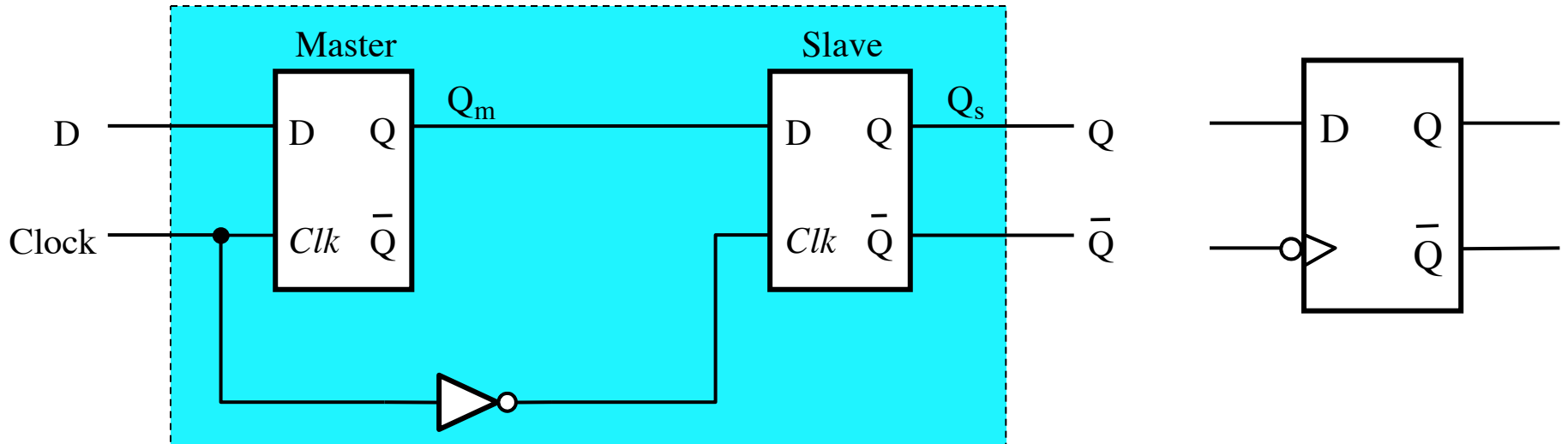
Negative-Edge-Triggered Master-Slave D Flip-Flop



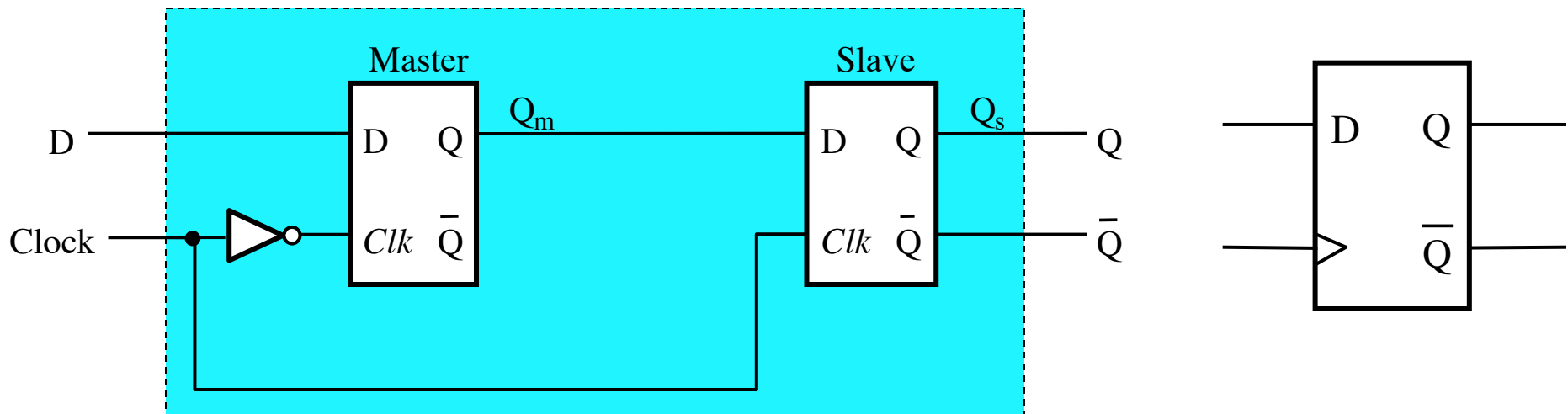
Positive-Edge-Triggered Master-Slave D Flip-Flop



Negative-Edge-Triggered Master-Slave D Flip-Flop

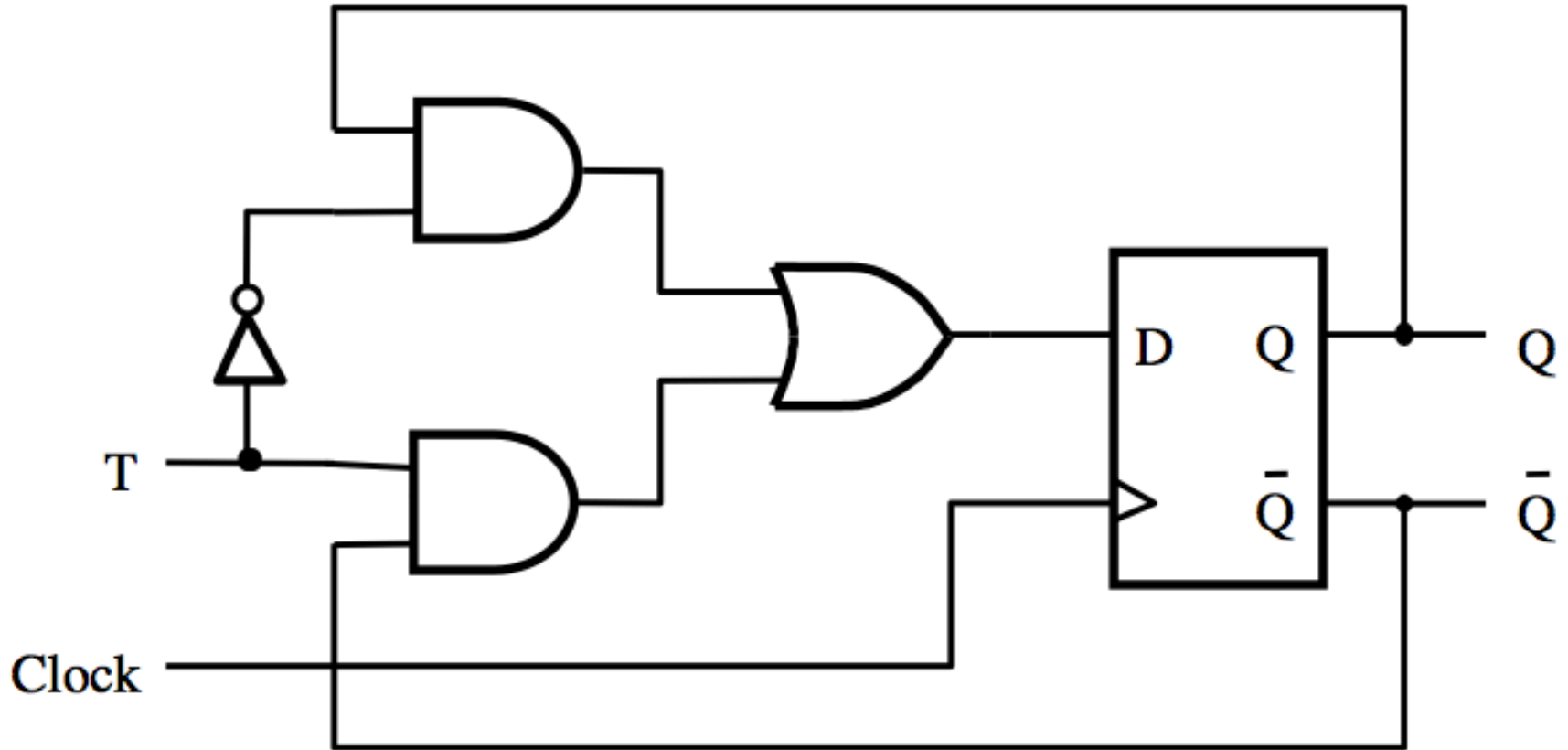


Positive-Edge-Triggered Master-Slave D Flip-Flop



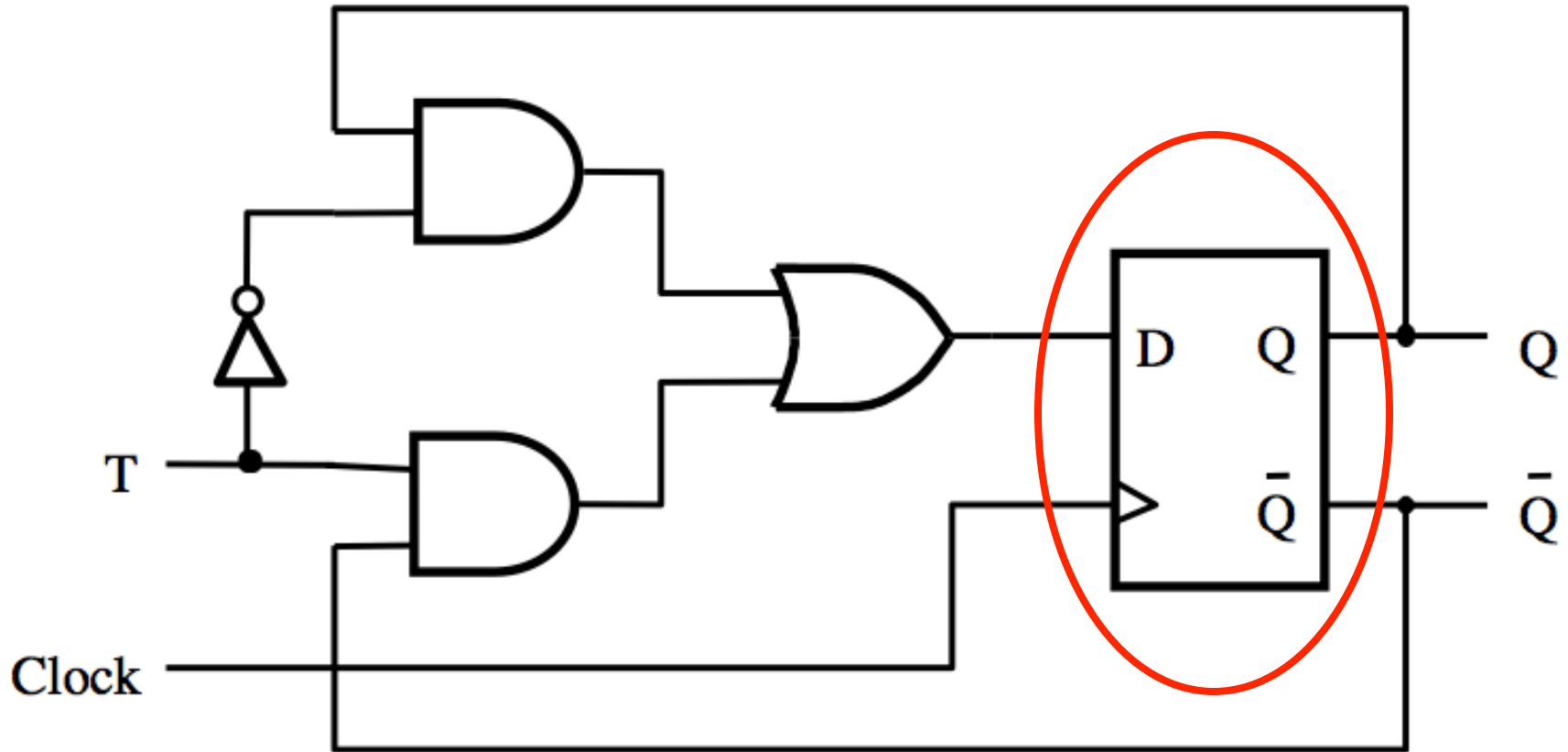
T Flip-Flop

T Flip-Flop



[Figure 5.15a from the textbook]

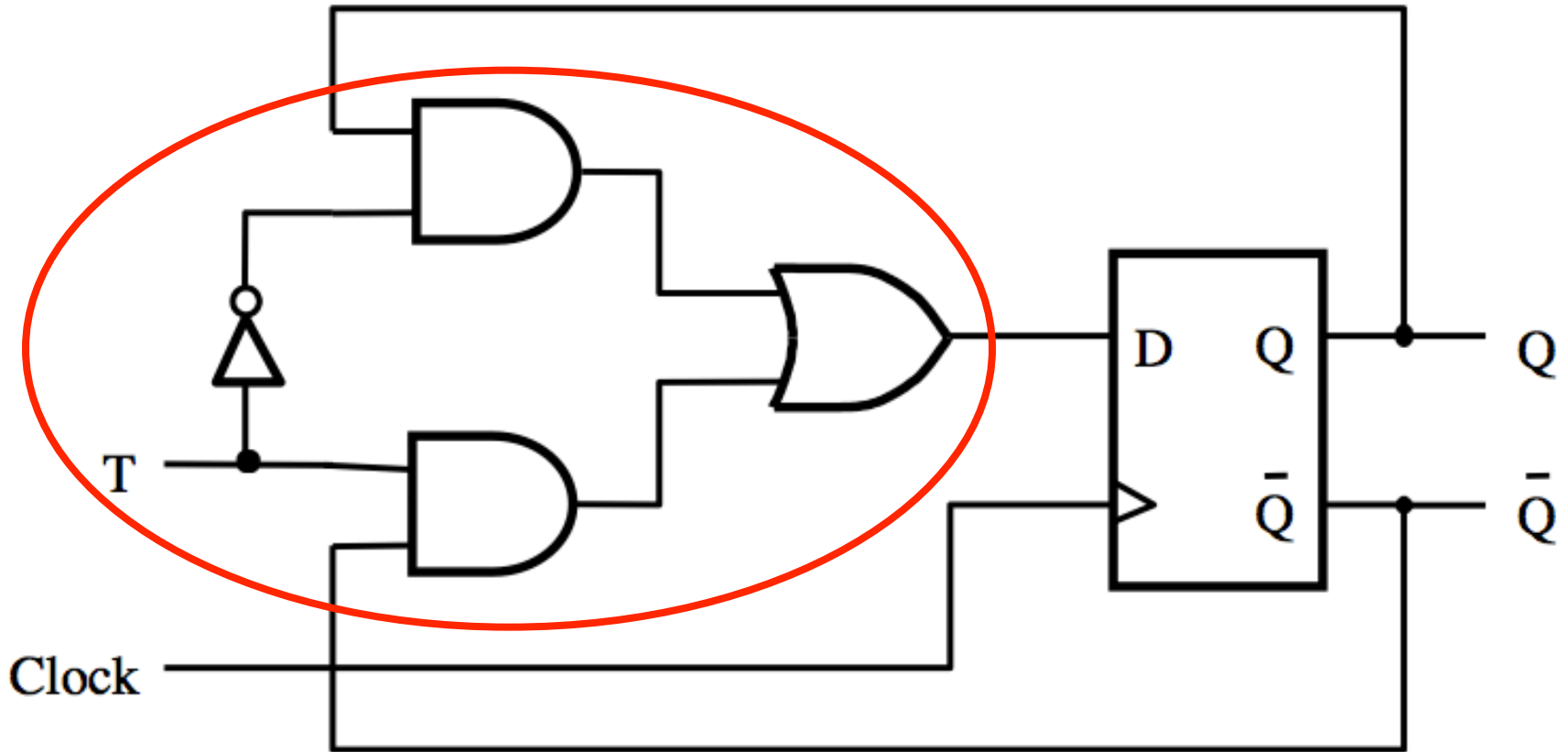
T Flip-Flop



Positive-edge-triggered
D Flip-Flop

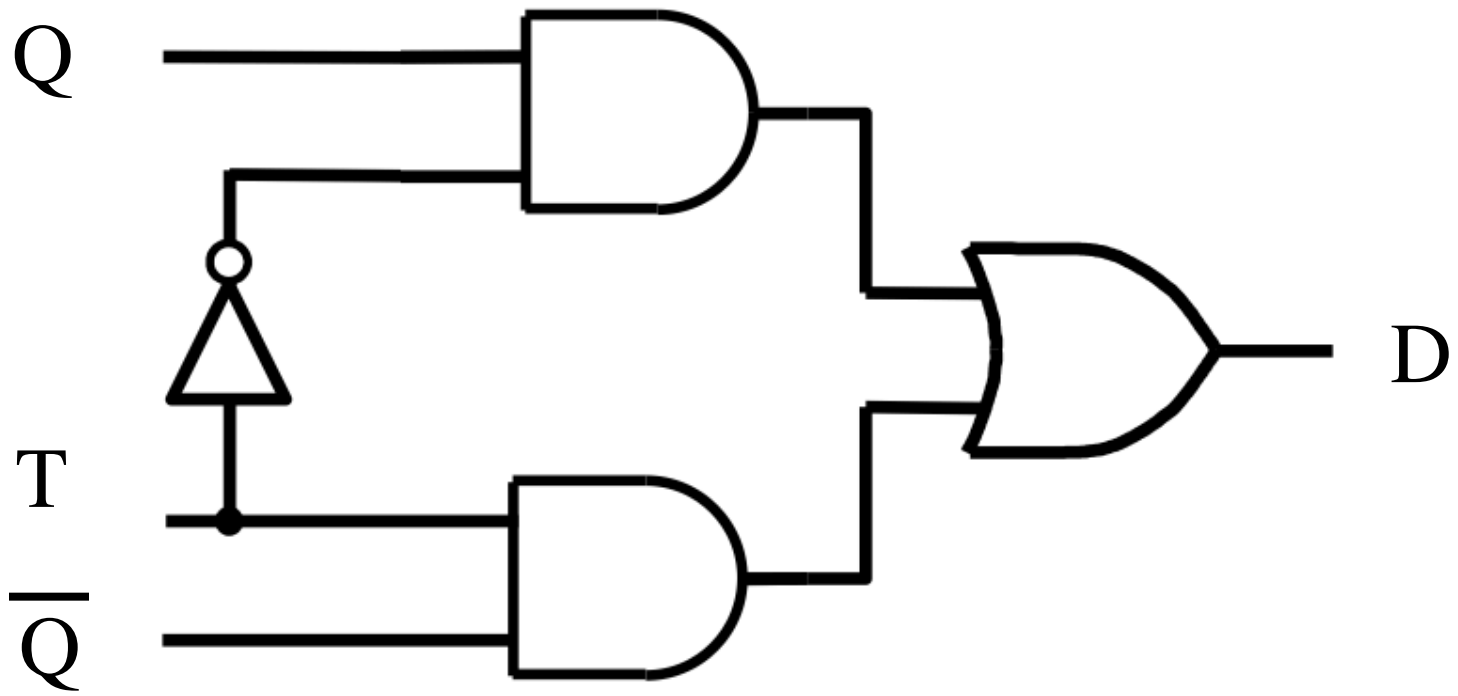
[Figure 5.15a from the textbook]

T Flip-Flop

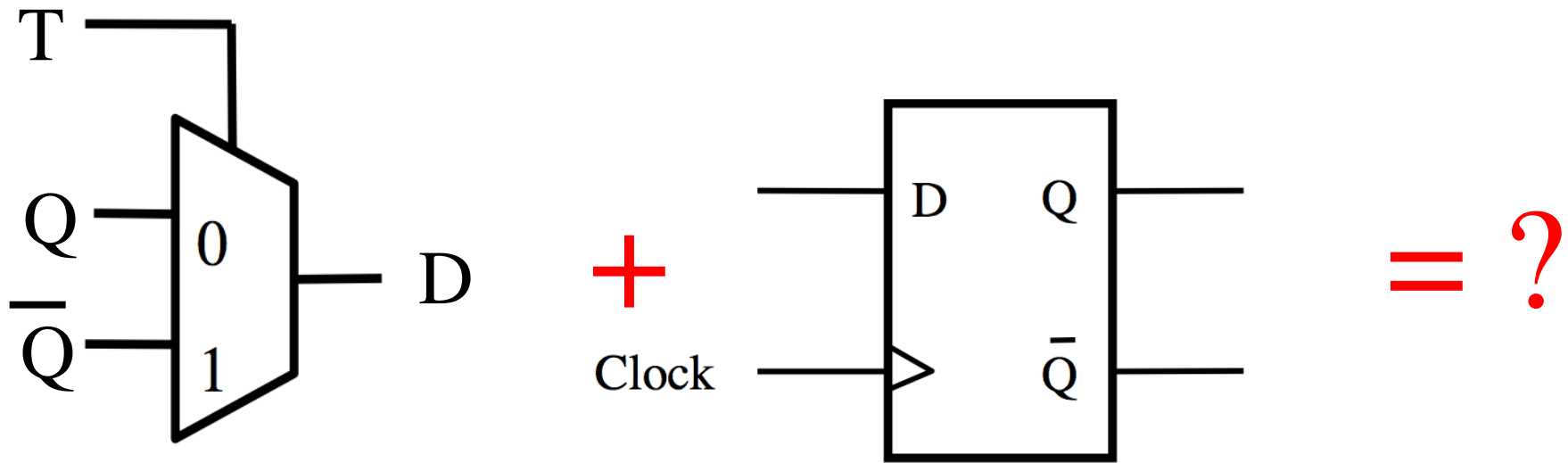


What is this?

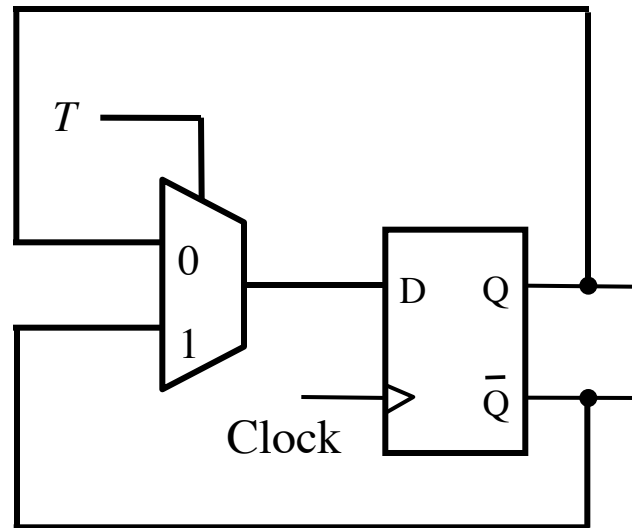
What is this?



What is this?



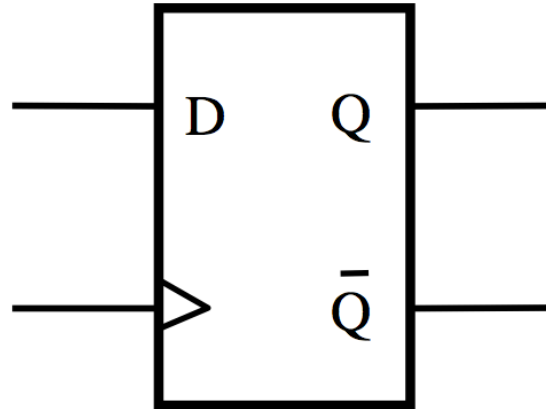
T Flip-Flop



What is this?

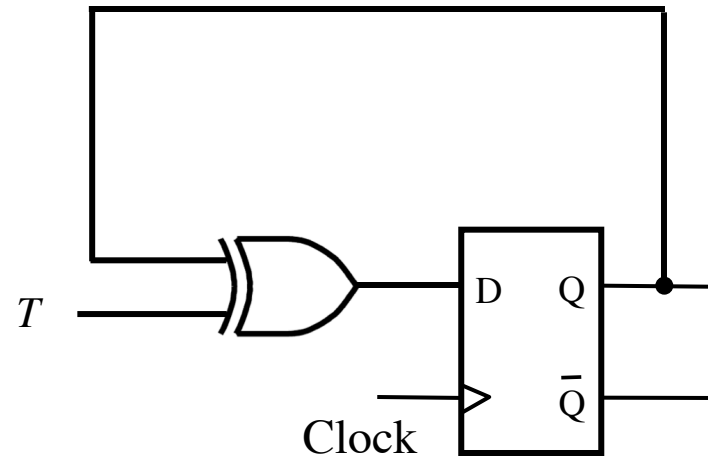


+
Clock



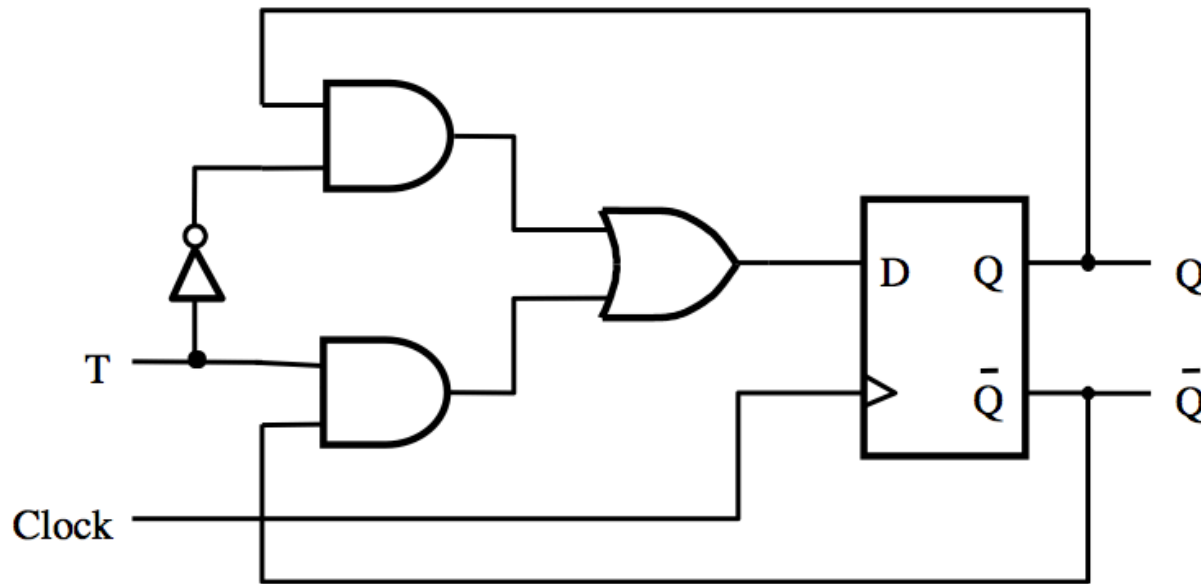
= ?

T Flip-Flop

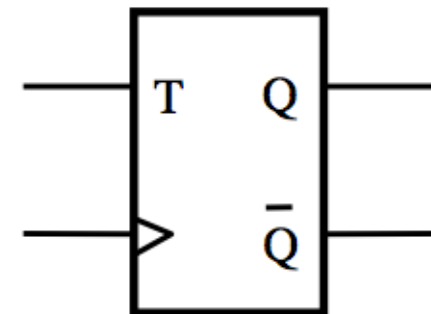


T Flip-Flop

(circuit, truth table and graphical symbol)



T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q(t)}$



[Figure 5.15a-c from the textbook]

T Flip-Flop (How it Works)

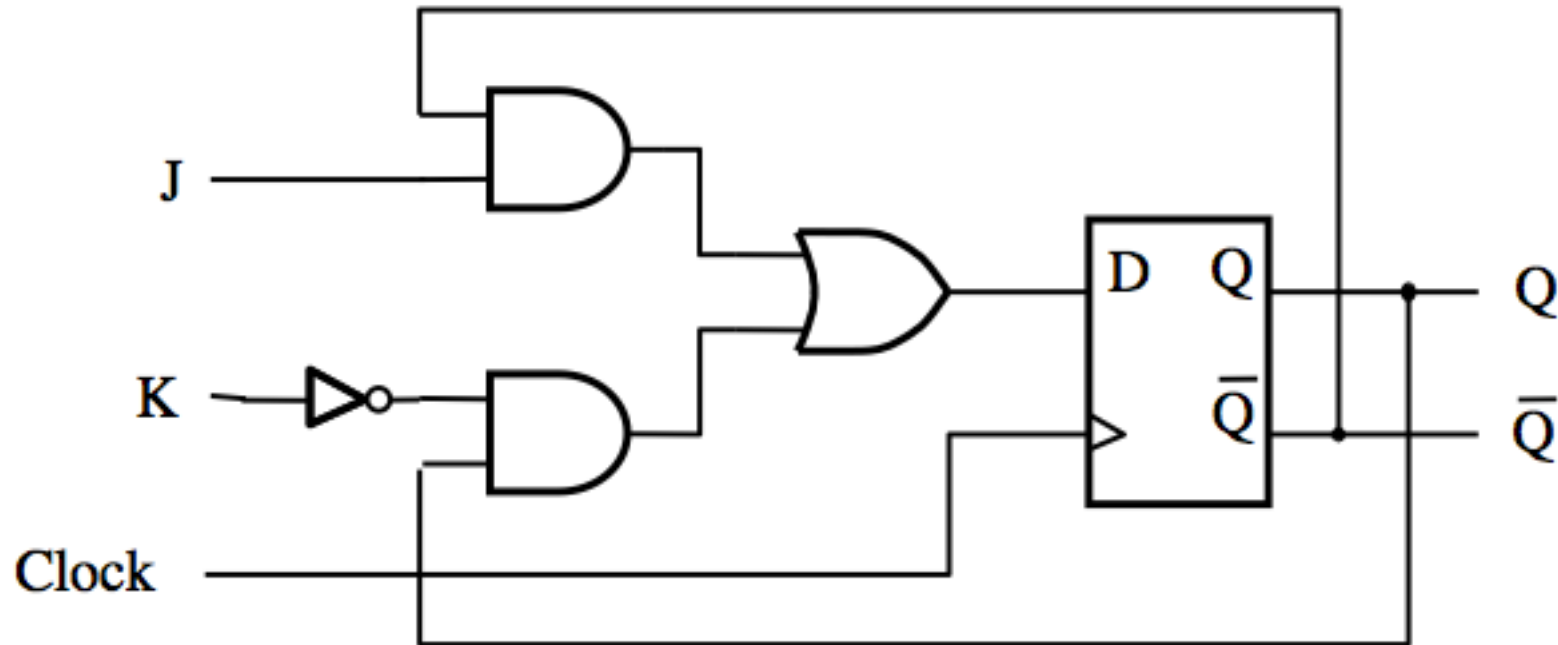
If $T=0$ then it stays in its current state

If $T=1$ then it reverses its current state

In other words the circuit “toggles” its state when $T=1$. This is why it is called T flip-flop.

JK Flip-Flop

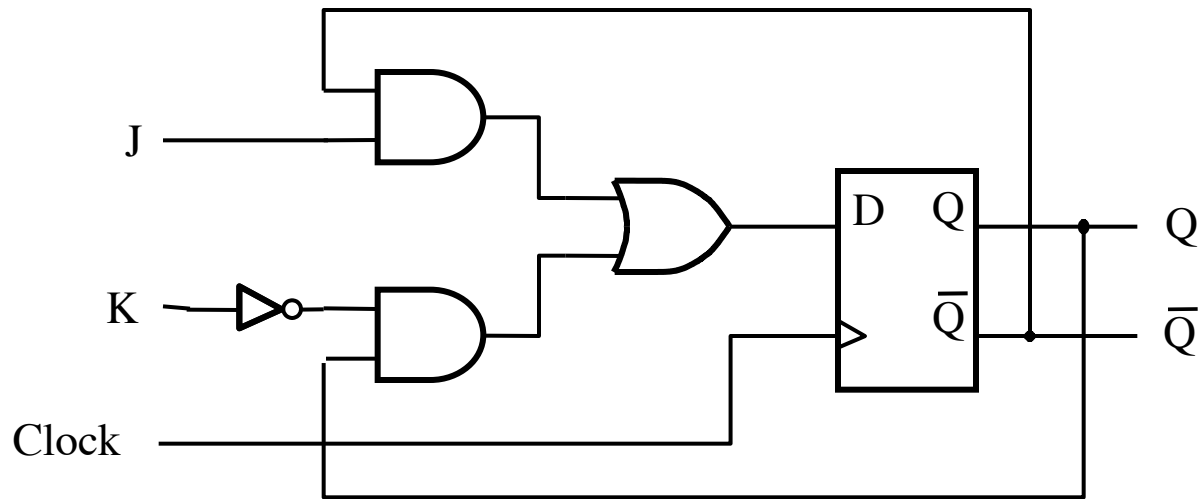
JK Flip-Flop



$$D = \overline{JQ} + \overline{KQ}$$

[Figure 5.16a from the textbook]

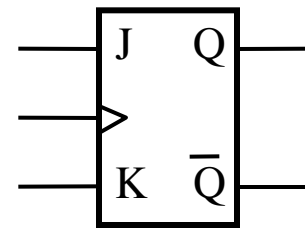
JK Flip-Flop



(a) Circuit

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

(b) Truth table



(c) Graphical symbol

JK Flip-Flop (How it Works)

A versatile circuit that can be used both as a SR flip-flop and as a T flip flop

If $J=0$ and $S=0$ it stays in the same state

Just like SR It can be set and reset

$J=S$ and $K=R$

If $J=K=1$ then it behaves as a T flip-flop

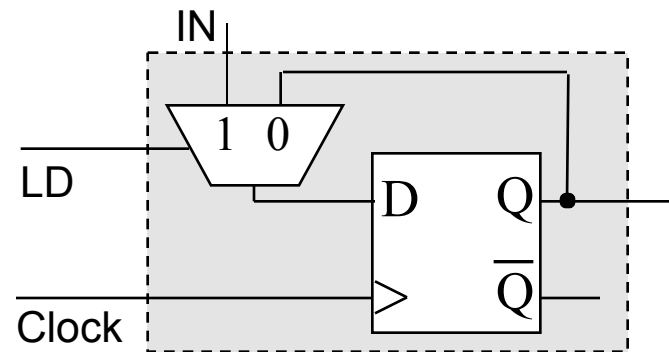
Registers

Register (Definition)

An n-bit structure consisting of flip-flops

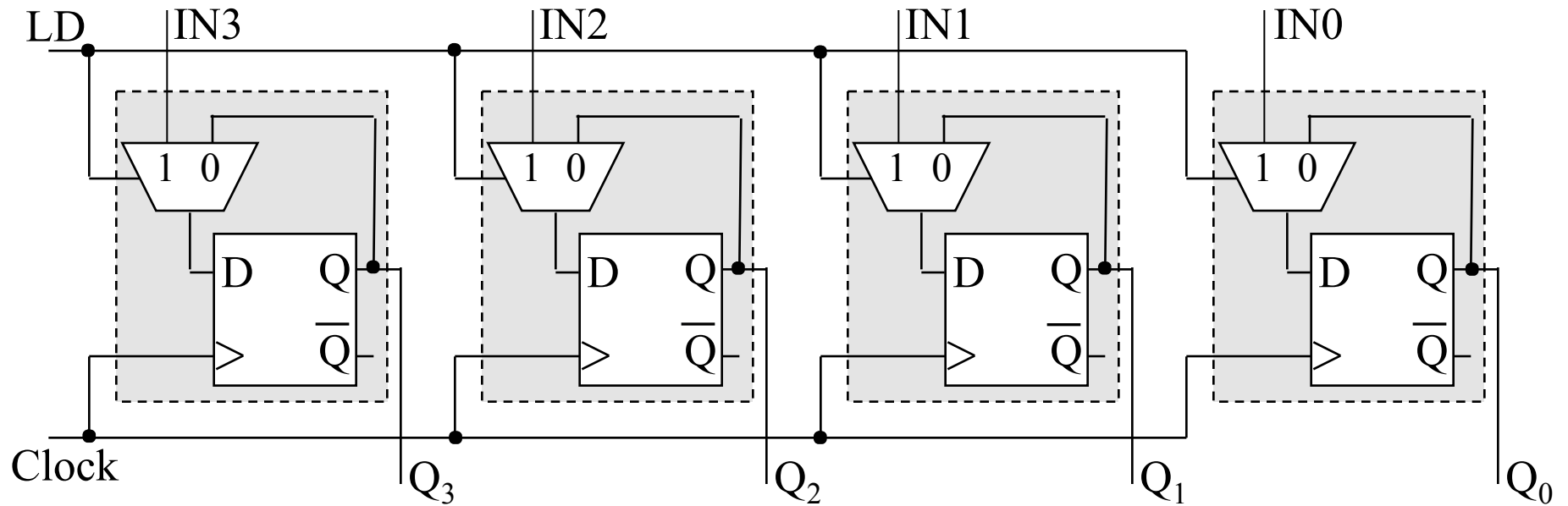
Parallel-Access Register

1-bit Parallel-access register



- **At the input of the D flip-flop, a 2-to-1 Multiplexer is used to select whether to load a new input value or to retain the old value**
- **If signal LD = 1 then load the new value**
- **If signal LD = 0 then retain the old value**

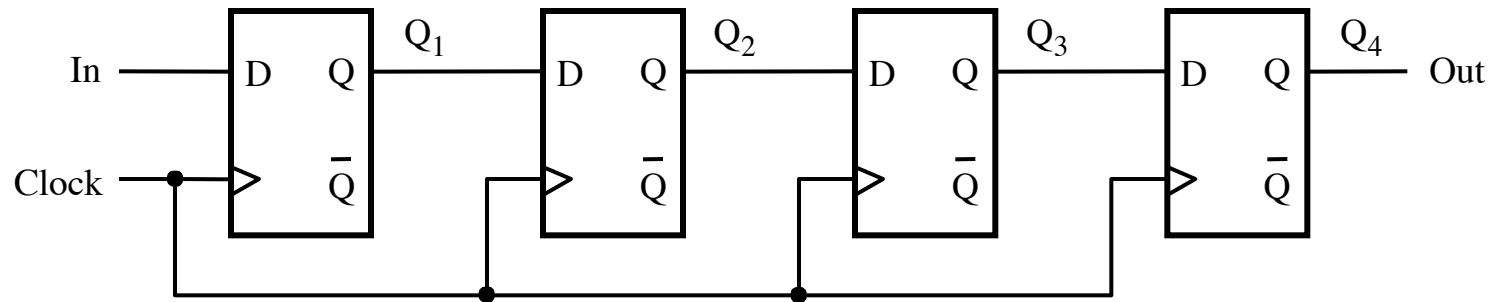
4-bit Parallel-access register



Notice that all flip-flops are on the same clock cycle.

Shift Register

A simple shift register



(a) Circuit

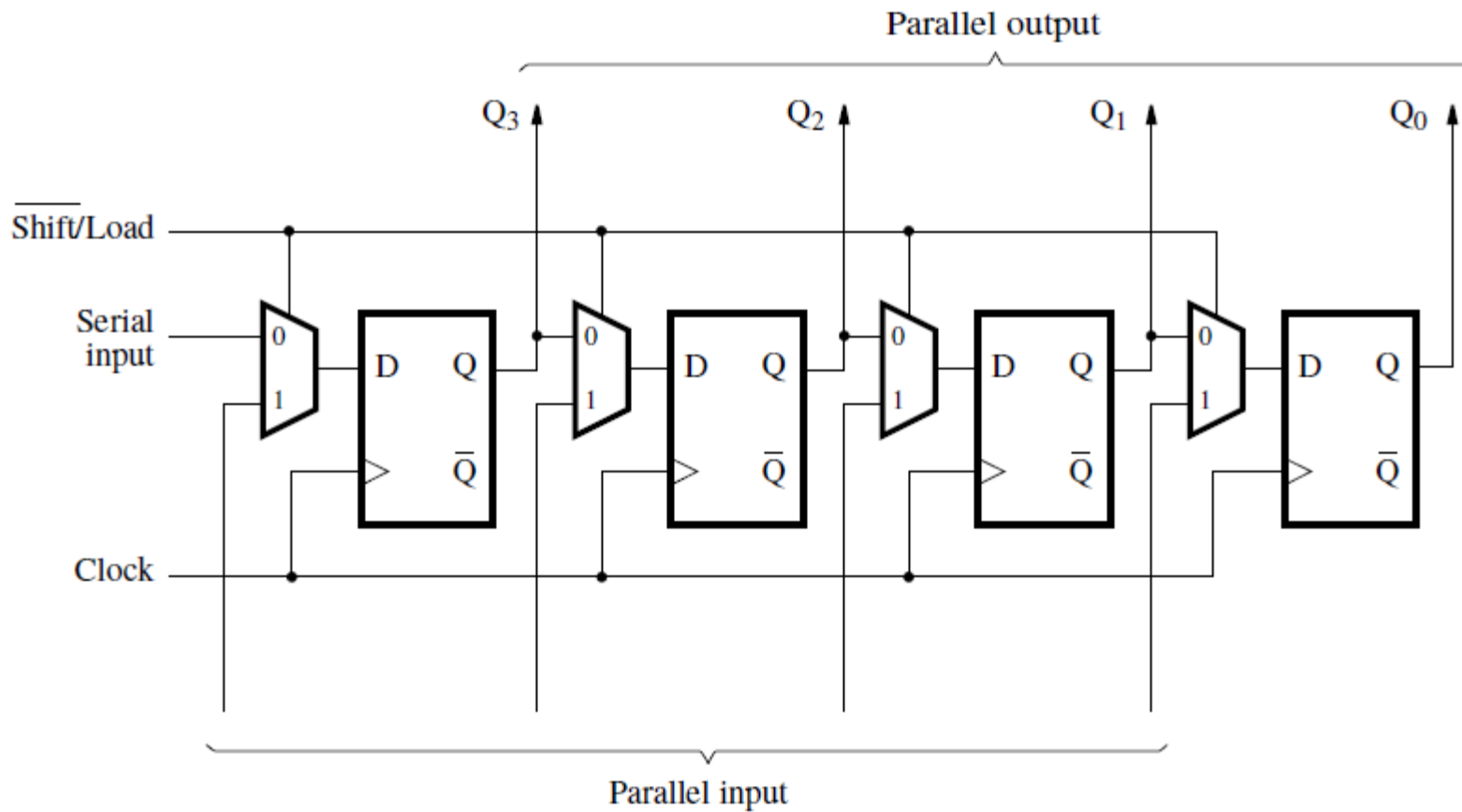
	In	Q ₁	Q ₂	Q ₃	Q ₄ = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

(b) A sample sequence

[Figure 5.17 from the textbook]

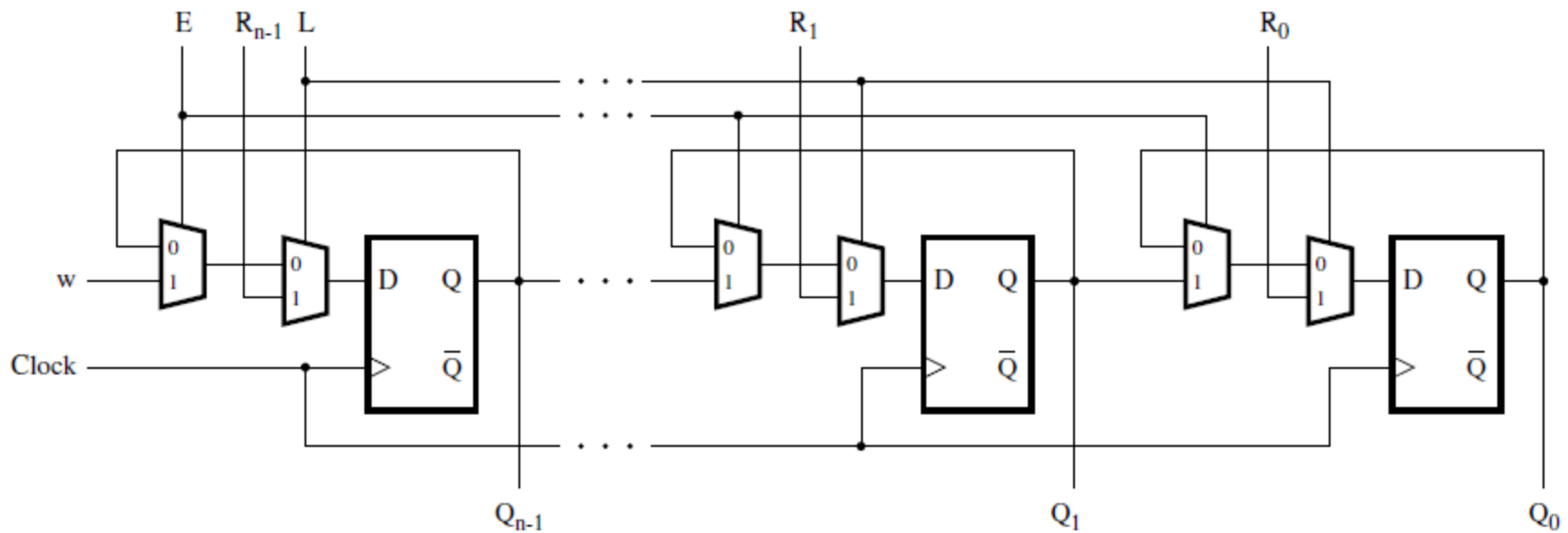
Parallel-Access Shift Register

Parallel-access shift register



[Figure 5.18 from the textbook]

A shift register with parallel load and enable control inputs

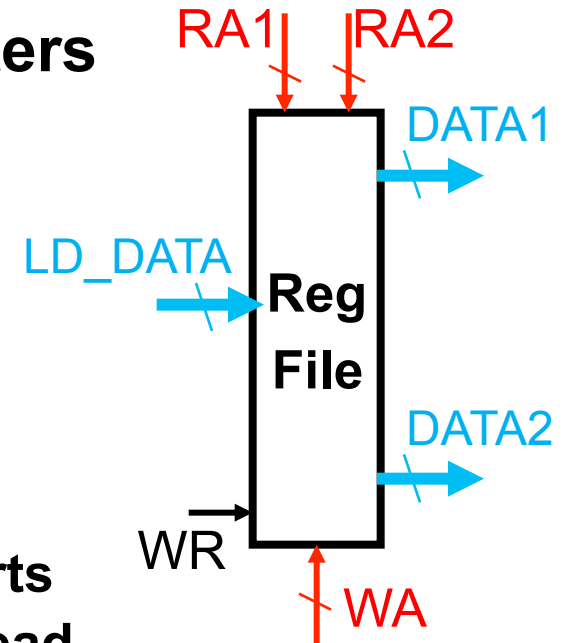


[Figure 5.59 from the textbook]

Register File

Register File

- **Register file is a unit containing r registers**
 - r can be 4, 8, 16, 32, etc.
- **Each register has n bits**
 - n can be 4, 8, 16, 32, etc.
 - n defines the data path width
- **Output ports (DATA1 and DATA2) are used for reading the register file**
 - Any register can be read from any of the ports
 - Each port needs a $\log_2 r$ bits to specify the read address (RA1 and RA2)
- **Input port (LD_DATA) is used for writing data to the register file**
 - Write address is also specified by $\log_2 r$ bits (WA)
 - Writing is enabled by a 1-bit signal (WR)

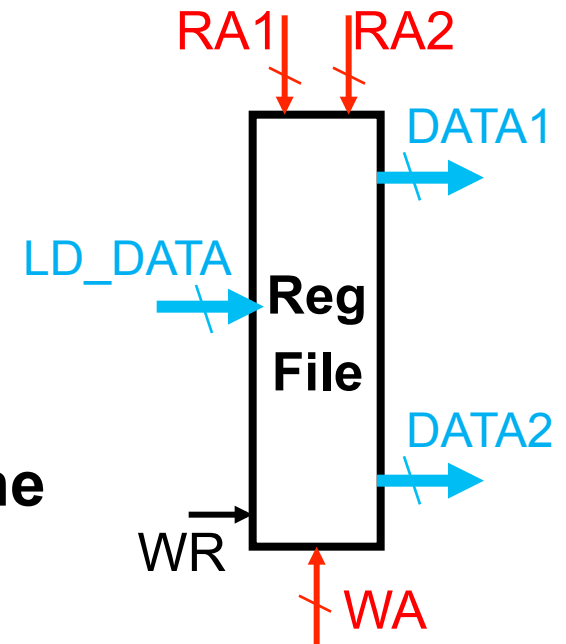


Register File: Exercise

- Suppose that a register file
 - contains 32 registers
 - width of data path is 16 bits (i.e., each register has 16 bits)

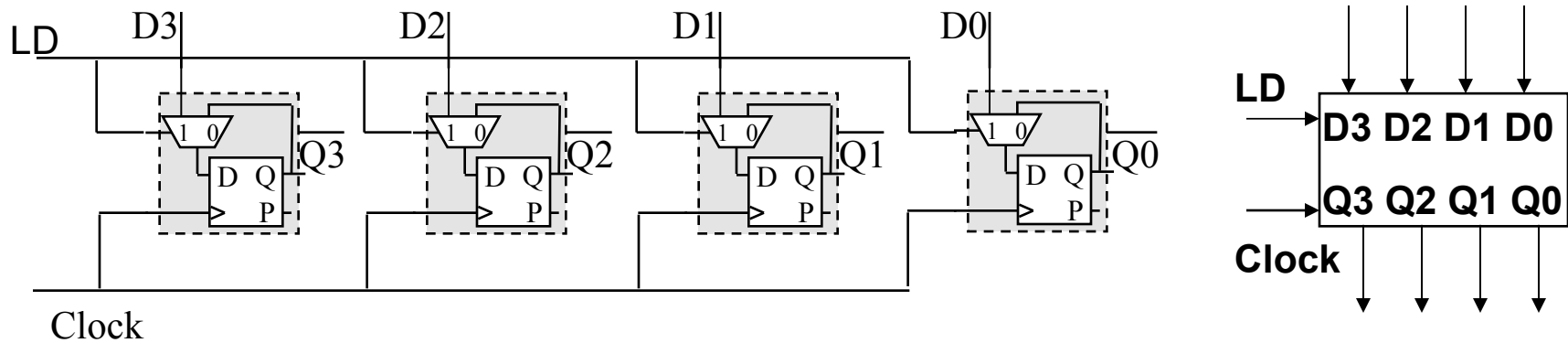
- How many bits are there for each of the signals?

- RA1 5
- RA2 5
- DATA1 16
- DATA2 16
- WA 5
- LD_DATA 16
- WR 1

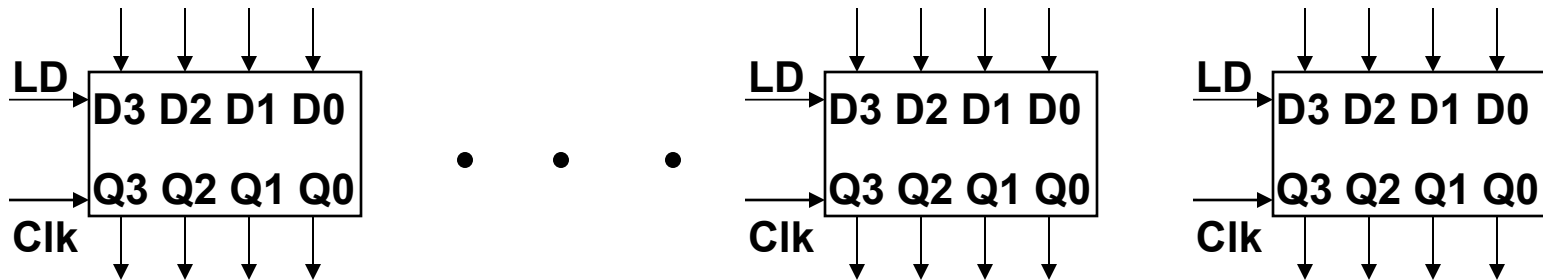


Register file design

- We will design an eight-register file with 4-bit wide registers
- A single 4-bit register and its abstraction are shown below



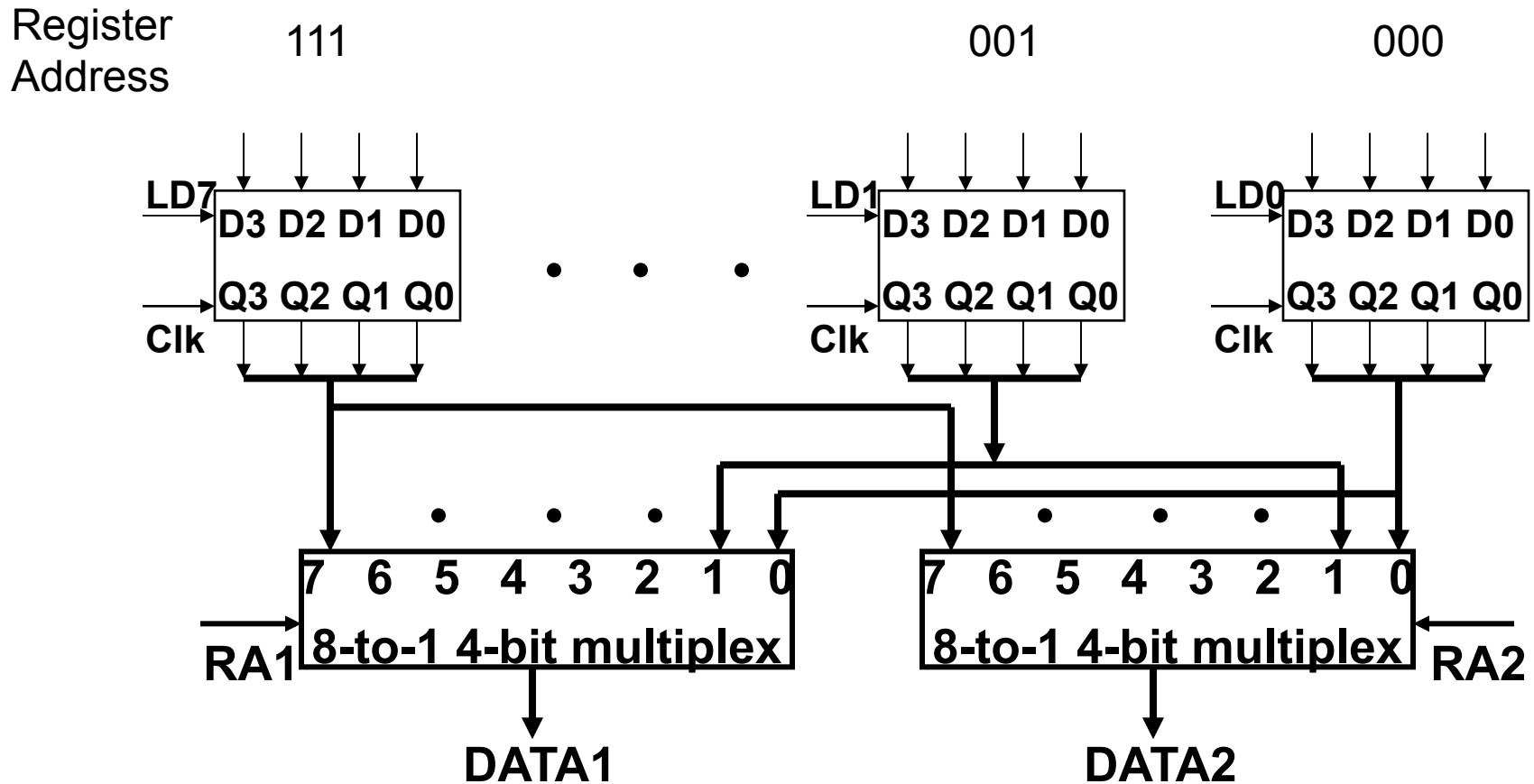
- We have to use eight such registers to make an eight register file



- How many bits are required to specify a register address?

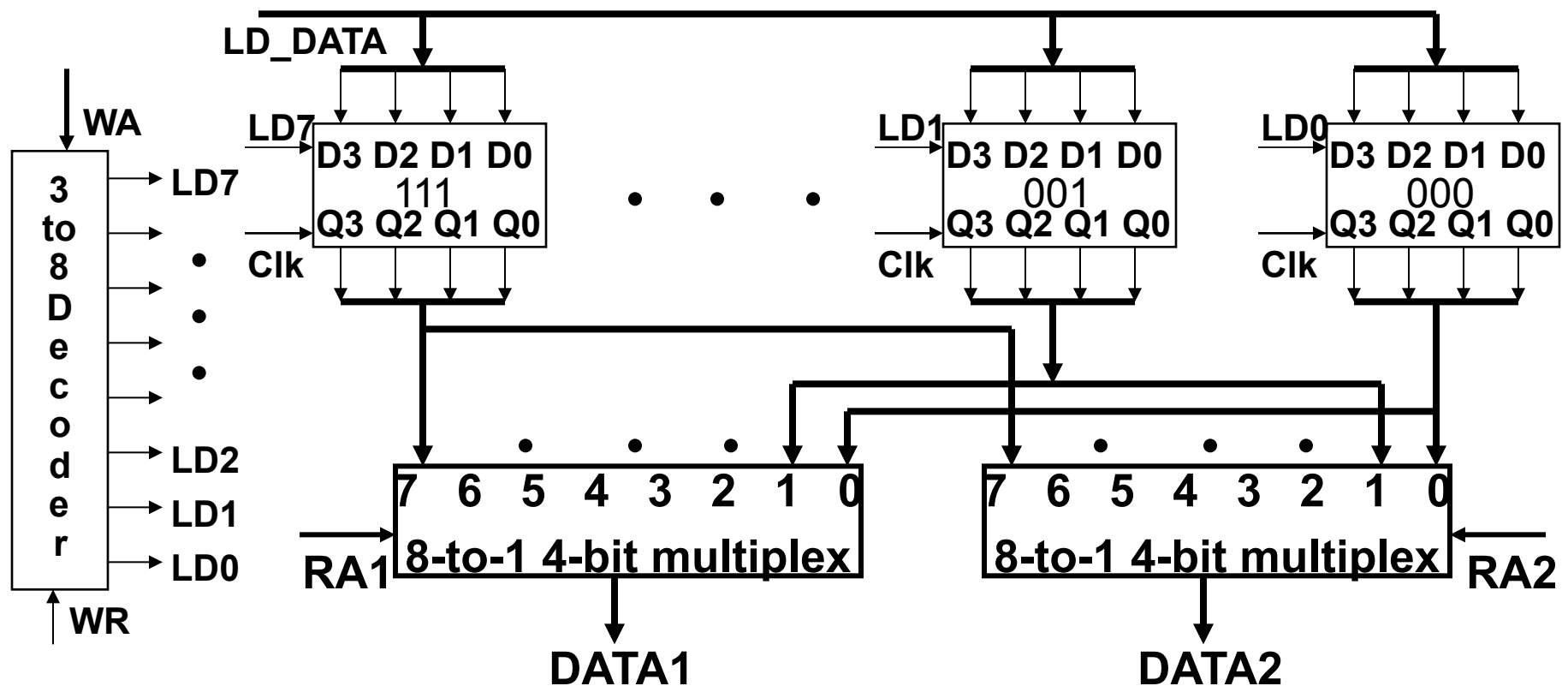
Reading Circuit

- A 3-bit register address, RA, specifies which register is to be read
- For each output port, we need one 8-to-1 4-bit multiplier



Adding write control to register file

- To write to any register, we need the register's address (WA) and a write register signal (WR)
- A 3-bit write address is decoded if write register signal is present
- One of the eight registers gets a LD signal from the decoder



Questions?

THE END