

In your answers, please clearly label the inputs and outputs of each multiplexer, decoder, encoder, and any other design block.

**P1. (10 points)**

Consider the following logic function:

$$F(A, B, C) = A'BC' + A'BC + AB'C + ABC$$

- (5 points) Show the Shannon's expansion of the function  $F$  using variable  $A$ .
- (5 points) Implement the circuit for function  $F$  using one 2-to-1 multiplexer and a minimal number of other logic gates.

**P2. (20 points)**

Consider the following truth table for the function  $f(a, b, c, d)$ .

$a$	$b$	$c$	$d$	$f$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

- (10 points) Implement  $f$  using one 4-to-16 decoder and a minimal number of gates.
- (10 points) Implement  $f$  using one 8-to-1 multiplexer and a minimal number of gates.

**P3. (10 points)**

Show how to construct a 4-to-16 decoder using five 2-to-4 decoders. Assume each 2-to-4 decoder has an ENABLE input (which enables each decoder).

**P4. (10 points)**

Implement the circuit for an 8-to-1 multiplexer using a 3-to-8 decoder and other necessary gates. The circuit should have control inputs  $s_2s_1s_0$ , data inputs  $w_7w_6w_5w_4w_3w_2w_1w_0$ , and an output  $f$ .

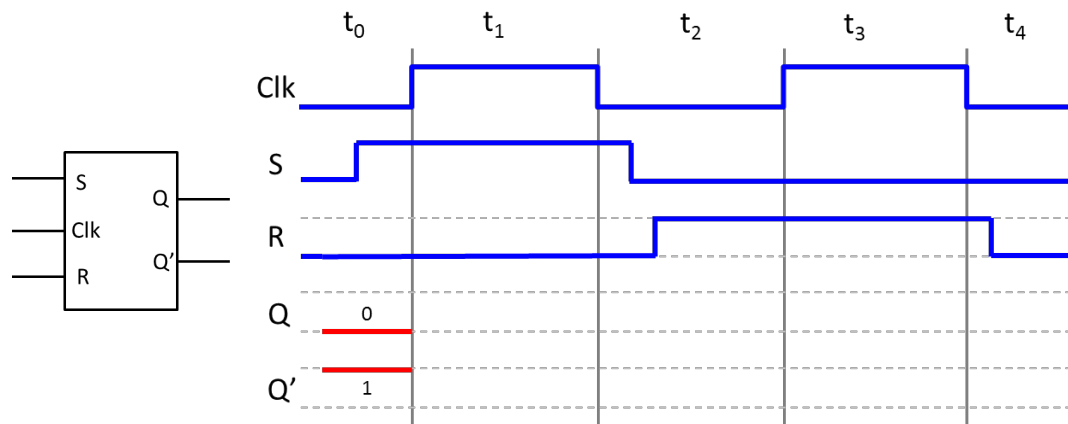
**P5. (20 points)**

Design a 4-to-2 priority encoder with the same inputs and outputs as in Figure 4.20 in the textbook, but with the following priority order:  $w_3 < w_2 < w_1 < w_0$

- (10 points) Show the truth table of this encoder.
- (10 points) Derive the minimal POS expression for  $y_1$ ,  $y_0$ , and  $z$ , respectively.

**P6. (10 points)**

Complete the following timing diagram for a gated SR-latch. Assume there's no gate delay.



**P7. (20 points)**

A full-adder (FA) has the following truth table:

$x$	$y$	$c_{in}$	$S$	$c_{out}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- (10 points) Implement the circuit for the output  $s$  by using one 4-to-1 multiplexer and a minimal number of gates.
- (10 points) Implement the circuit for the output  $c_{out}$  by using one 4-to-1 multiplexer. Please use  $x$  and  $y$  as control inputs  $s_1$  and  $s_0$  for the multiplexer.