Cpre 281 HW08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

## Flip-Flops, Registers, and Counters Assigned Date: Ninth Week

 Due Date: Wednesday, Oct. 24, 2016P1. (10 points)
Consider a basic SR latch with inputs $S, R$, and outputs $Q_{a}, Q_{b}$. (Figure 5.4 in the textbook)
a) (5 points) What would happen to $Q_{a}$ and $Q_{b}$ if $S=R=1$ ?
b) (5 points) What would happen to $Q_{a}$ and $Q_{b}$ if we transit from $S=R=1$ to $S=R=0$ ?

## P2. (15 points)

Complete the following timing diagram for $Q_{a}, Q_{b}$, and $Q_{c}$, which are the outputs of a gated D latch, a positive edge-triggered D flip-flop, and a negative edge-triggered D flip-flop. Assume $Q=0$ initially and no gate delays. (5 points each)


## P3. (10 points)

Complete the following timing diagram for a T flip-flop. Assume no gate delays.


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P4. (10 points)
The following truth table can be used to construct a T flip-flop using a D flip-flop.

| T | Output |  | D |
| :---: | :---: | :---: | :---: |
|  | $\mathrm{Q}(t)$ | $\mathrm{Q}(t+1)$ |  |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

a) (5 points) Write down the simplified SOP expression of D using T and $\mathrm{Q}(t)$ for inputs.
b) (5 points) Draw the circuit for a T flip-flop using a D flip-flop and other necessary gates. Make sure you connect the flip-flop to a clock signal.

## P5. (20 points)

Construct a JK flip-flop using a T flip-flop.
a) (10 points) Complete the following truth table.

| J | K | Output |  | T |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{Q}(t)$ | $\mathrm{Q}(t+1)$ |  |
| 0 | 0 | 0 |  |  |
| 0 | 0 | 1 |  |  |
| 0 | 1 | 0 |  |  |
| 0 | 1 | 1 |  |  |
| 1 | 0 | 0 |  |  |
| 1 | 0 | 1 |  |  |
| 1 | 1 | 0 |  |  |
| 1 | 1 | 1 |  |  |

b) (5 points) Write down the simplified SOP expression of T using J, K, and $\mathrm{Q}(t)$ for inputs.
c) (5 points) Draw the circuit for a JK flip-flop using a T flip-flop and other necessary gates.

Make sure that you connect the flip-flop to a clock signal.

## P6. (20 points)

Design a 4-bit shift register that has a control input $S$, a data input $X$, and output $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}$. When $S=0$, the register will shift left, i.e., the output becomes $\mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0} \mathrm{X}$. When $\mathrm{S}=1$, the register will shift right and the output becomes $\mathrm{XQ}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1}$. Draw a circuit for such a shift register using 4 D flip-flops and 4 2-to-1 multiplexers.

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P7. (15points)

a) (10 points) Complete the truth table for the circuit above.

| Input | $\mathrm{Q}(t)$ | J | K | $\mathrm{Q}(t+1)$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 |  |  |  |
| 0 | 1 |  |  |  |
| 1 | 0 |  |  |  |
| 1 | 1 |  |  |  |

b) (5 points) Based on the truth table, could you identify which flip-flop it is?

