Cpr E 281 HW 09
ELECTRICAL AND COMPUTER
ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Eleventh Week
Due Date: Monday, Nov. 7, 2016

P1. (15 points)
To construct a register file containing *eight* 16-bit registers, two input ports and three output ports, we use **w** number of 16-bit registers with parallel load input, **x** number of **y**-to-1 **z**-bit multiplexers, and **p** number of **q**-to-**r** decoders with enable. Specify the values of **w**, **x**, **y**, **z**, **p**, **q**, and **r**. (2 points for each variable)

P2. (10 points)
What is the counting sequence of the following counter?
Assume the counter starts from $Q_2Q_1Q_0 = 000$.
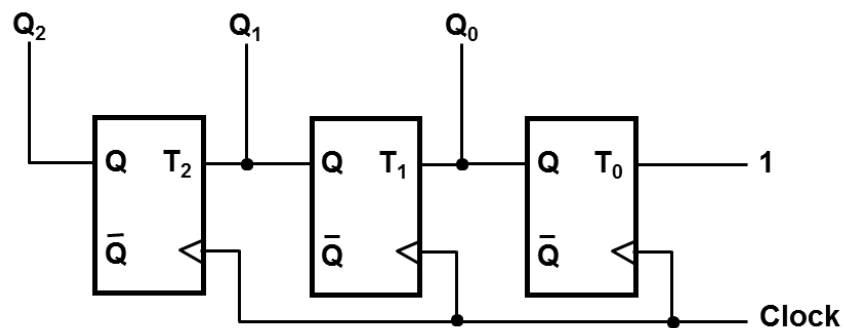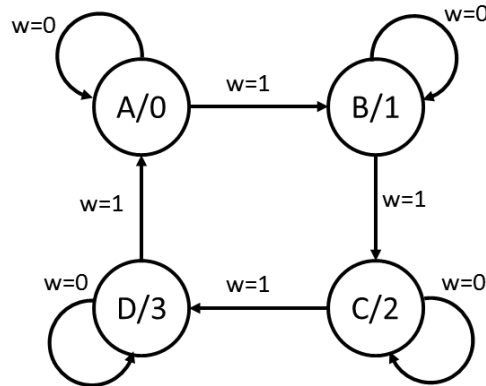

P3. (20 points)
Answer the following questions:
  a) (5 points) Draw a circuit for a 4-bit asynchronous up-counter using T flip-flops.
  b) (5 points) Draw a circuit for a 4-bit synchronous up-counter using T flip-flops.
  c) (5 points) Let $Q_n \ldots Q_2Q_1Q_0$ be the bits that represent the count value of an asynchronous counter. What could happen if n is increased?
  d) (5 points) Could you think of one possible reason that a designer may choose to implement an asynchronous counter over a synchronous counter?

P4. (10 points)
Figure 5.25 in textbook shows the design of a modulo-6 counter with reset synchronization. Modify the circuit and make it a modulo-5 counter instead?

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P5. (25 points) Consider a FSM with the following state diagram:

a) (5 points) Complete the following state table based on the state diagram:

Present State	Next State $w=0$	Next State $w=1$	Output
A	A	B	0
B			
C			
D			

b) (5 points) Encode each state and outputs in (a) with binary numbers to build the following state-assigned table:

Present State $y_1 y_0$	Next State $w=0$ $Y_1 Y_0$	Next State $w=1$ $Y_1 Y_0$	Output $z_1 z_0$

c) (5 points) Derive the minimal logic expressions for Y_1, Y_0, z_1, and z_0.

d) (5 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required.

e) (5 points) What does this FSM do? What happens when $w=0$ and $w=1$?

P6. (20 points)

Design a 2-bit counter controlled by an input w. When $w=0$, it acts as a down-counter. When $w=1$, it acts as an up-counter. The output shows the current value of counter.

a) (5 points) Draw the state diagram for this counter.

b) (5 points) Derive the state-assigned table for this counter. Each state and output should be encoded with binary numbers.

c) (5 points) Derive the minimal logic expressions for Y_1, Y_0, z_1, and z_0.

d) (5 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required.

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