Cpr E 281 HW 10

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Twelfth Week
Due Date: Monday, Nov. 14, 2016

P1. (10 points)
Briefly explain the major difference between a Moore state machine and a Mealy state machine.

P2. (25 points)
A FSM with an input w and an output z has the following state table.

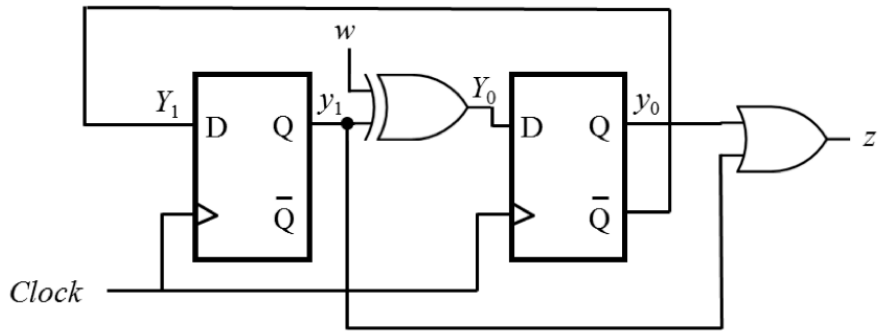
Present State	Next State		Output z	
	w=0	w=1	w=0	w=1
A	A	B	0	1
B	C	B	1	0
C	B	A	0	0

a) (5 points) Draw the state diagram based on the state table.
b) (5 points) Complete the state-assigned table based on the state table.

	Present State	Next State		Output z	
		w=0	w=1	w=0	w=1
	y_1y_0	Y_1Y_0	Y_1Y_0	z	z
A	0 0				
B	0 1				
C	1 0				

c) (5 points) Find the simplified SOP expressions for Y_1, Y_0, and z.
d) (5 points) Draw the circuit diagram using D flip-flops and any other required gates.
e) (5 points) Is this a Moore machine or a Mealy machine? Why?

P3. (15 points)
A FSM has two D flip-flops, an input w, and an output z. The circuit diagram is shown below.



a) (5 points) Find the logic expressions of Y_1, Y_0, and the output z.
b) (5 points) Show the state-assigned table of the FSM.
c) (5 points) Draw the state diagram of the FSM.

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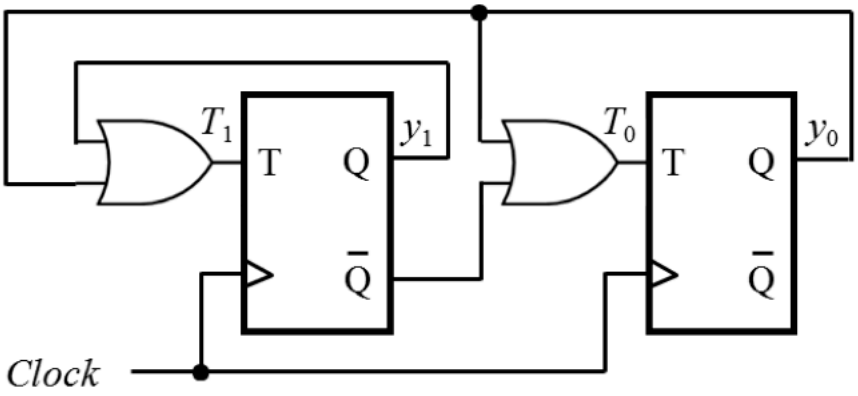
P4. (10 points)
A two-bit counter has the following circuit diagram. The output is $z_1z_0 = y_1y_0$.



a) (5 points) Draw the state diagram of the counter.
b) (5 points) What is the repeated counting sequence of this counter?

P5. (30 points)
Consider the following state table for a FSM.

Present State	Next State		Output
	w=0	w=1	z
A	A	B	0
B	B	C	1
C	C	D	0
D	D	A	1

a) (5 points) Draw the state diagram of the FSM.
b) (5 points) Draw the circuit diagram of FSM using D flip-flops.
c) (5 points) Perform state minimization to minimize the number of states. Show your partitions in the procedure.
d) (5 points) Draw the new state diagram of the minimized FSM.
e) (5 points) Draw the circuit diagram of the minimized FSM using D flip-flops.
f) (5 points) Compare the circuits in (b) and (e), what is the benefit of state minimization?

P6. (10 points)
Bob needs to use a 3-bit up-counter. However, he only has a 4-bit synchronous down-counter and several NOT gates. He is NOT allowed to modify the internal structure of the down-counter. How can he construct the 3-bit up-counter using only the devices that he has?