

**In problems P1-P5, your answers should include at least the following: the state-assigned table, logic expressions for the next state and for the output, and the circuit diagram.**

**P1. (10 points)**

Design a modulo-5 counter that counts in the sequence 0, 1, 2, 3, 4, 0, 1, 2, 3, 4... when the input  $w=1$ , and stops counting when  $w=0$ . Use D flip-flops in your circuit.

**P2. (10 points)**

Repeat P1 using T flip-flops.

**P3. (10 points)**

Repeat P1 using JK flip-flops.

**P4. (10 points)**

Design a modulo-12 up-counter that counts in the sequence 0, 1, 2, 3, ..., 9, 10, 11, 0.... with input  $w$  as an enable. Use JK flip-flops in your circuit.

**P5. (40 points)**

A counter has a special counting sequence: 0, 5, 7, 1, 0, 5, 7, 1, and so on. Design this counter with minimal number of states.

- (5 points) Draw a state diagram for the counter.
- (5 points) Construct a state-assigned table including the next state and output.
- (10 points) Draw the circuit diagram for the counter using D flip-flops.
- (10 points) Repeat (c) using T flip-flops.
- (10 points) Repeat (c) using JK flip-flops.

**P6. (10 points)**

Draw a state transition diagram for:

- (5 points) A state machine that reads in a sequence of binary digits, one at a time, and stops when it has read in a total of five 1s (need not to be consecutive). To “stop” the machine, merely have it loop repeatedly in a final state.
- (5 points) A state machine that stops when it has read in at least three consecutive 1s followed by a 0.

**P7. (10 points) Arbiter Circuits**

The arbiter FSM defined in Section 6.8 (Figure 6.72) may cause device 3 to never get serviced if devices 1 and 2 continuously keep raising requests, so that in the *Idle* state it always happens that either device 1 or device 2 has an outstanding request. Modify the proposed FSM to ensure that device 3 will get serviced, such that if it raises a request, then device 1 and 2 will be serviced only once before device 3 is granted its request.