

CprE 281: Digital Logic

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<http://www.ece.iastate.edu/~alexs/classes/>

T Flip-Flops & JK Flip-Flops

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Iowa State University, Ames, IA
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Administrative Stuff

- **Homework 8 is due next Monday.**
- **The second midterm exam is next Friday.**

Administrative Stuff

- **Midterm Exam #2**
- **When: Friday October 28 @ 4pm.**
- **Where: This classroom**
- **What: Chapters 1, 2, 3, 4 and 5.1-5.8**
- **The exam will be open book and open notes (you can bring up to 3 pages of handwritten notes).**

Midterm 2: Format

- The exam will be out of 130 points
- You need 95 points to get an A
- It will be great if you can score more than 100 points.
 - but you can't roll over your extra points ☹️

Midterm 2: Topics

- **Binary Numbers and Hexadecimal Numbers**
- **1's complement and 2's complement representation**
- **Addition and subtraction of binary numbers**
- **Circuits for adders and fast adders**

- **Single and Double precision IEEE floating point formats**
- **Converting a real number to the IEEE format**
- **Converting a floating point number to base 10**

- **Multiplexers (circuits and function)**
- **Synthesis of logic functions using multiplexers**
- **Shannon's Expansion Theorem**

Midterm 2: Topics

- **Decoders (circuits and function)**
- **Demultiplexers**
- **Encoders (binary and priority)**
- **Code Converters**
- **K-maps for 2, 3, and 4 variables**

- **Synthesis of logic circuits using adders, multiplexers, encoders, decoders, and basic logic gates**
- **Synthesis of logic circuits given constraints on the available building blocks that you can use**

- **Latches (circuits, behavior, timing diagrams)**
- **Flip-Flops (circuits, behavior, timing diagrams)**
- **Registers and Register Files**

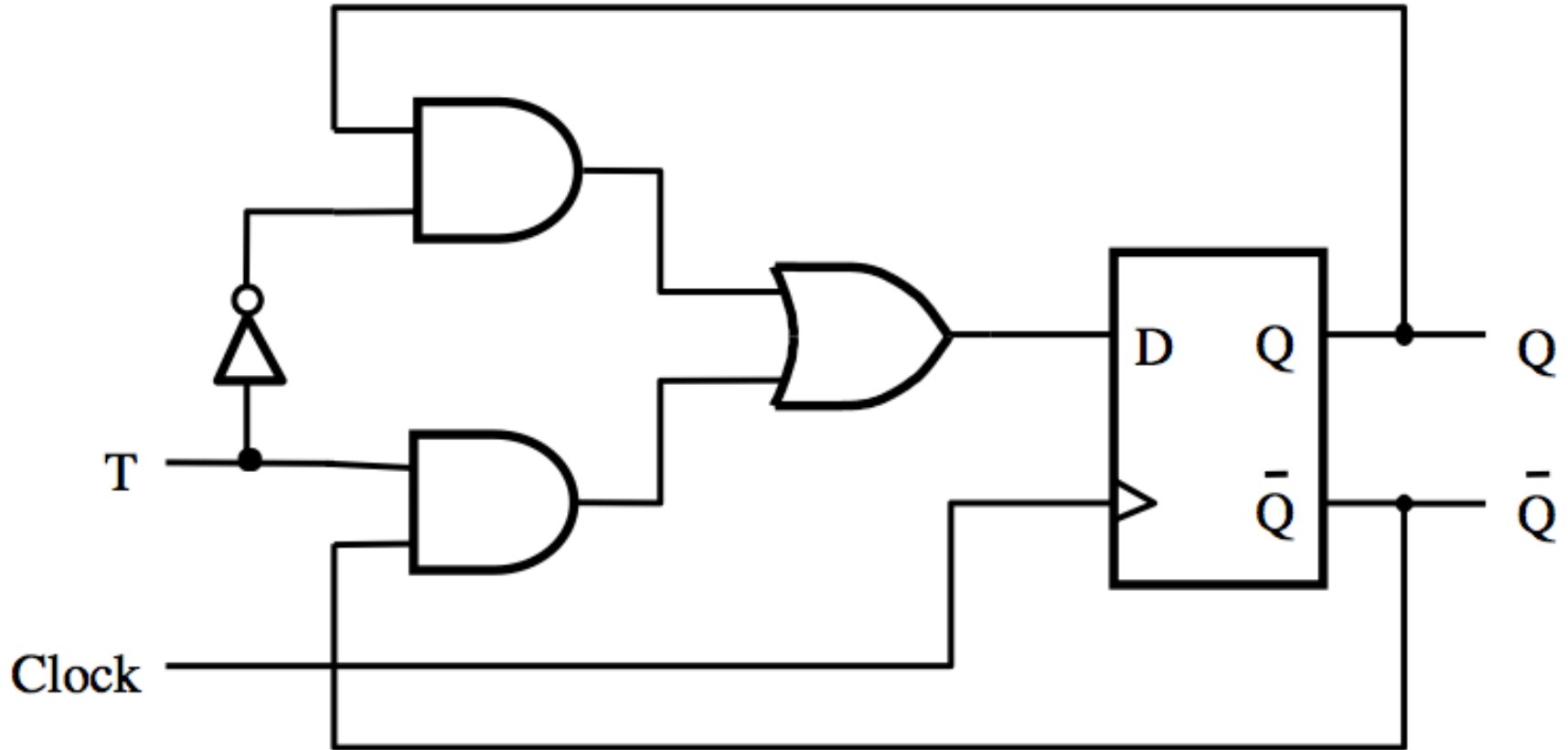
T Flip-Flop

Motivation

A slight modification of the D flip-flop that can be used for some nice applications.

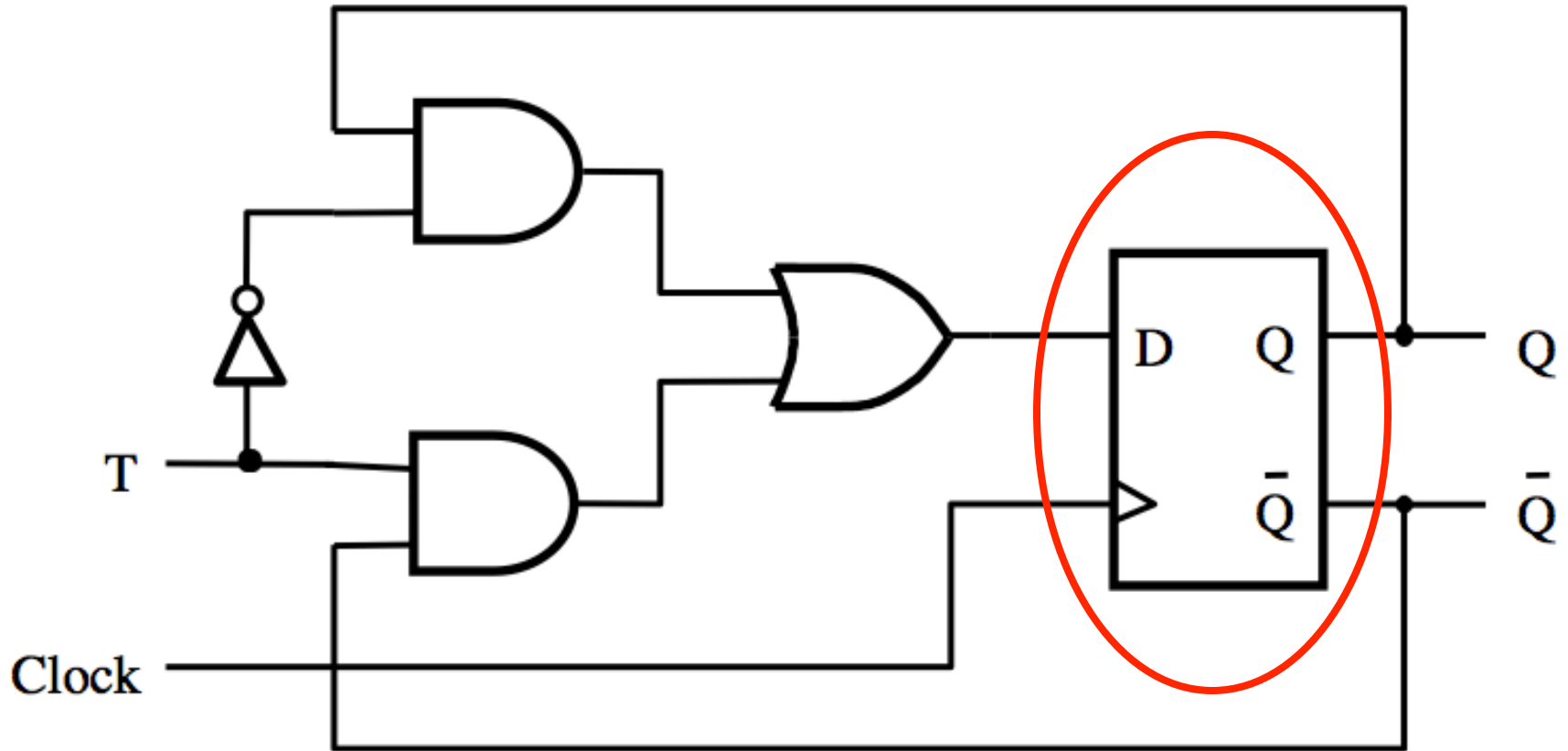
In this case, T stands for Toggle.

T Flip-Flop



[Figure 5.15a from the textbook]

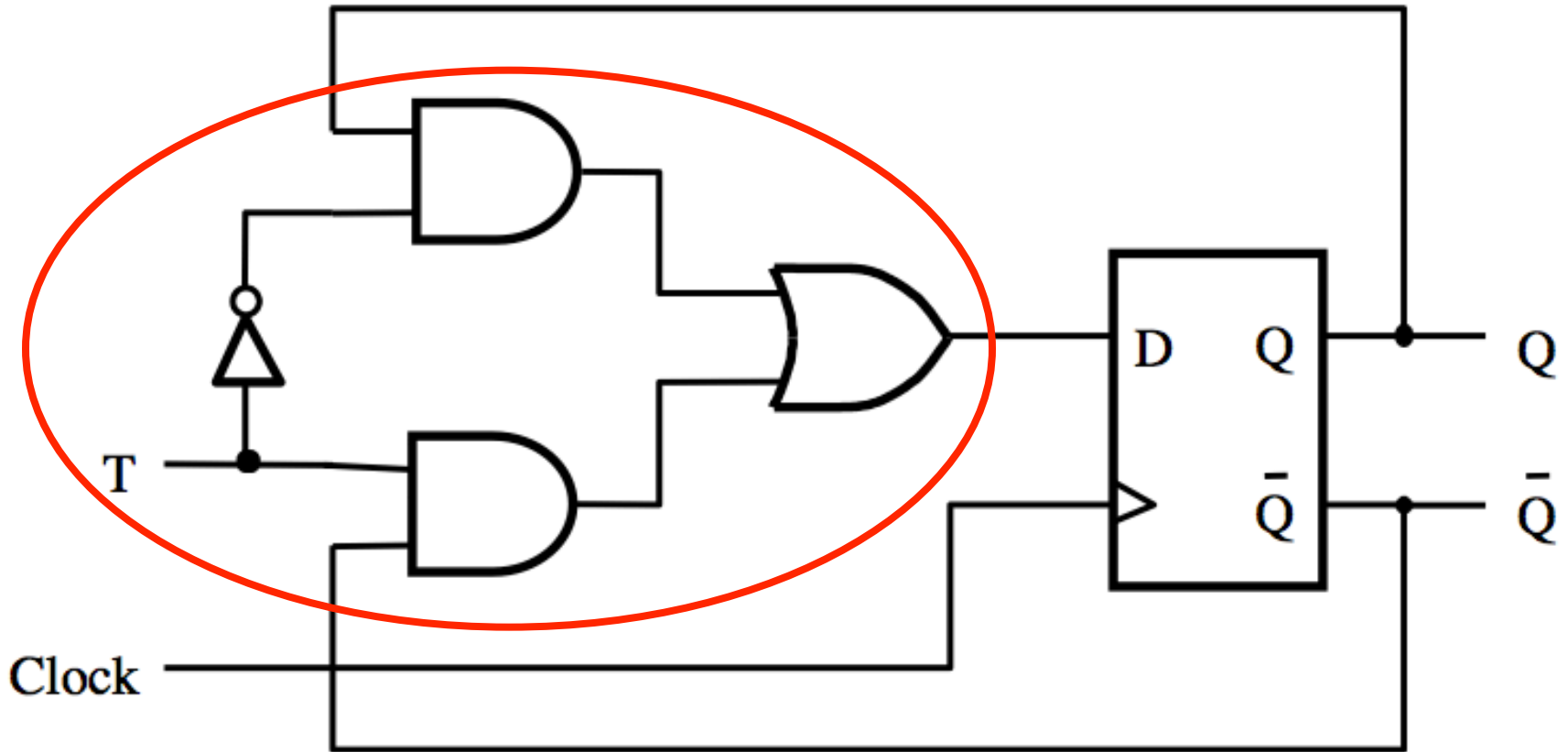
T Flip-Flop



Positive-edge-triggered
D Flip-Flop

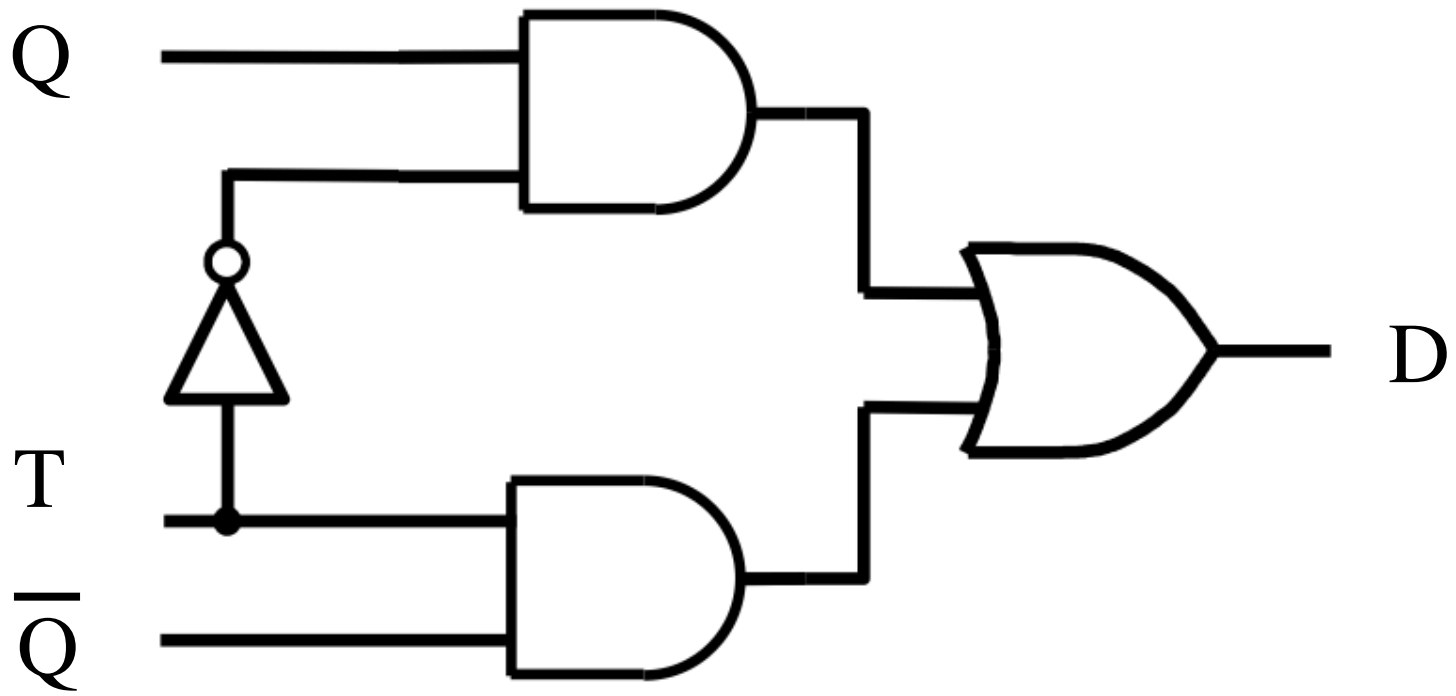
[Figure 5.15a from the textbook]

T Flip-Flop

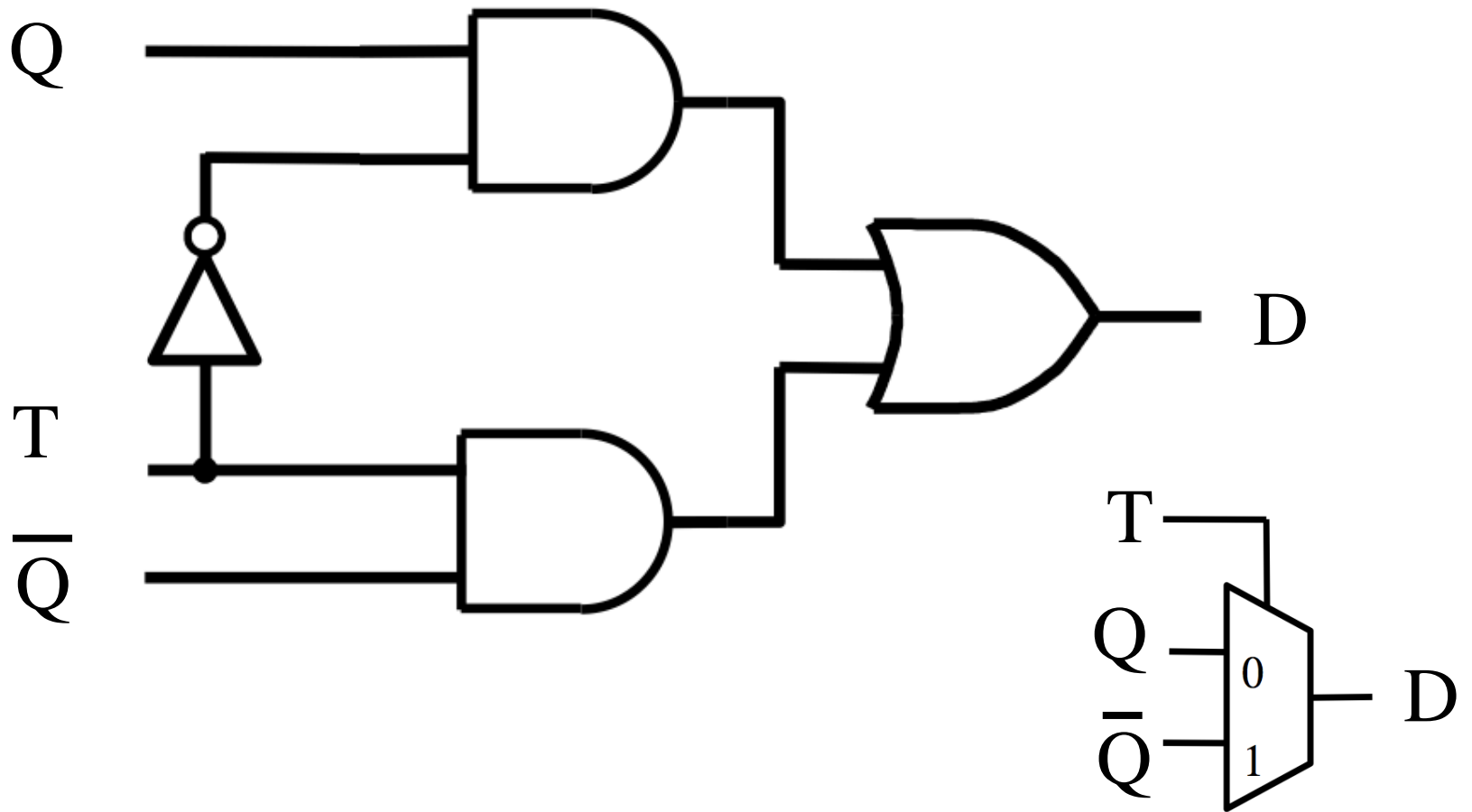


What is this?

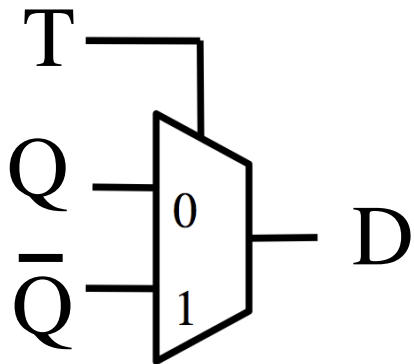
What is this?



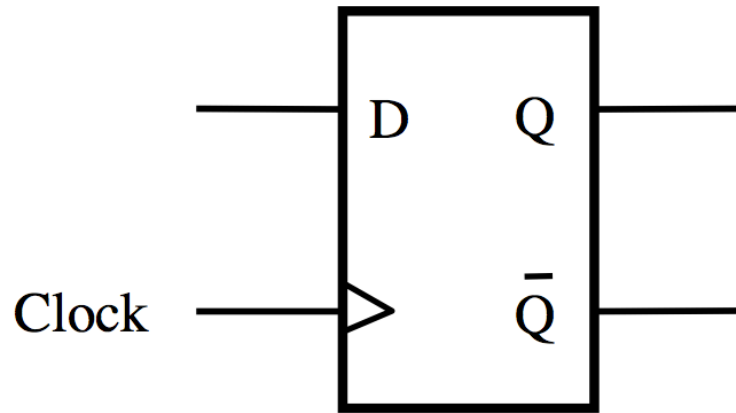
It is a 2-to-1 Multiplexer



What is this?

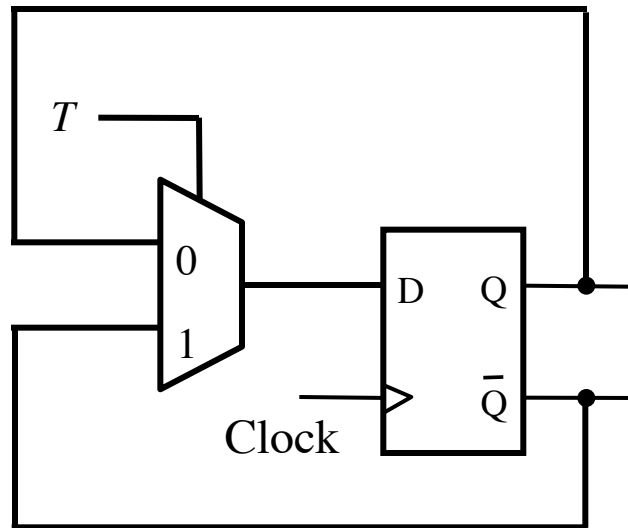


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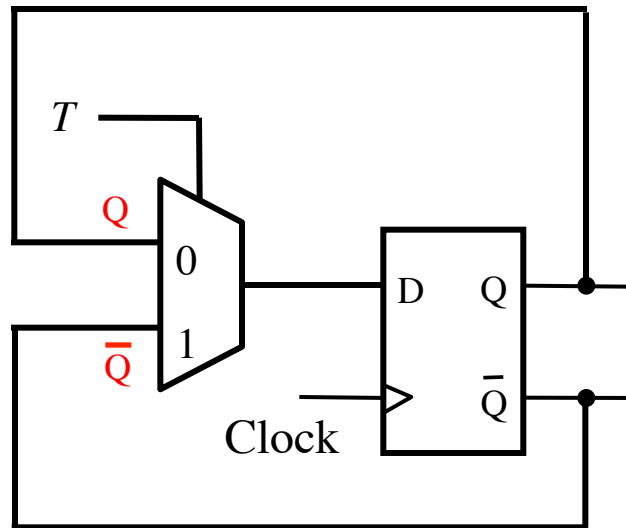


= ?

It is a T Flip-Flop

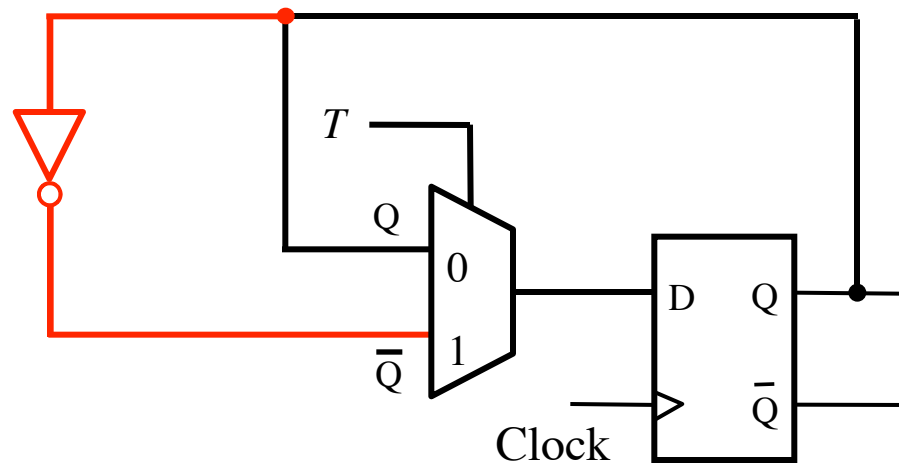


It is a T Flip-Flop

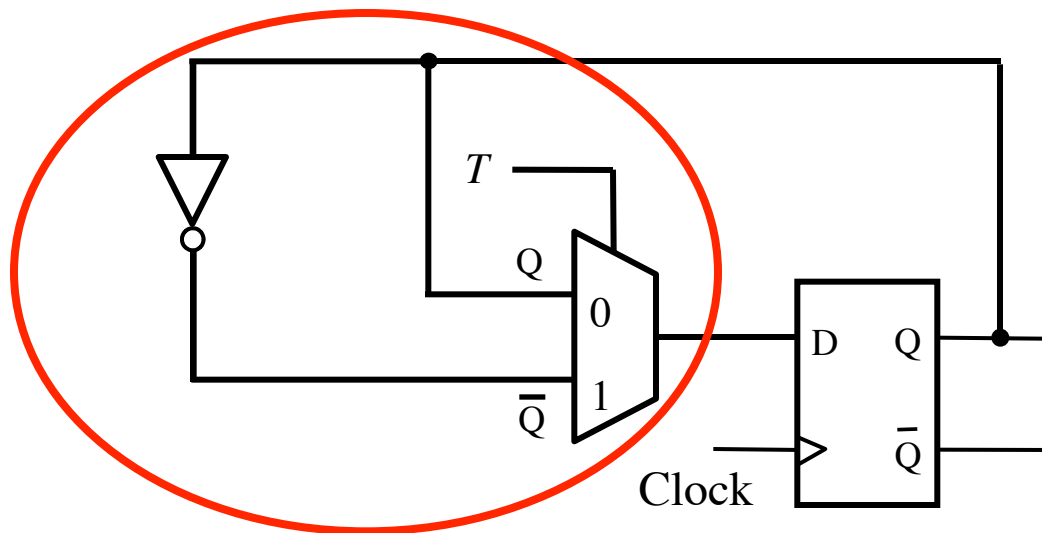


Note that the two inputs to the multiplexer are inverses of each other.

Another Way to Draw This

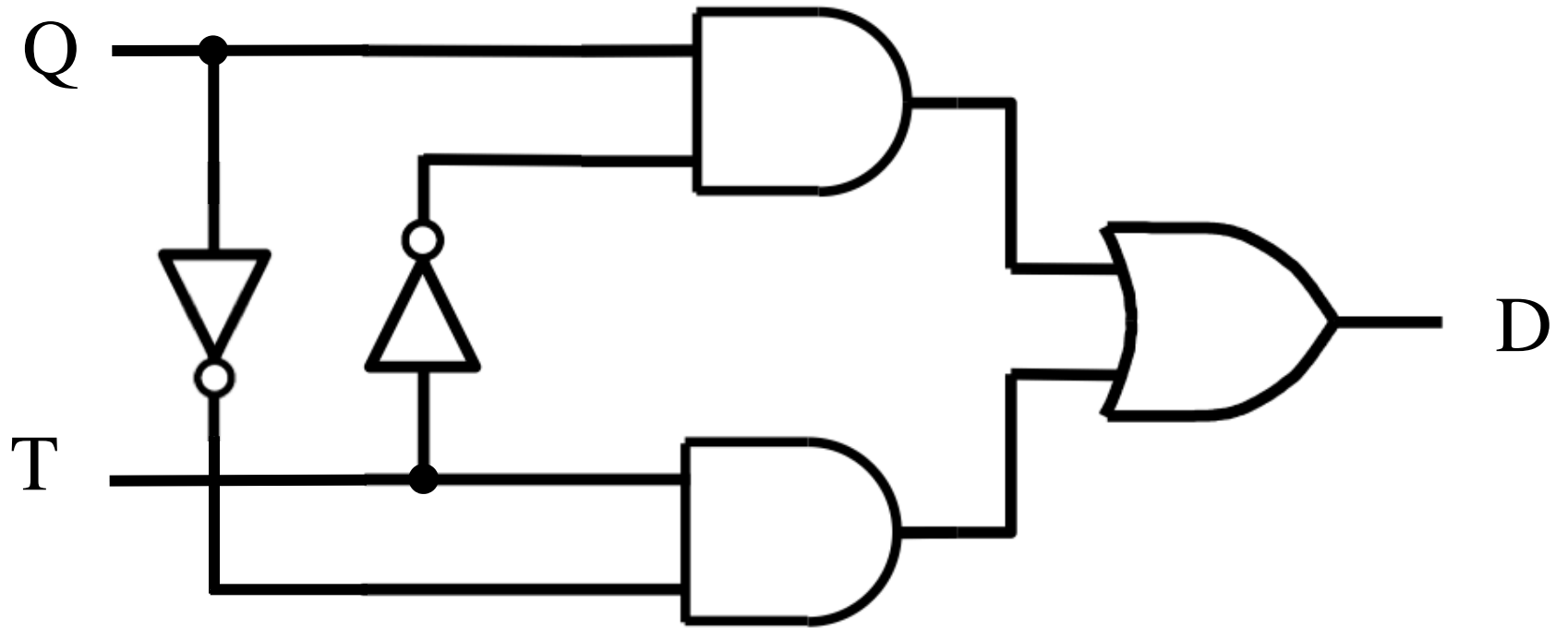


Another Way to Draw This

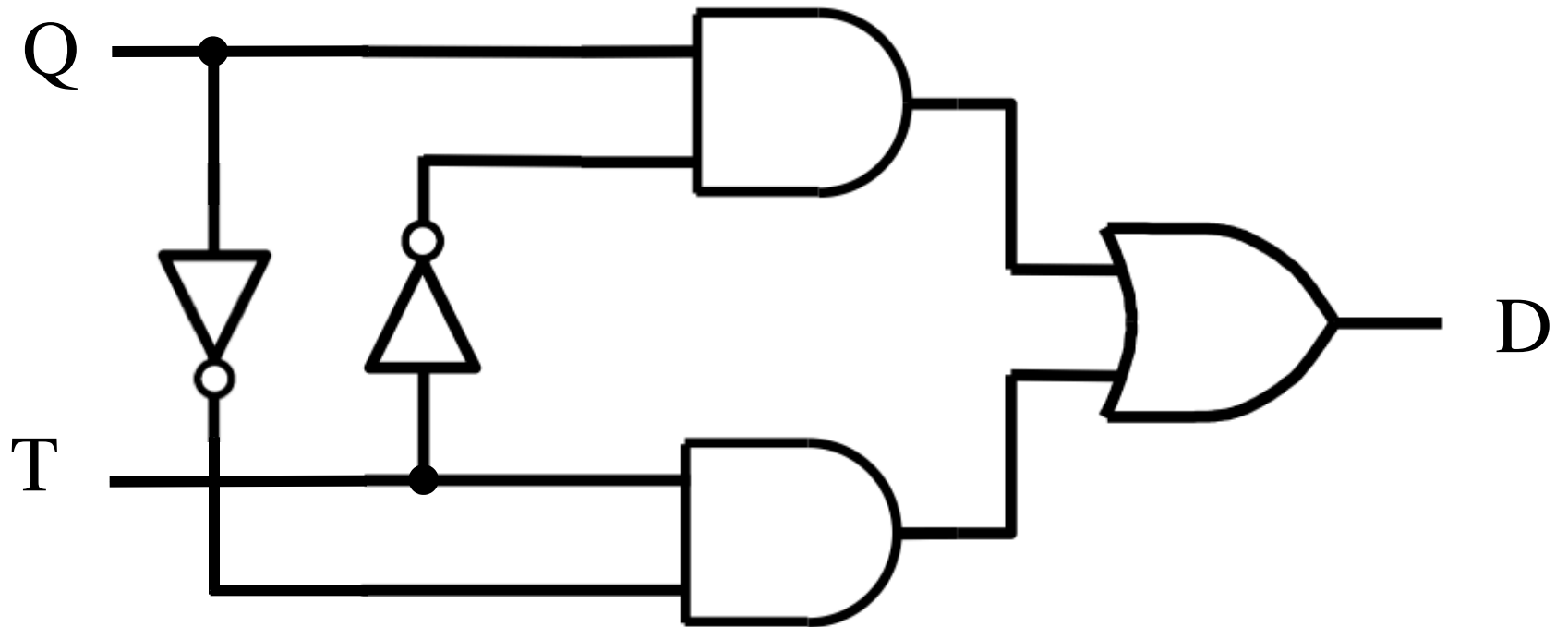


What is this?

What is this?

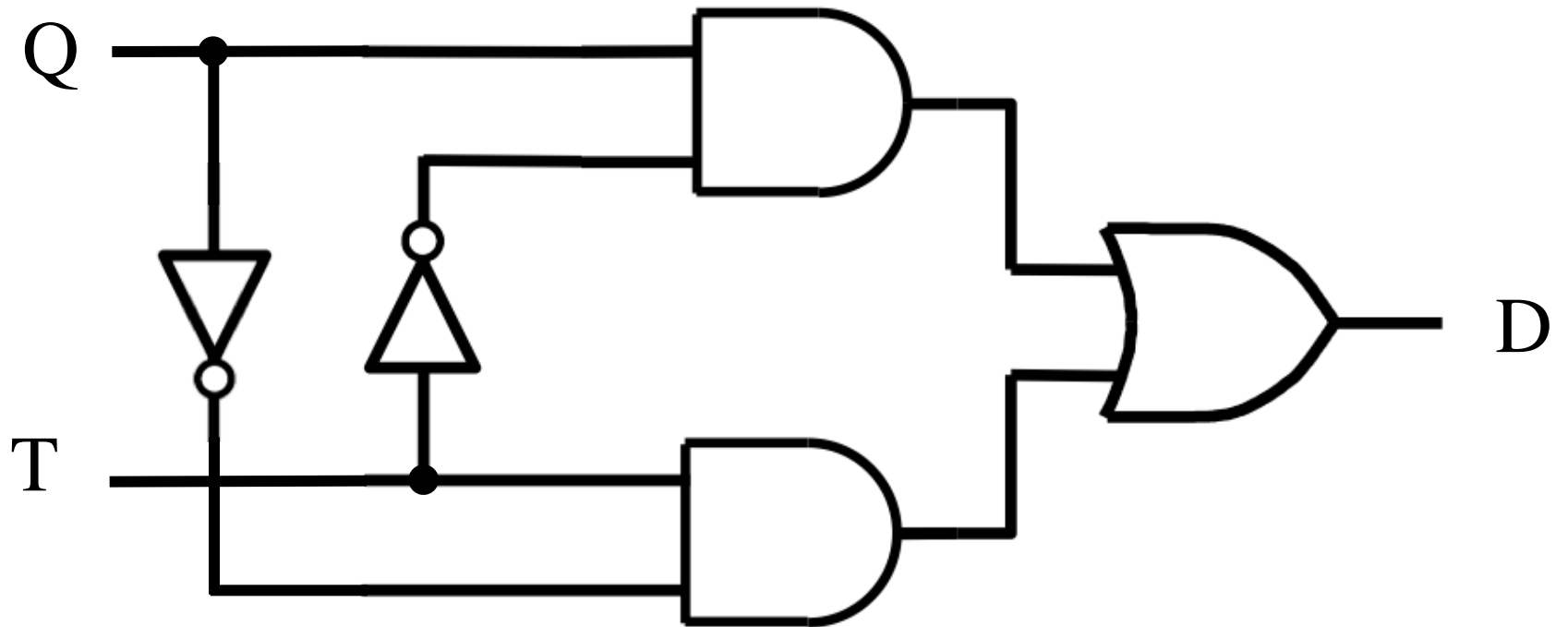


What is this?



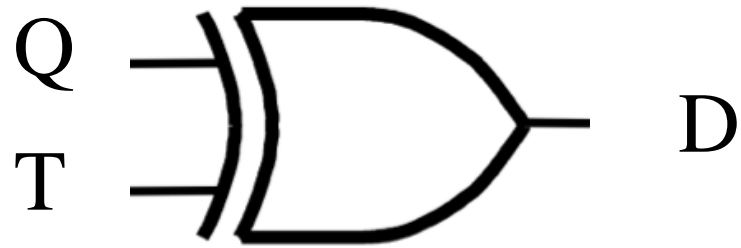
$$D = \overline{Q}T + Q\overline{T}$$

It is an XOR



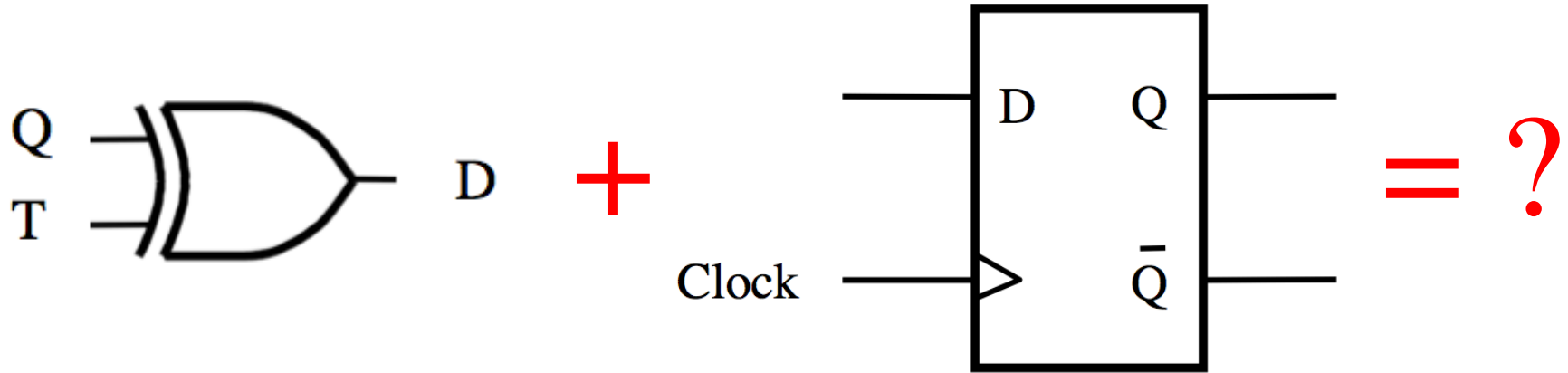
$$D = Q \oplus T$$

It is an XOR

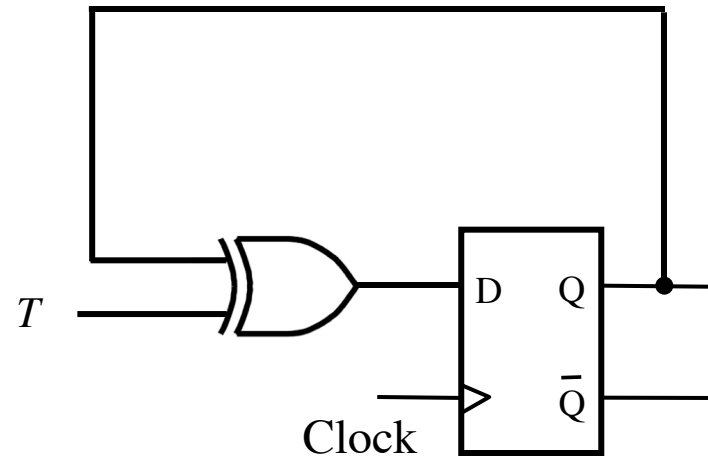


$$D = Q \oplus T$$

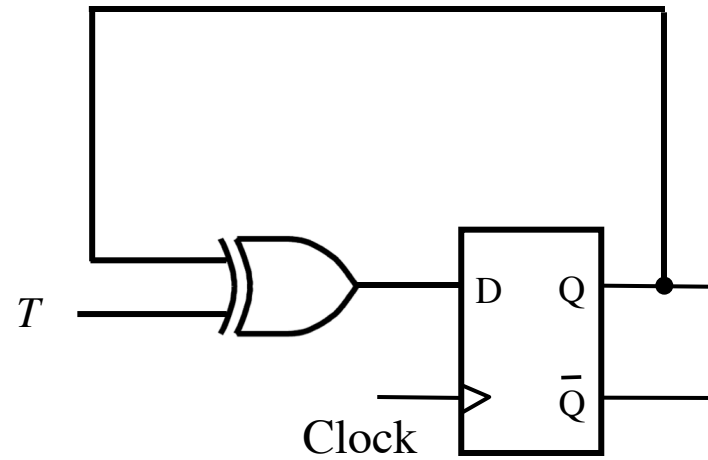
What is this?



It is a T Flip-Flop too

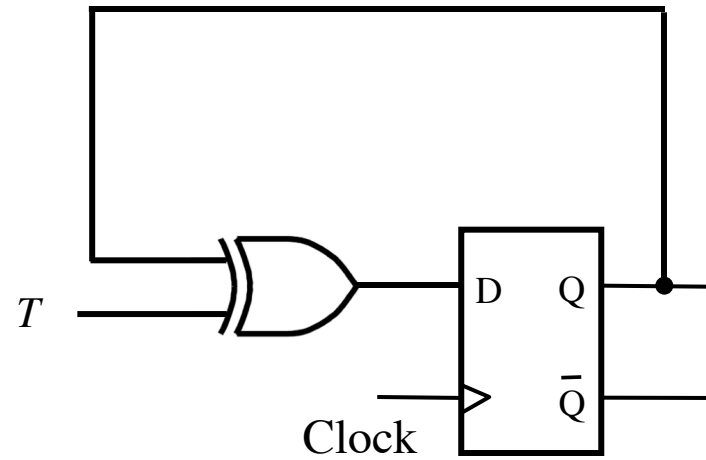


It is a T Flip-Flop too



T	Q	D
0	0	0
0	1	1
1	0	1
1	1	0

It is a T Flip-Flop too



T	Q	D
0	0	0
0	1	1
<hr/>		
1	0	1
1	1	0

Red brackets on the right side of the table group the rows. The first two rows (0,0) and (0,1) are grouped under a bracket labeled Q . The last two rows (1,0) and (1,1) are grouped under a bracket labeled \bar{Q} .

T Flip-Flop

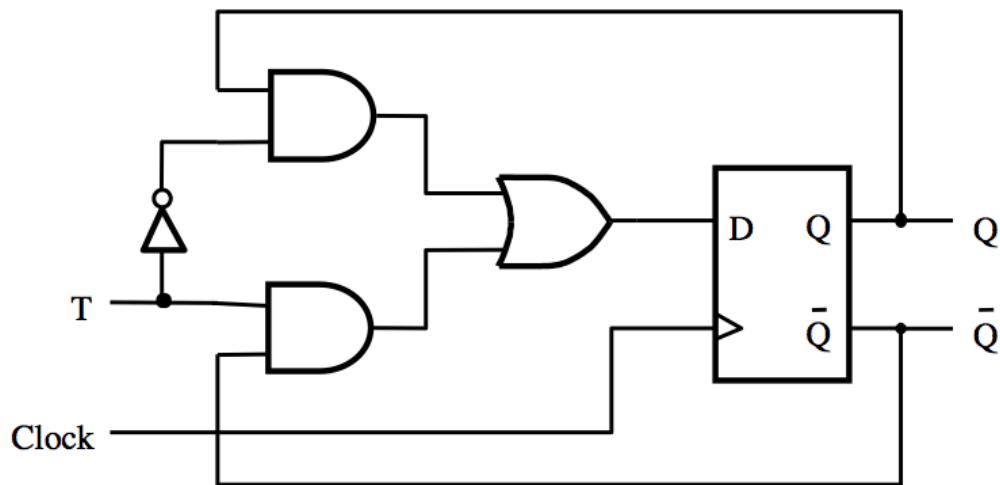
(how it works)

If $T=0$ then it stays in its current state

If $T=1$ then it reverses its current state

In other words the circuit “toggles” its state when $T=1$. This is why it is called T flip-flop.

T Flip-Flop (circuit and truth table)

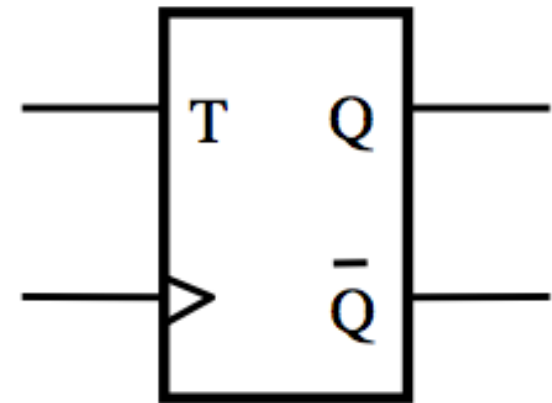
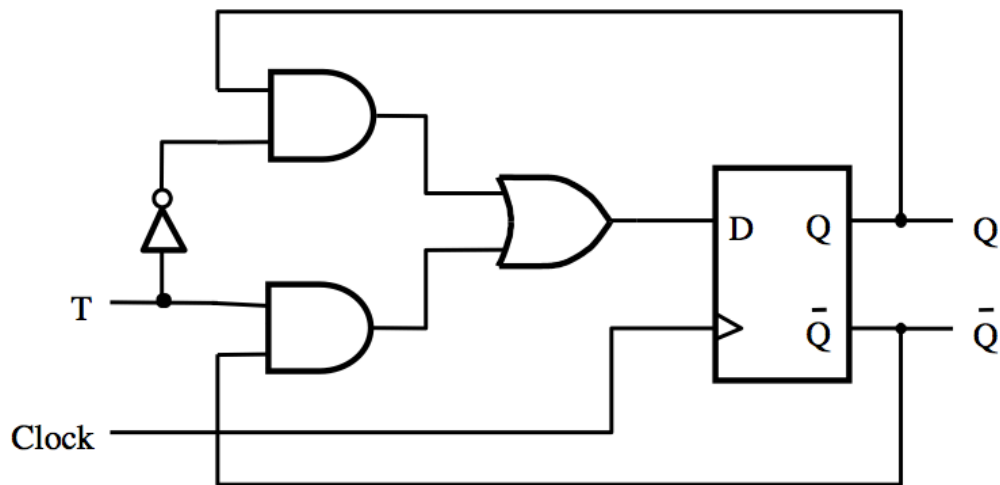


T	$Q(t+1)$
0	$Q(t)$
1	$\bar{Q}(t)$

[Figure 5.15a,b from the textbook]

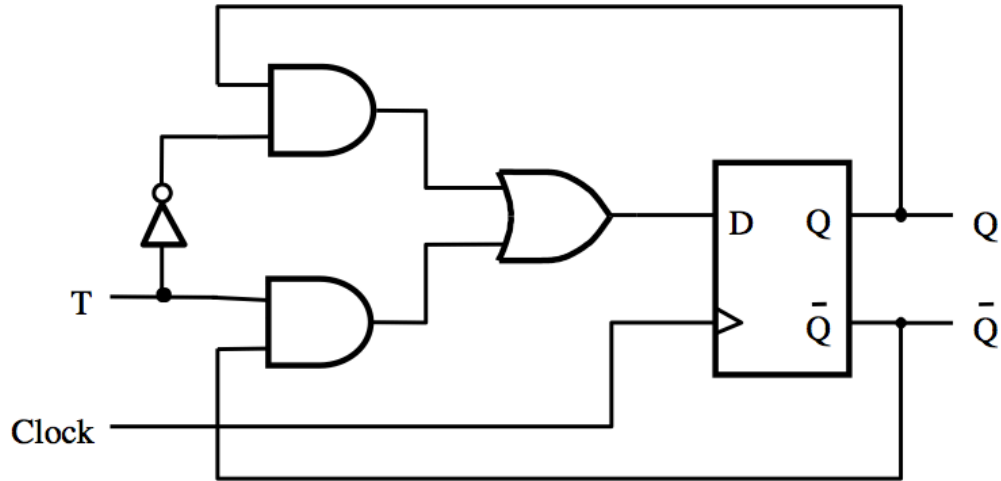
T Flip-Flop


(circuit and graphical symbol)



[Figure 5.15a,c from the textbook]

T Flip-Flop (Timing Diagram)

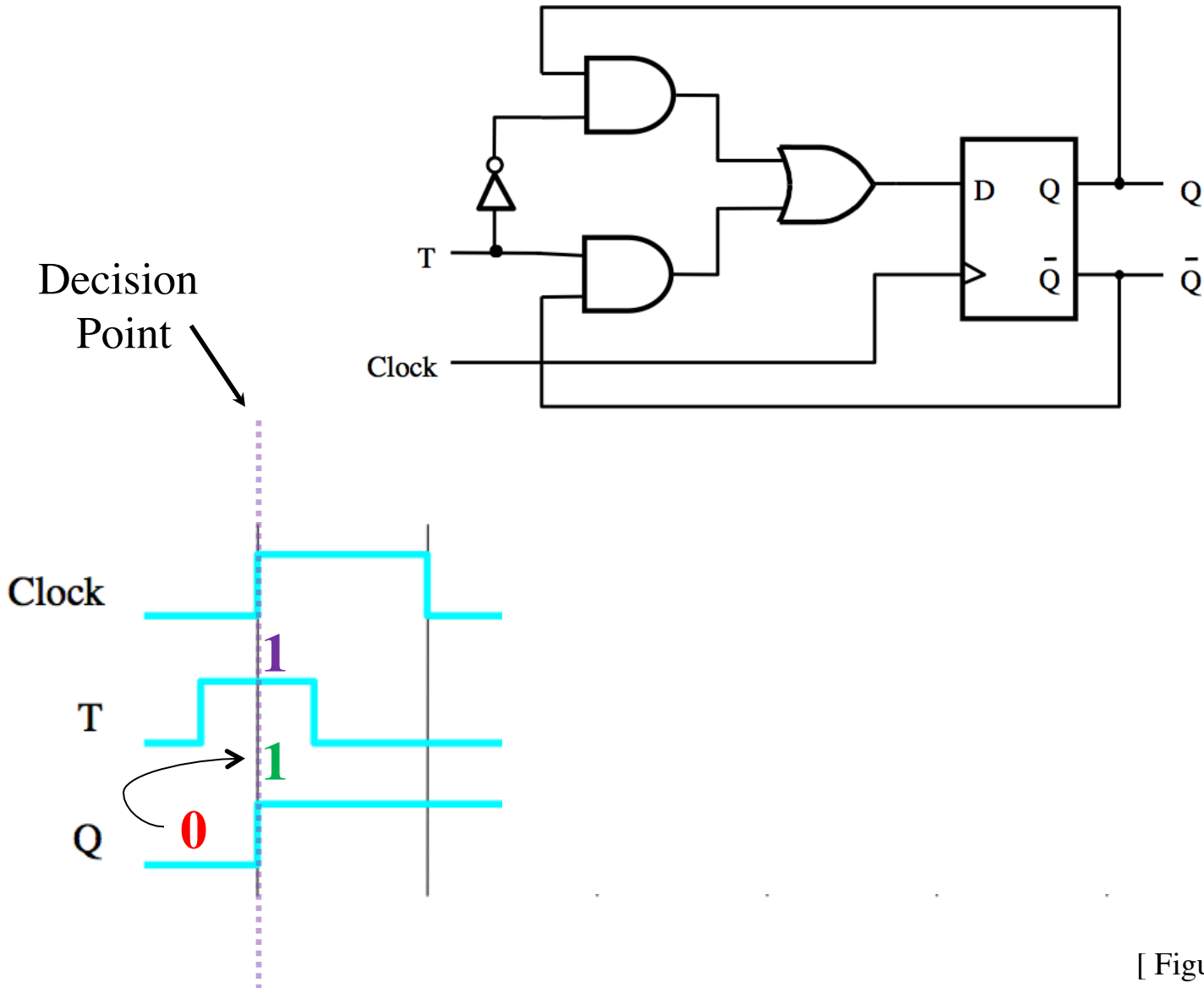


Clock 

T 

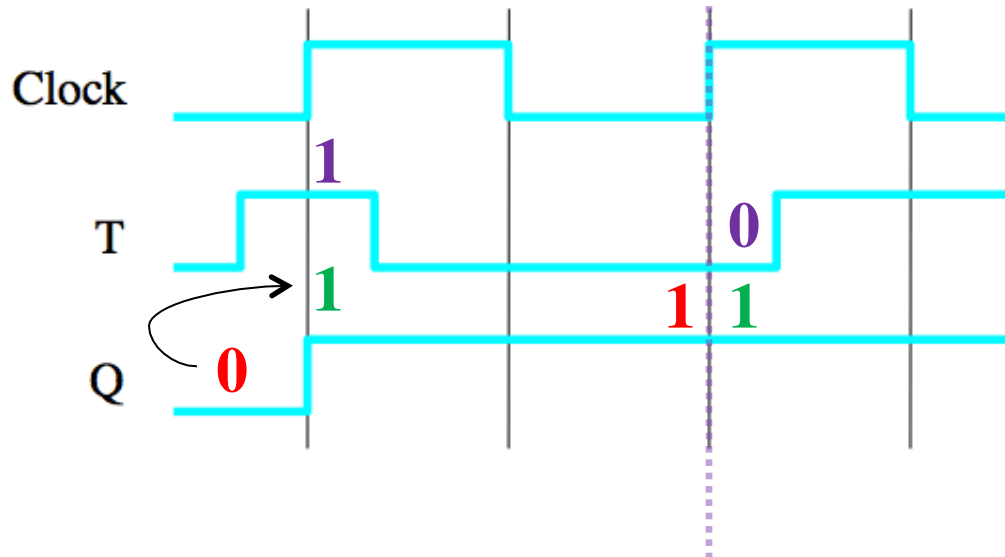
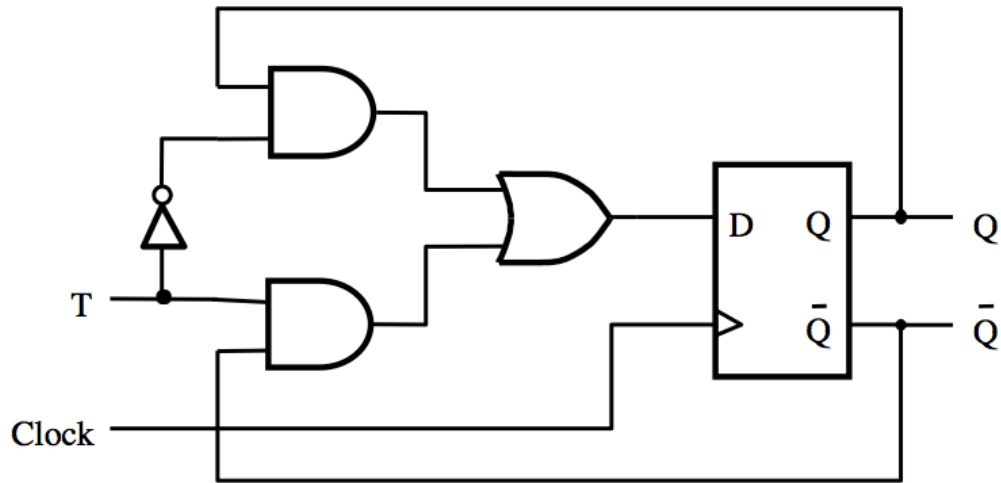
Q 

T Flip-Flop (Timing Diagram)



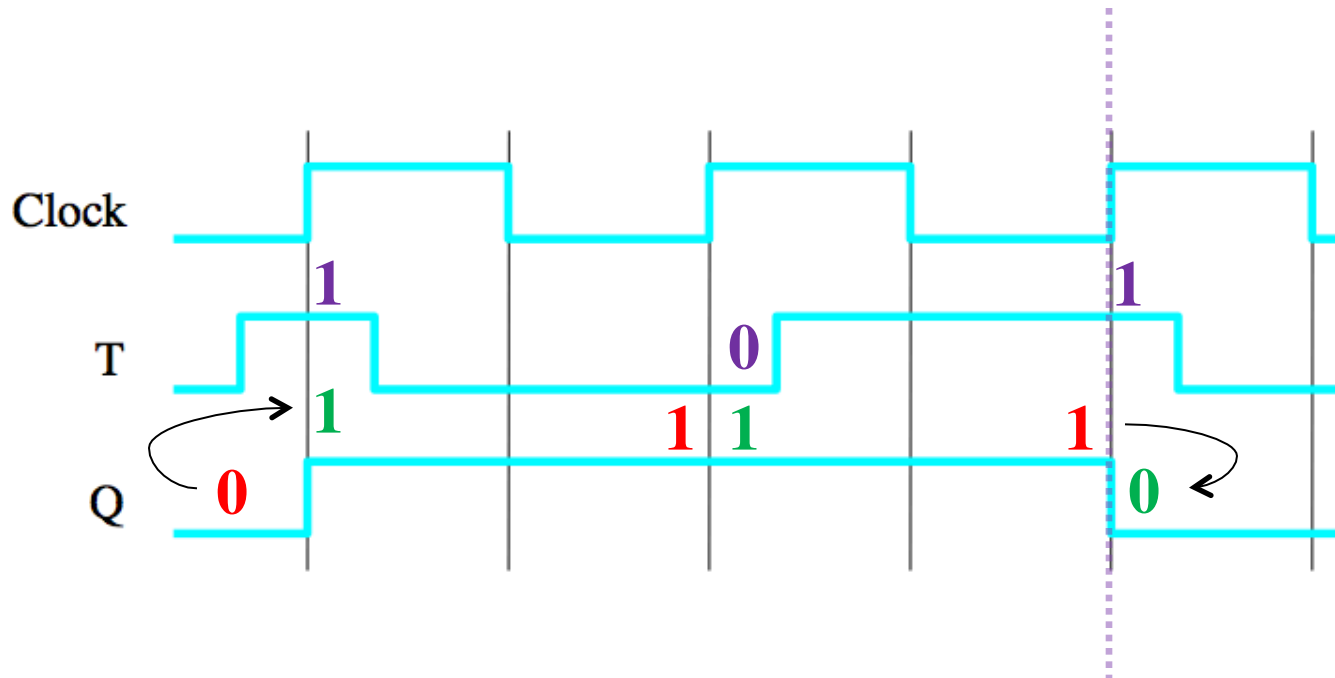
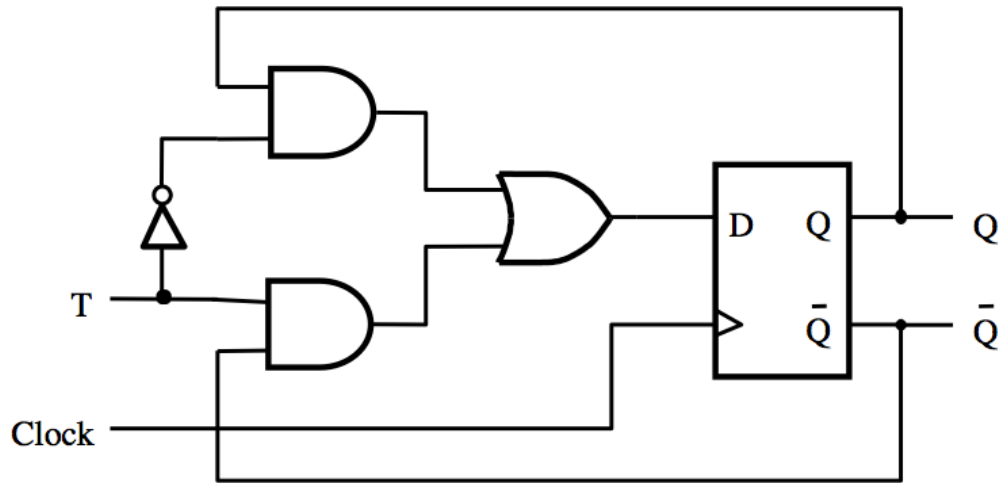
[Figure 5.15d from the textbook]

T Flip-Flop (Timing Diagram)



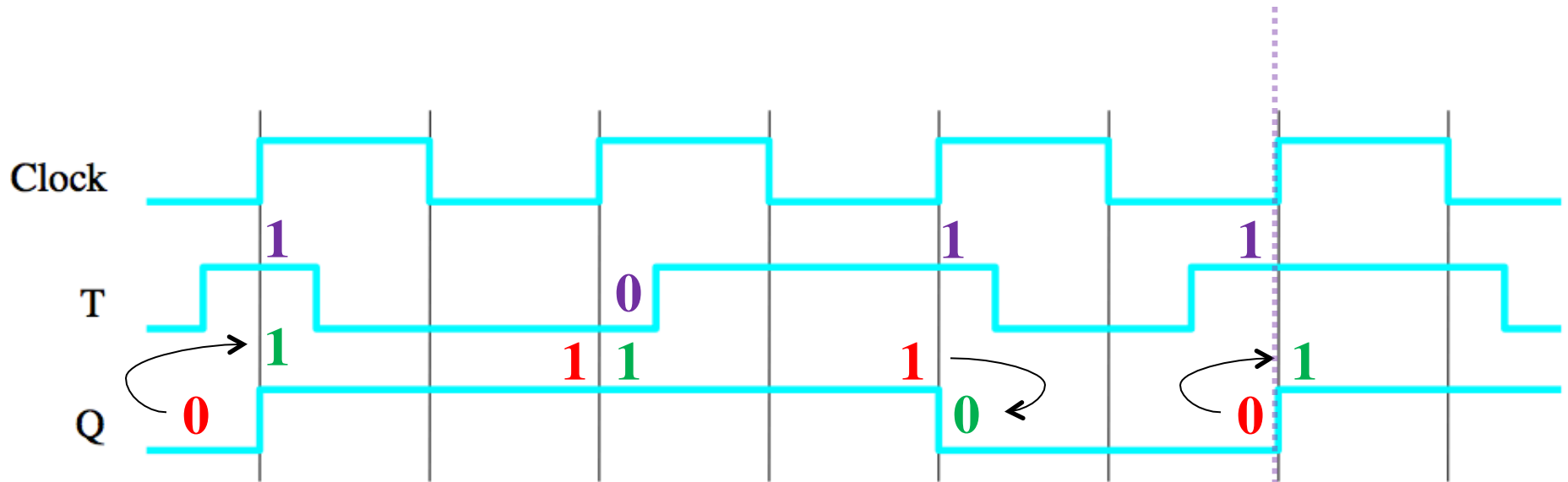
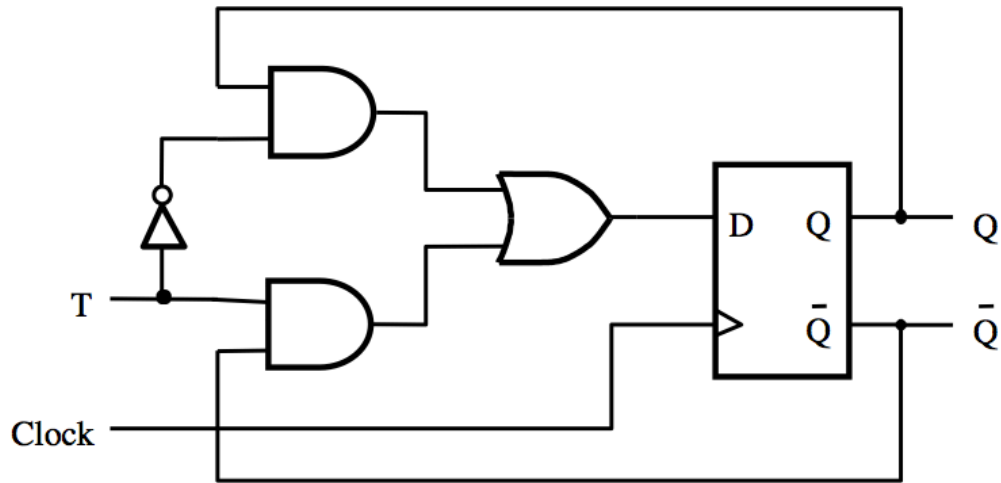
[Figure 5.15d from the textbook]

T Flip-Flop (Timing Diagram)



[Figure 5.15d from the textbook]

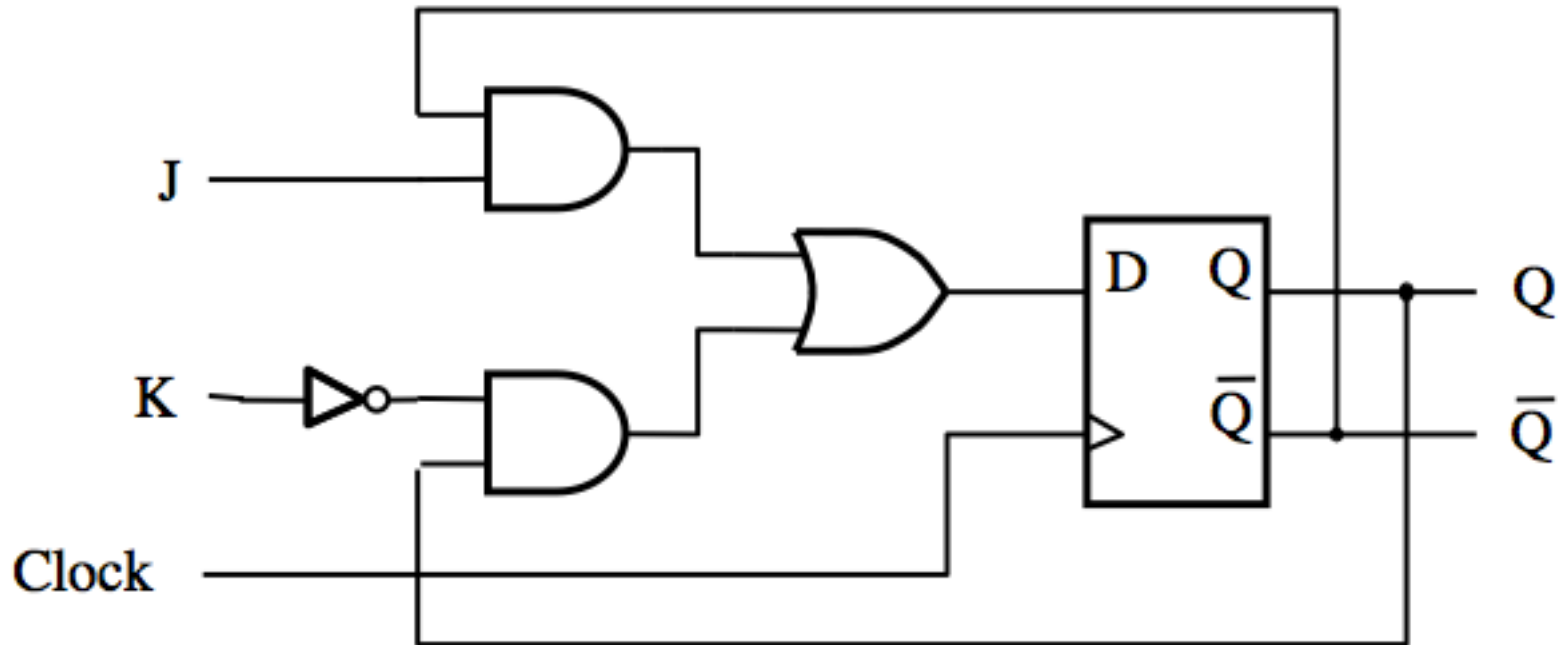
T Flip-Flop (Timing Diagram)



[Figure 5.15d from the textbook]

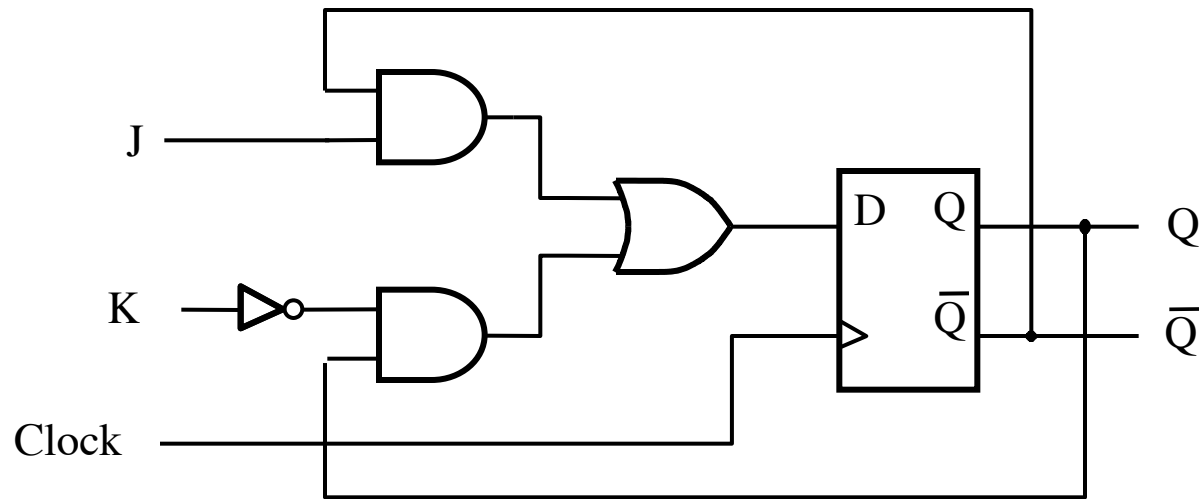
JK Flip-Flop

JK Flip-Flop



$$D = J\bar{Q} + \bar{K}Q$$

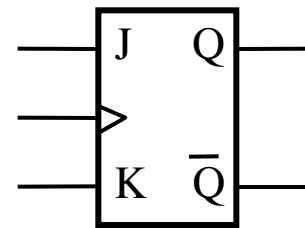
JK Flip-Flop



(a) Circuit

J	K	$Q(t+1)$	
0	0	$Q(t)$	Hold
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}(t)$	Toggle

(b) Truth table



(c) Graphical symbol

JK Flip-Flop (how it works)

A versatile circuit that can be used both as a SR flip-flop and as a T flip flop

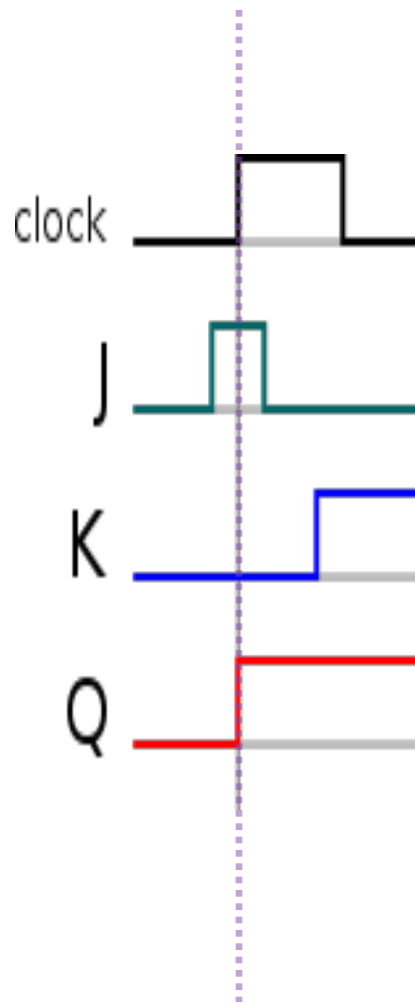
If $J=0$ and $S=0$ it stays in the same state

Just like SR It can be set and reset

$J=S$ and $K=R$

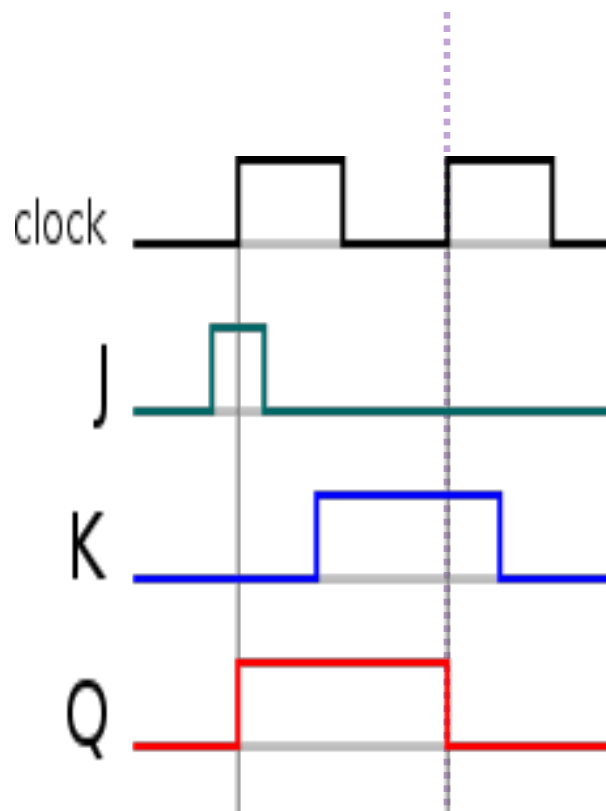
If $J=K=1$ then it behaves as a T flip-flop

JK Flip-Flop (timing diagram)



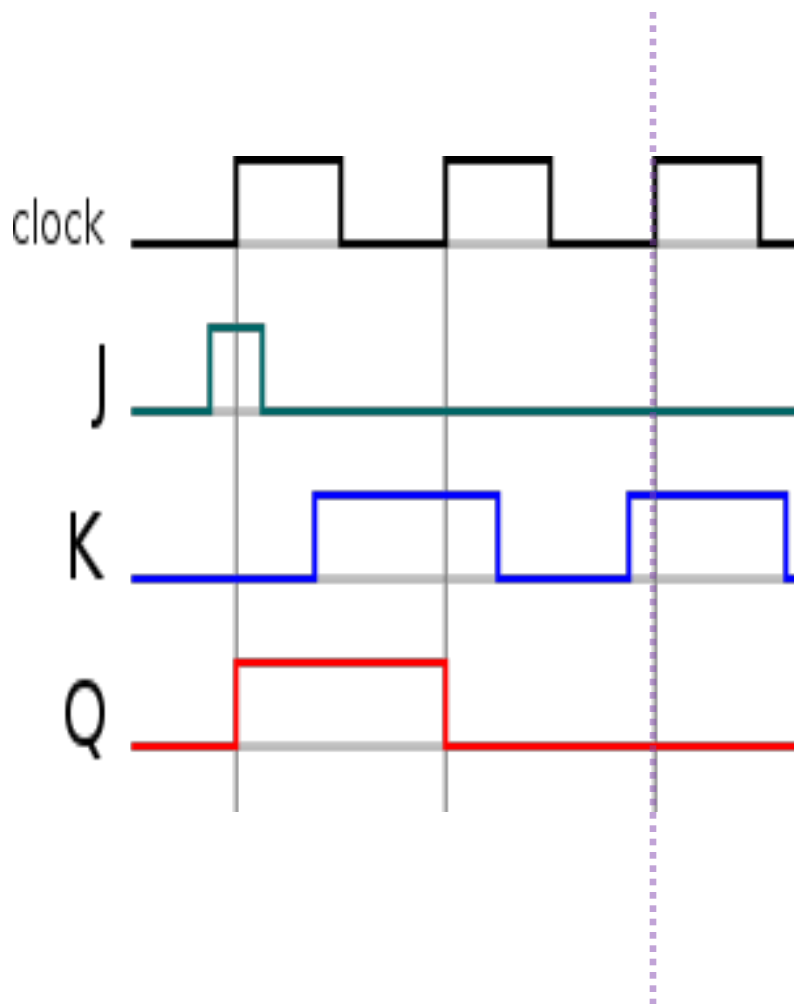
J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

JK Flip-Flop (timing diagram)



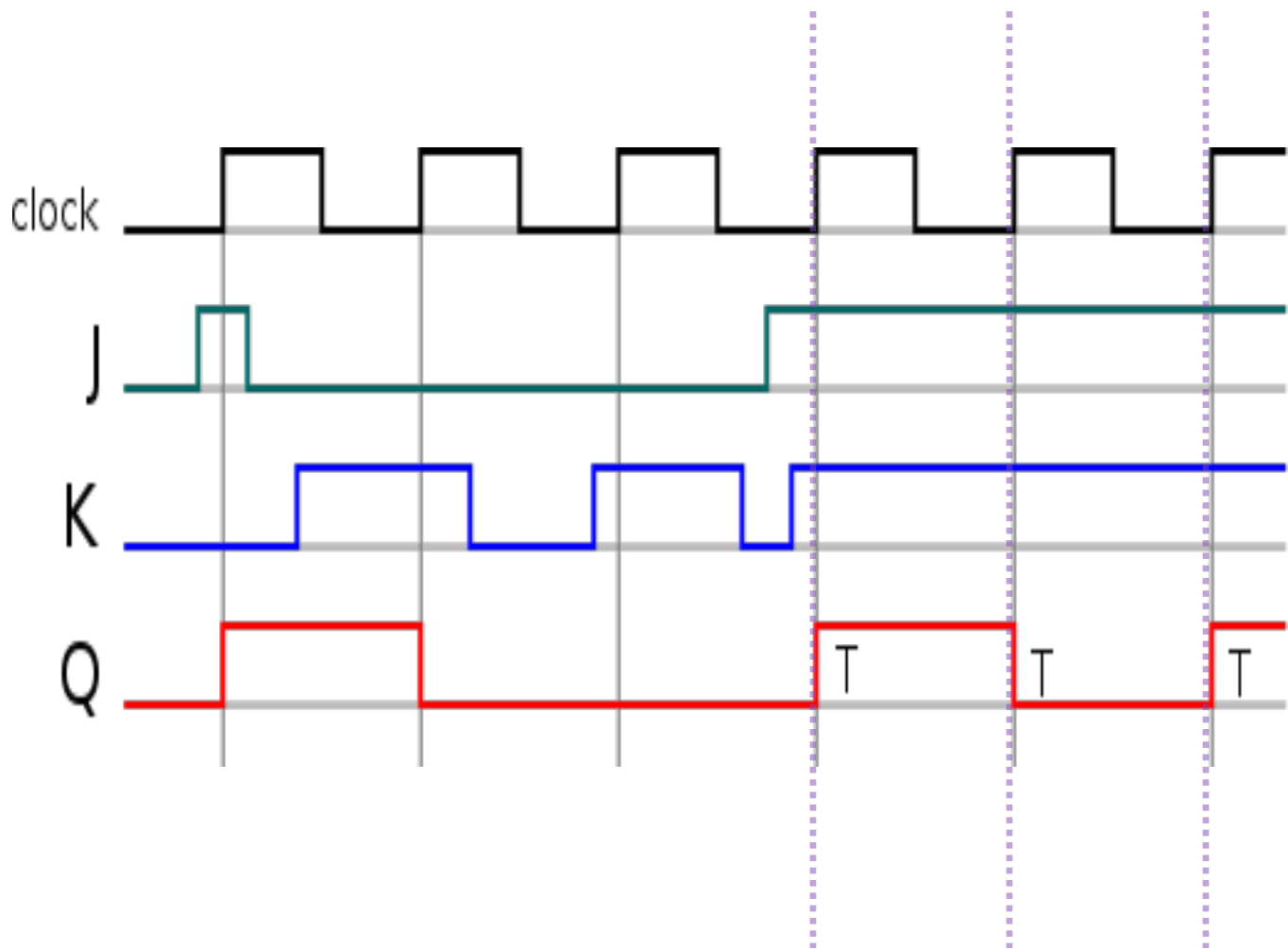
J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

JK Flip-Flop (timing diagram)



J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

JK Flip-Flop (timing diagram)



J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

Questions?

THE END