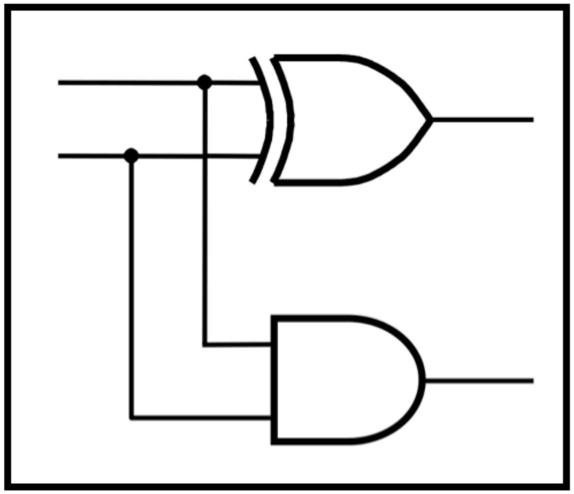


CprE 281: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Designing a Counter
(Using the Sequential Circuit Approach)

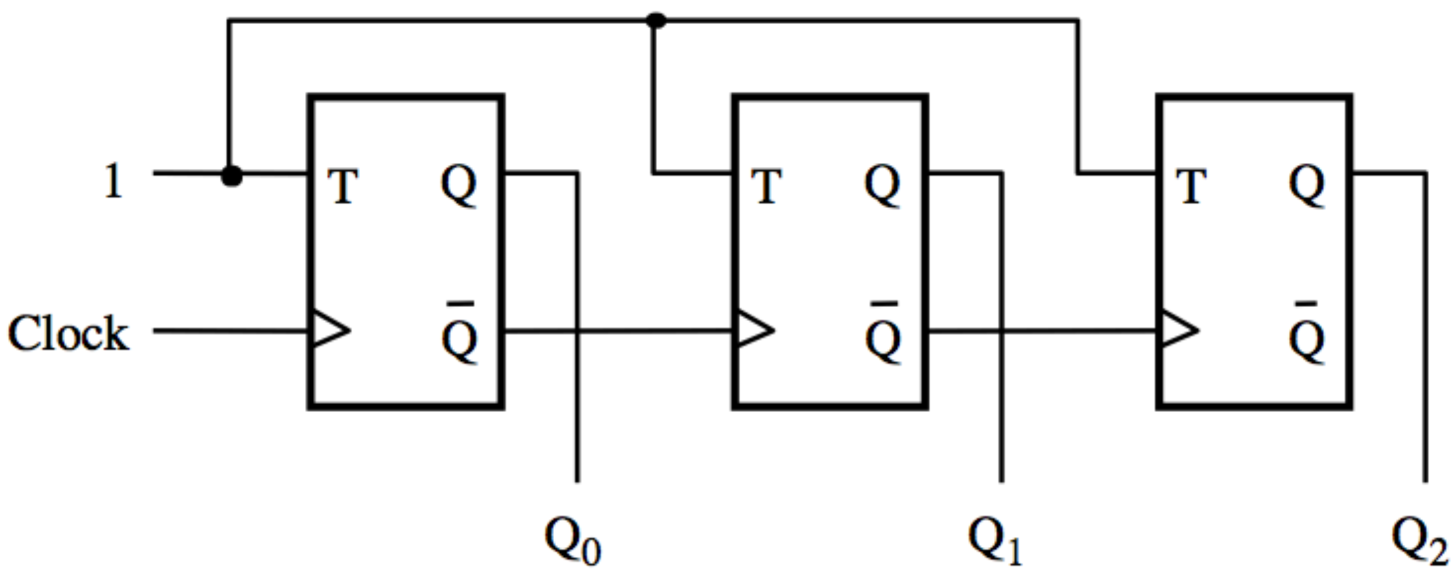
CprE 281: Digital Logic
Iowa State University, Ames, IA

Example:
Implement a modulo-8 counter

Mini Review

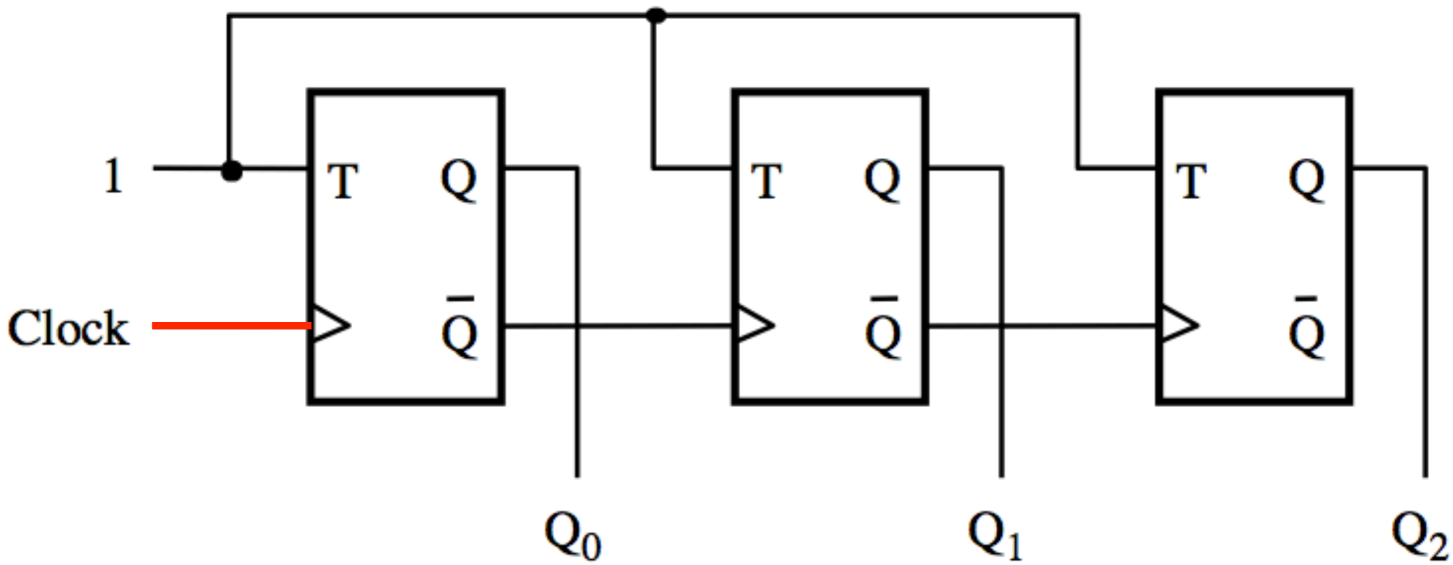
Asynchronous Counters

A three-bit up-counter



[Figure 5.19 from the textbook]

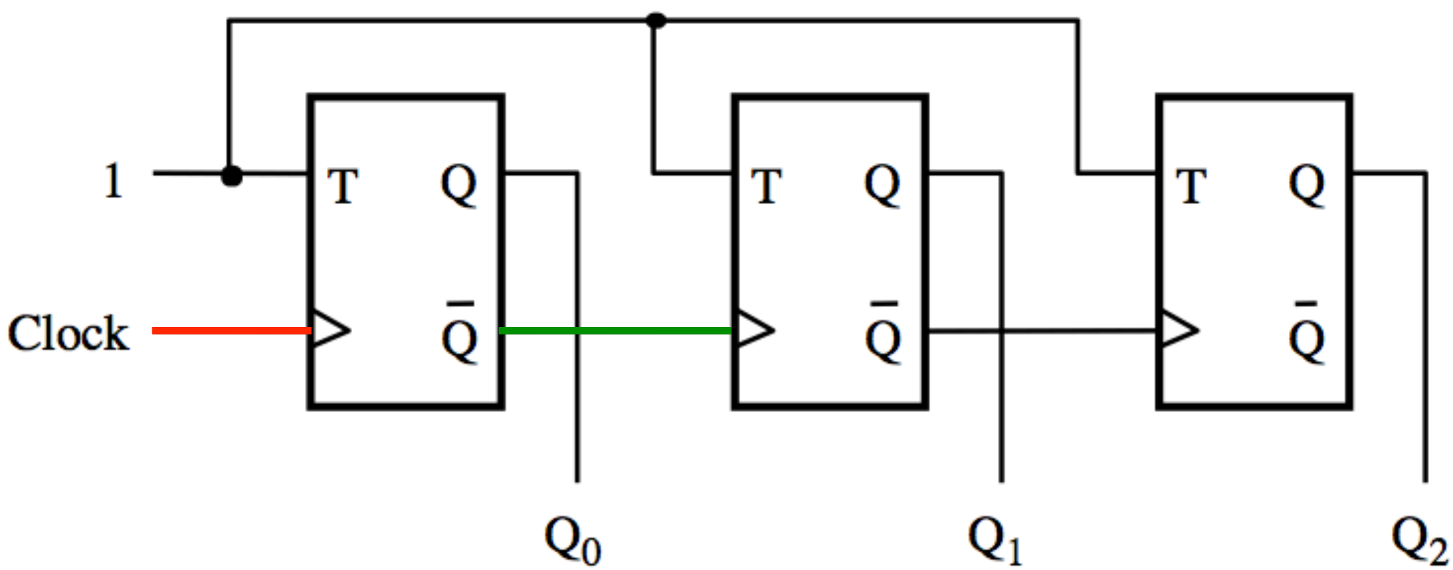
A three-bit up-counter



The first flip-flop changes
on the positive edge of the clock

[Figure 5.19 from the textbook]

A three-bit up-counter

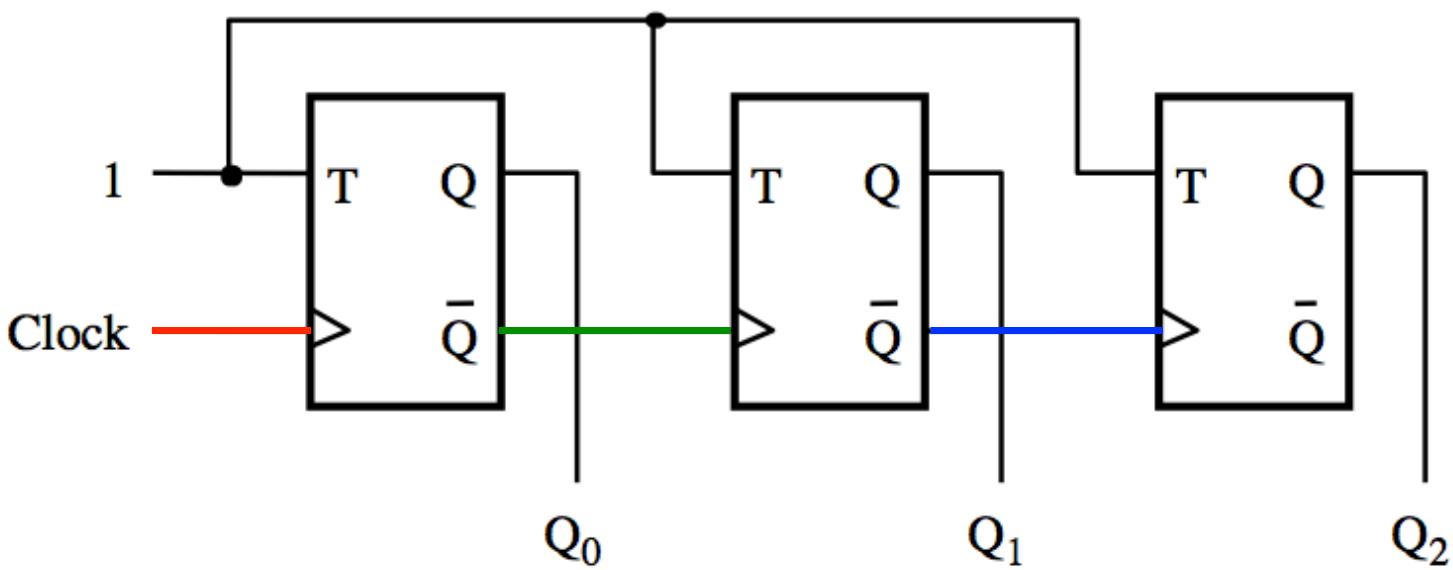


The first flip-flop changes
on the positive edge of the clock

The second flip-flop changes
on the positive edge of $\overline{Q}_0$

[Figure 5.19 from the textbook]

A three-bit up-counter



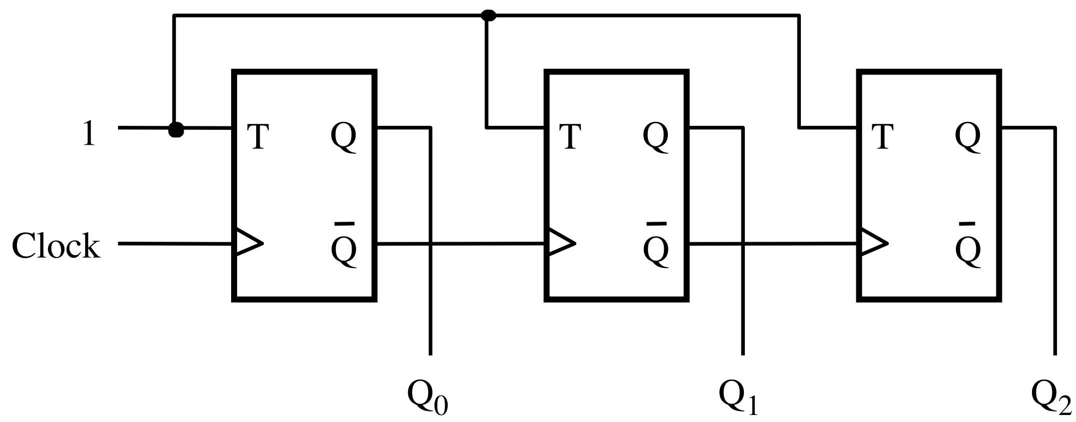
The first flip-flop changes on the positive edge of the clock

The second flip-flop changes on the positive edge of $\overline{Q}_0$

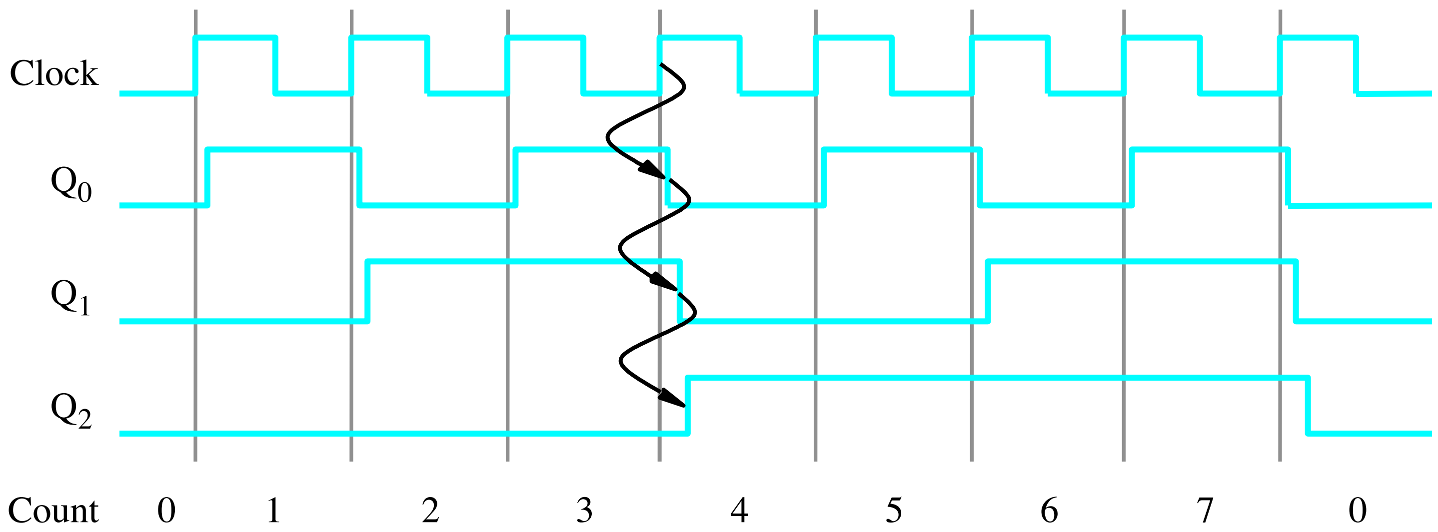
The third flip-flop changes on the positive edge of $\overline{Q}_1$

[Figure 5.19 from the textbook]

A three-bit up-counter



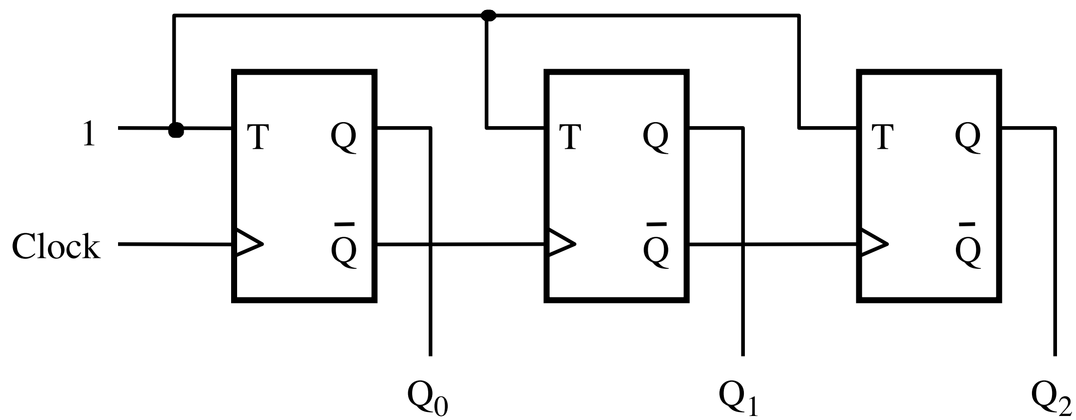
(a) Circuit



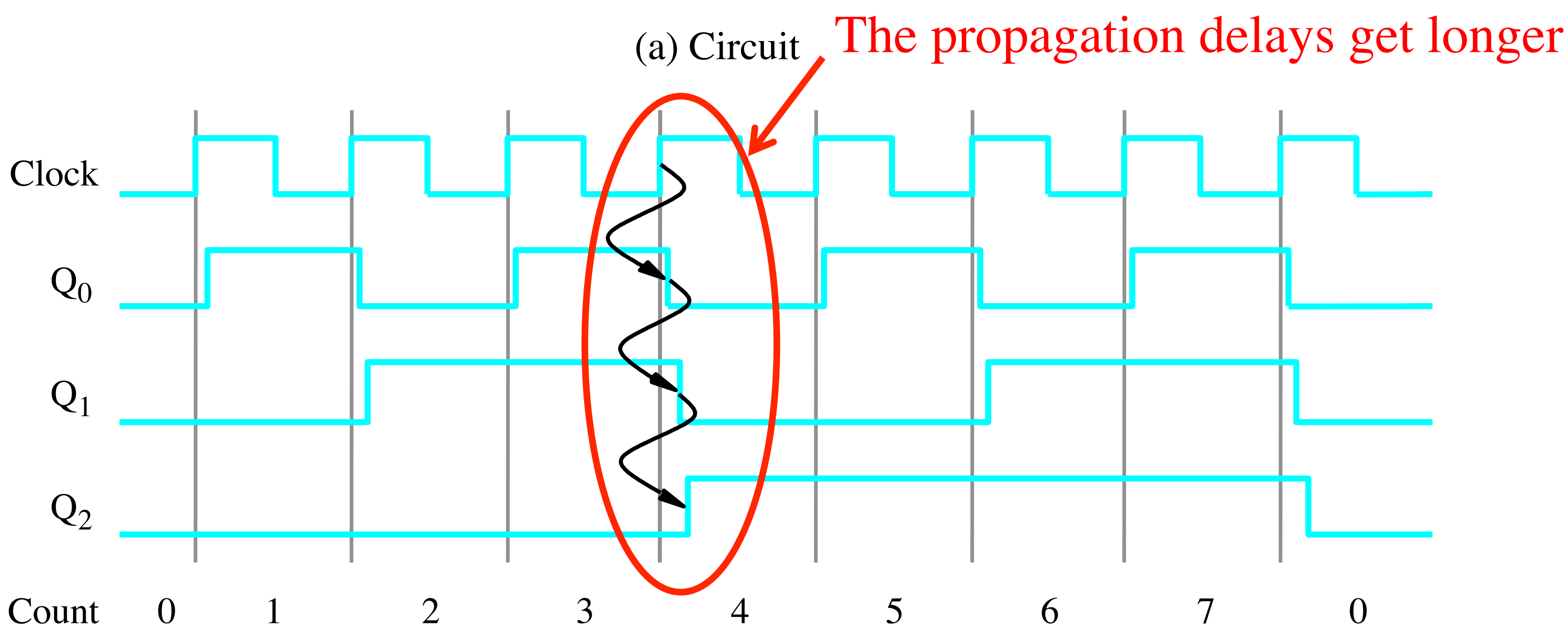
(b) Timing diagram

[Figure 5.19 from the textbook]

A three-bit up-counter



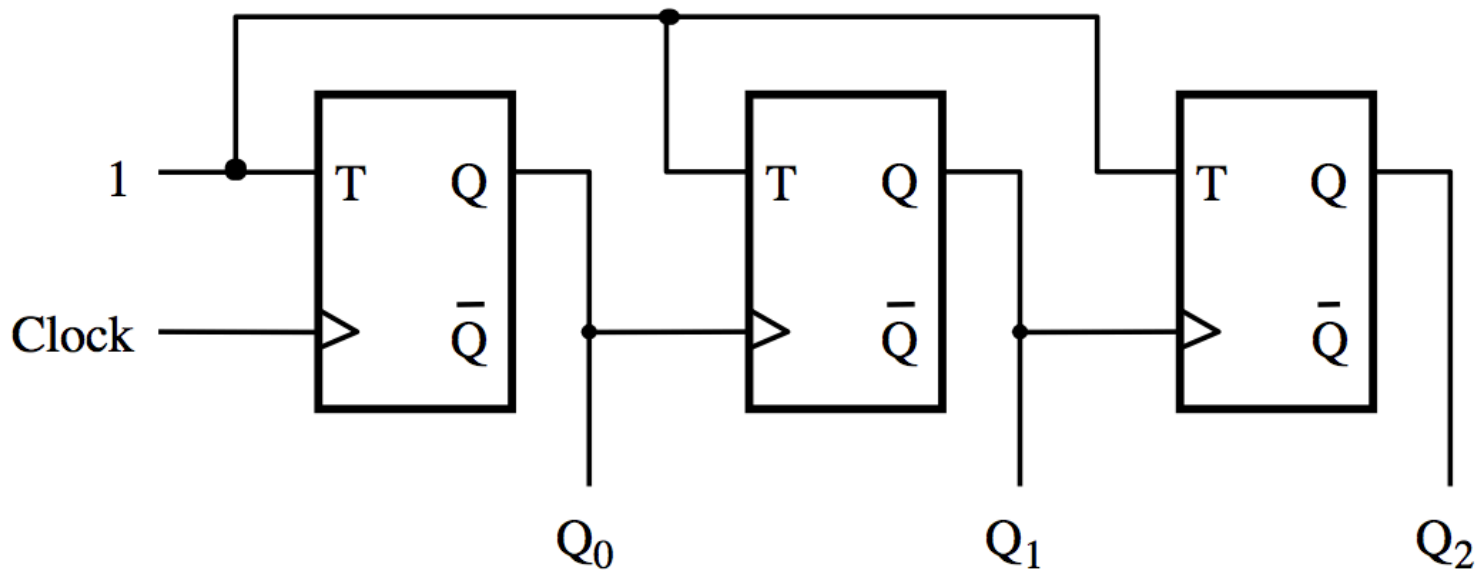
(a) Circuit



(b) Timing diagram

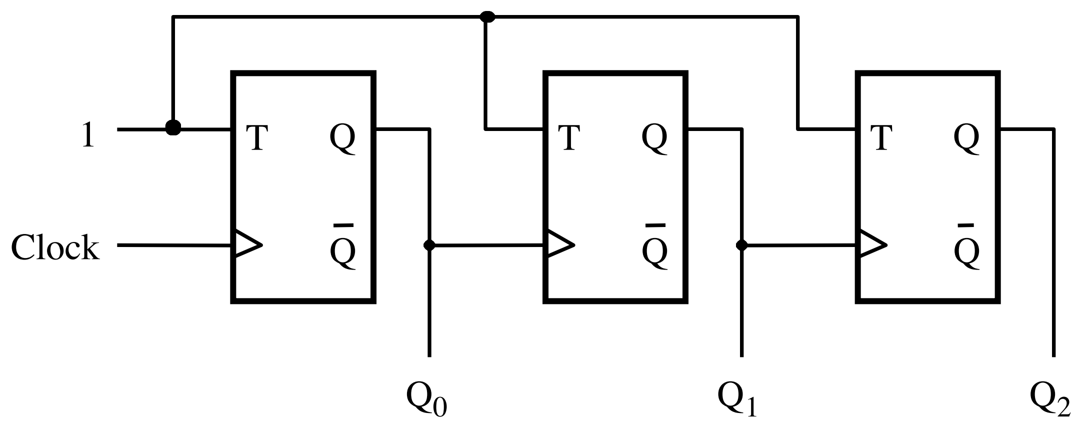
[Figure 5.19 from the textbook]

A three-bit down-counter

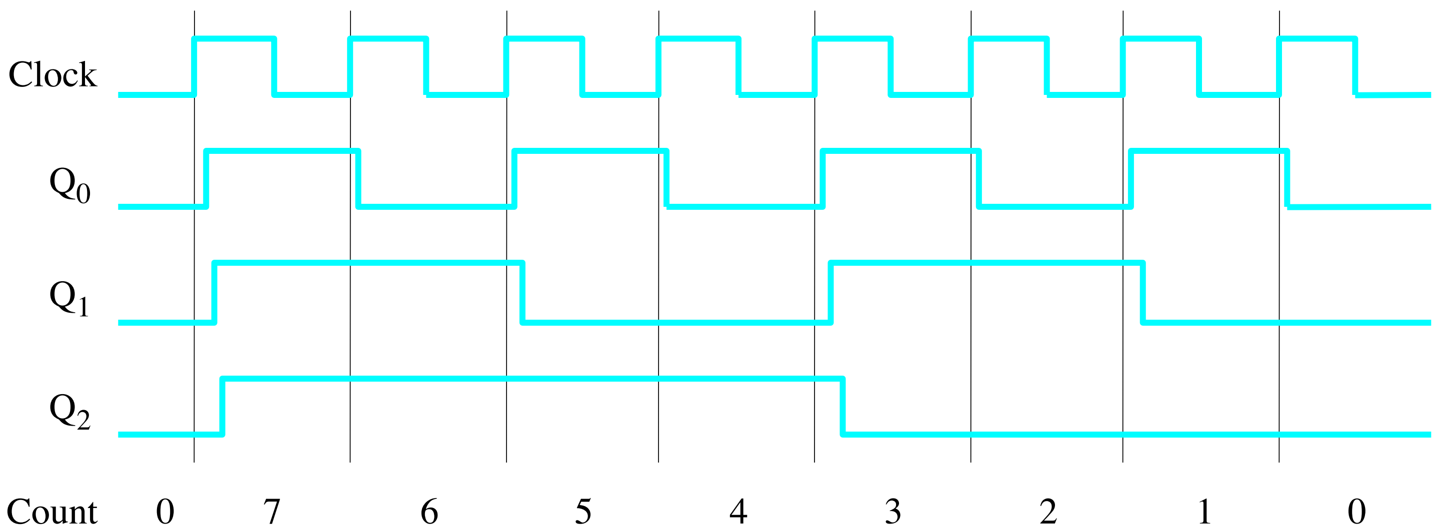


[Figure 5.20 from the textbook]

A three-bit down-counter



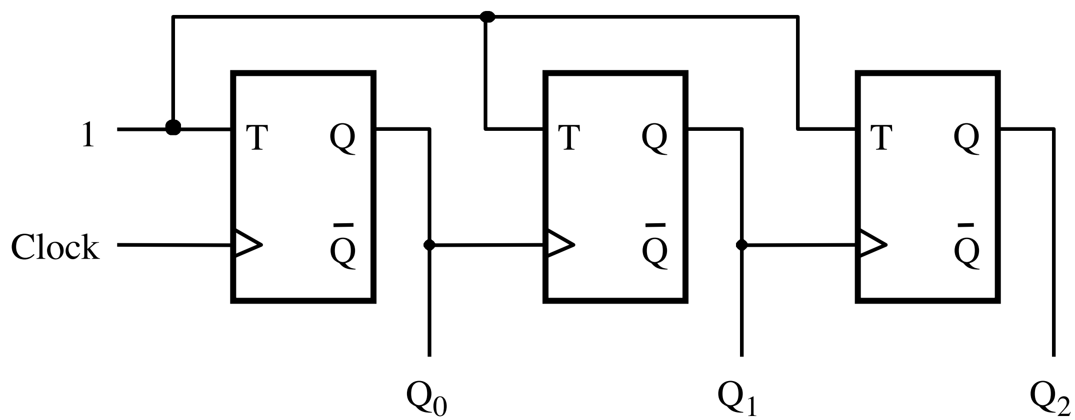
(a) Circuit



(b) Timing diagram

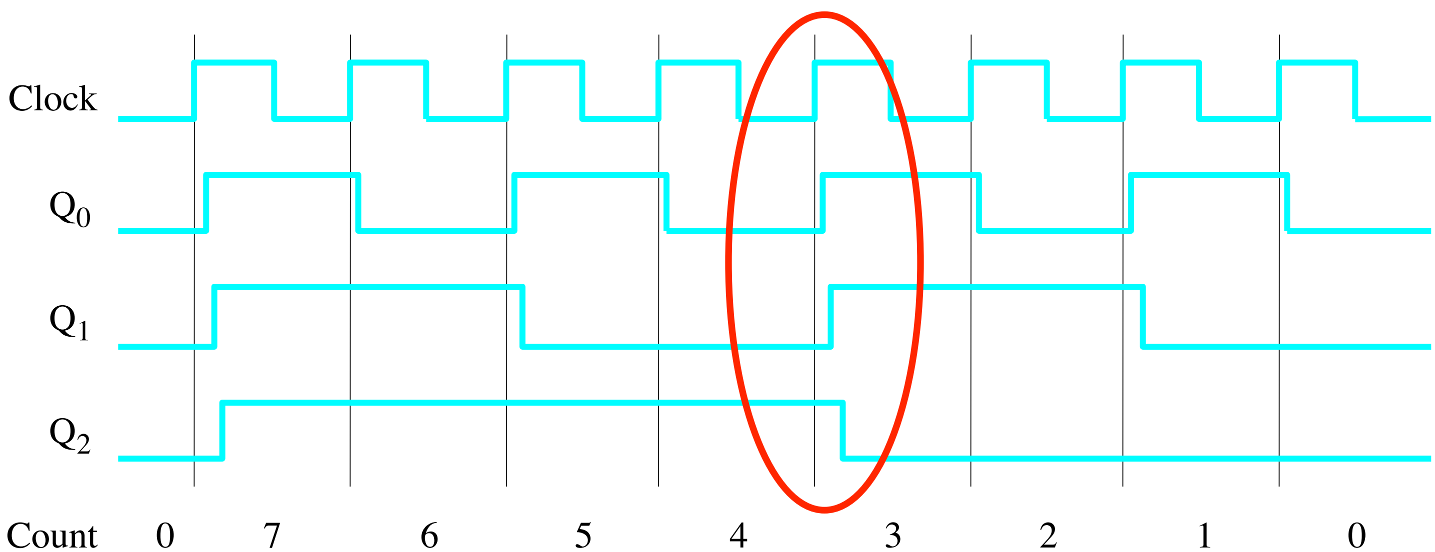
[Figure 5.20 from the textbook]

A three-bit down-counter



(a) Circuit

The propagation delays get longer

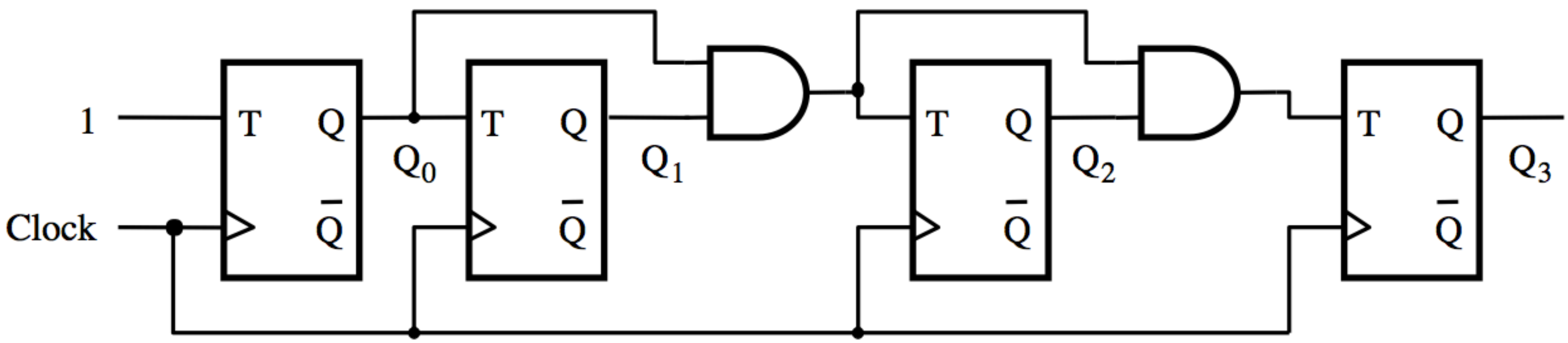


(b) Timing diagram

[Figure 5.20 from the textbook]

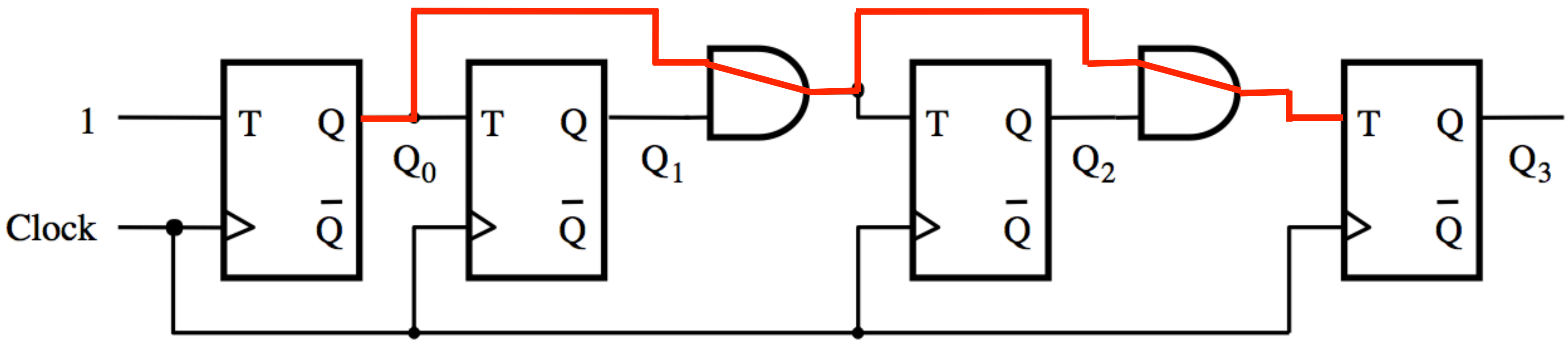
Synchronous Counters

A four-bit synchronous up-counter



[Figure 5.21 from the textbook]

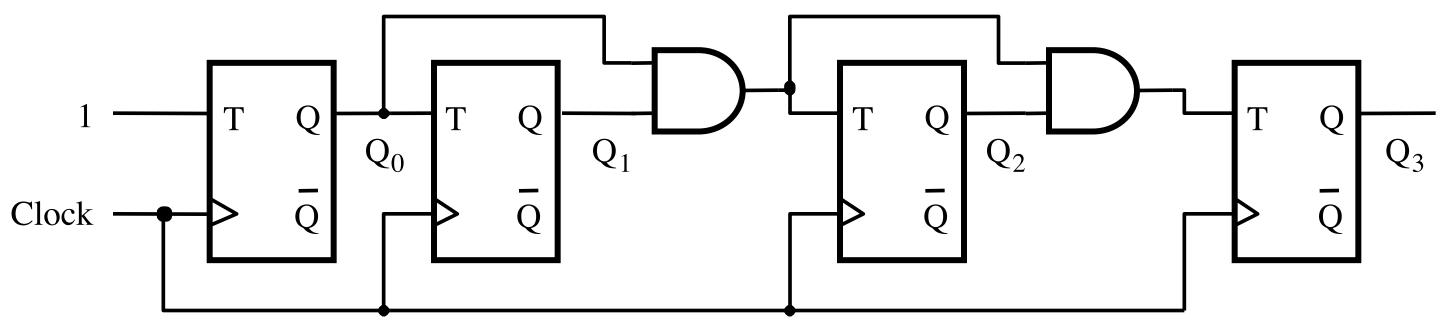
A four-bit synchronous up-counter



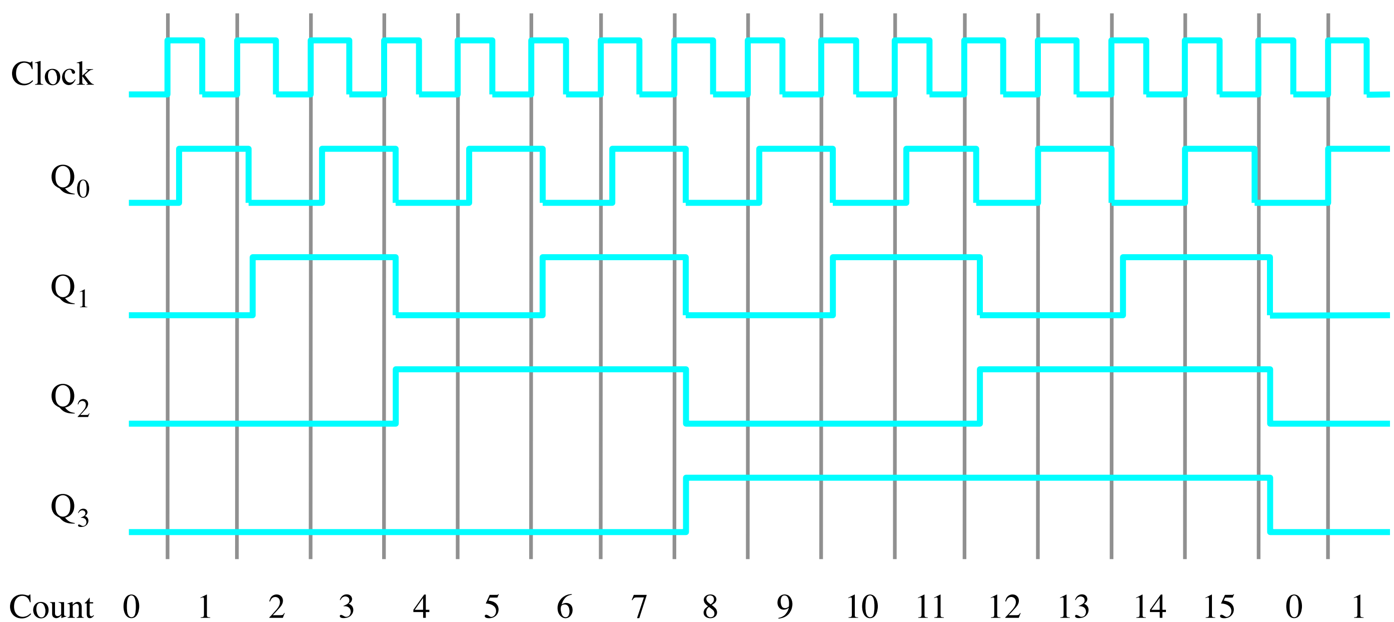
The propagation delay through all AND gates combined must not exceed the clock period minus the setup time for the flip-flops

[Figure 5.21 from the textbook]

A four-bit synchronous up-counter



(a) Circuit

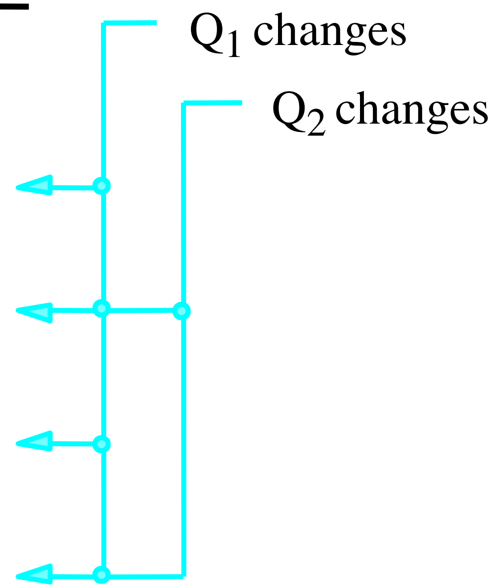


(b) Timing diagram

[Figure 5.21 from the textbook]

Derivation of the synchronous up-counter

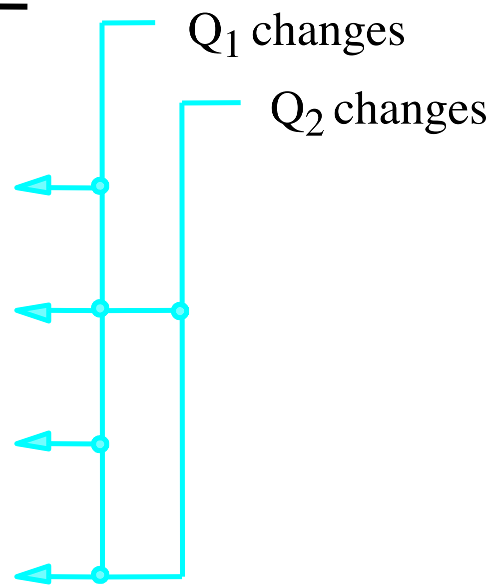
Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



[Table 5.1 from the textbook]

Derivation of the synchronous up-counter

Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



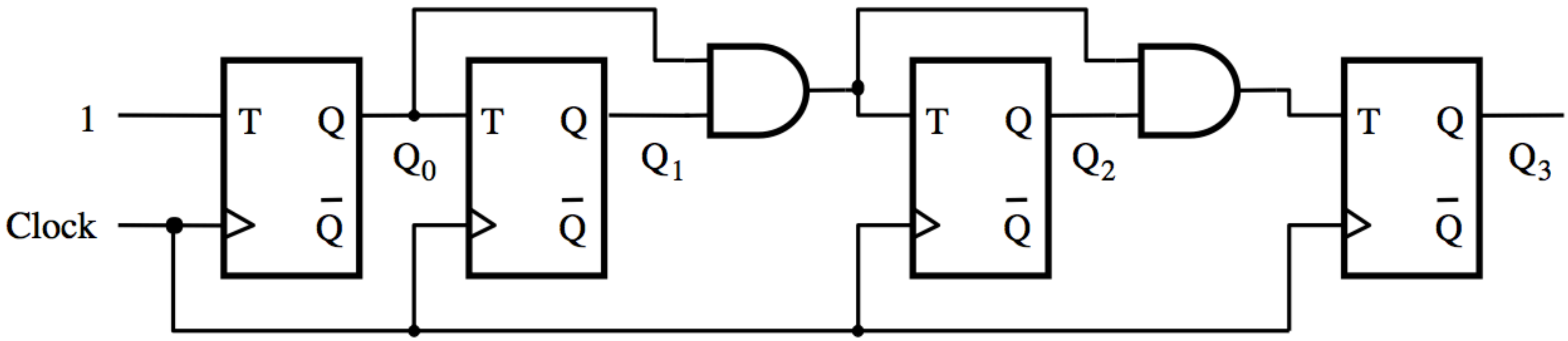
$T_0 = 1$

$T_1 = Q_0$

$T_2 = Q_0 Q_1$

[Table 5.1 from the textbook]

A four-bit synchronous up-counter



$T_0 = 1$

$T_1 = Q_0$

$T_2 = Q_0 \, Q_1$

[Figure 5.21 from the textbook]

In general we have

$$T_0 = 1$$

$$T_1 = Q_0$$

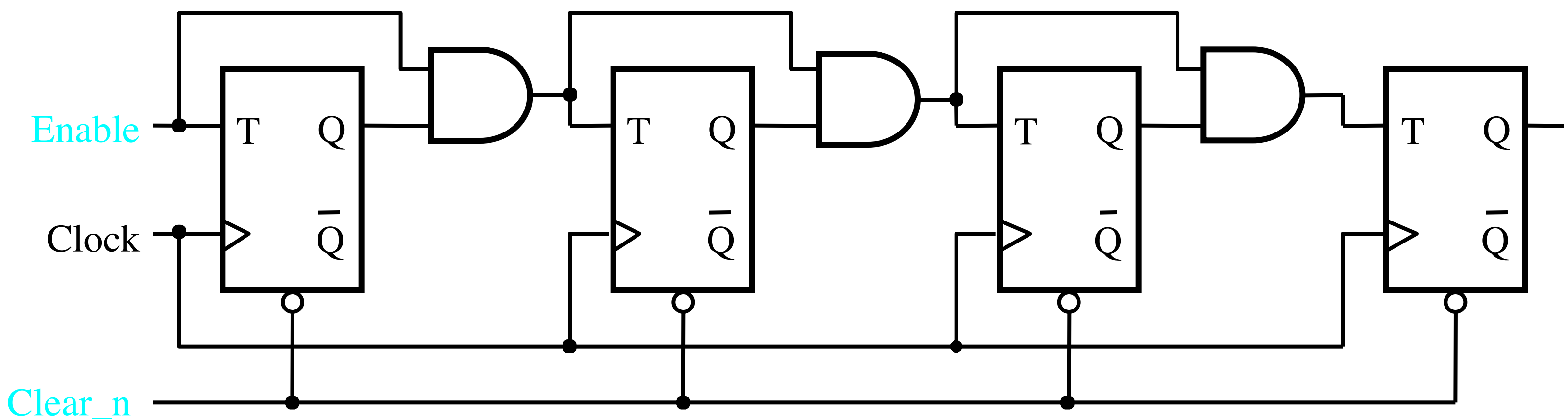
$$T_2 = Q_0\, Q_1$$

$$T_3 = Q_0\, Q_1\, Q_2$$

$$\ldots$$

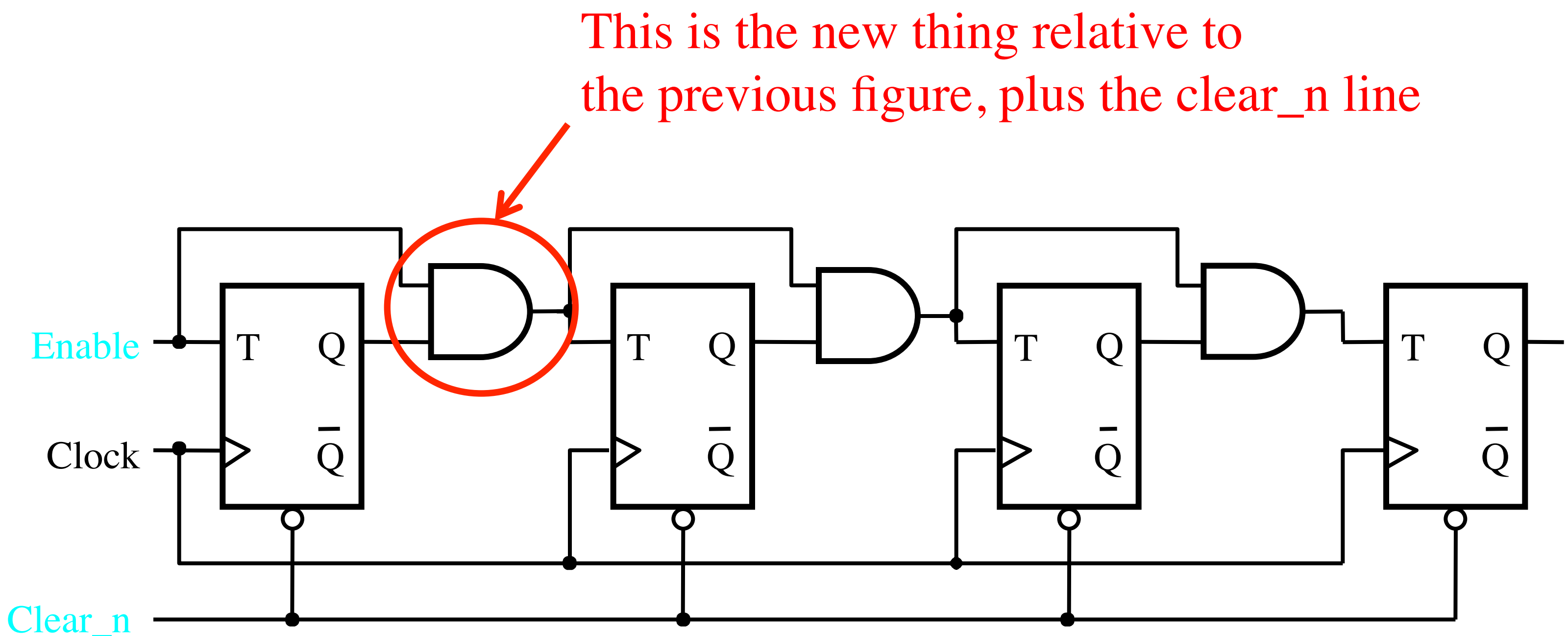
$$T_n = Q_0\, Q_1\, Q_2 \ldots Q_{n-1}$$

Inclusion of Enable and Clear capability



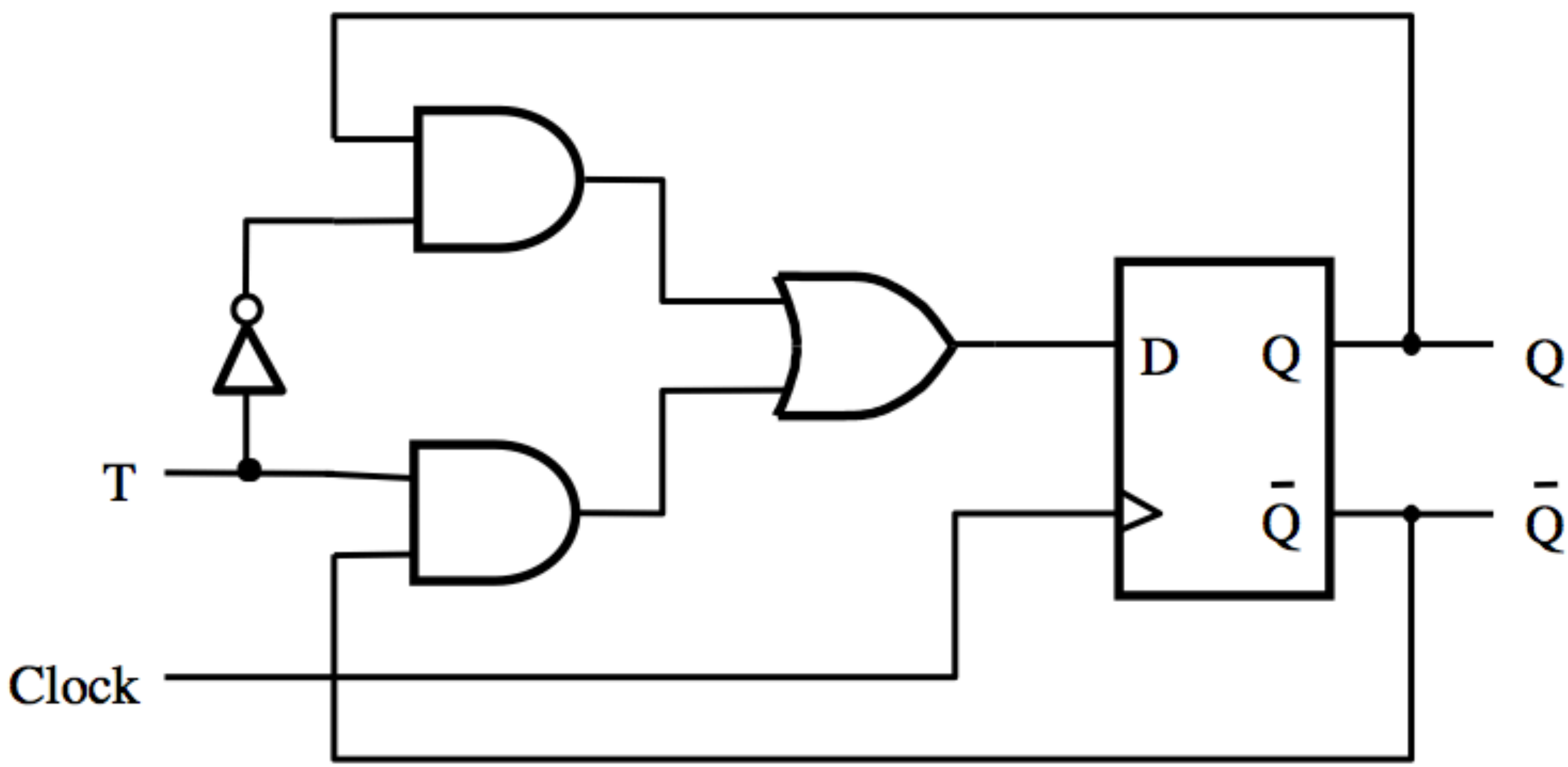
[Figure 5.22 from the textbook]

Inclusion of Enable and Clear capability



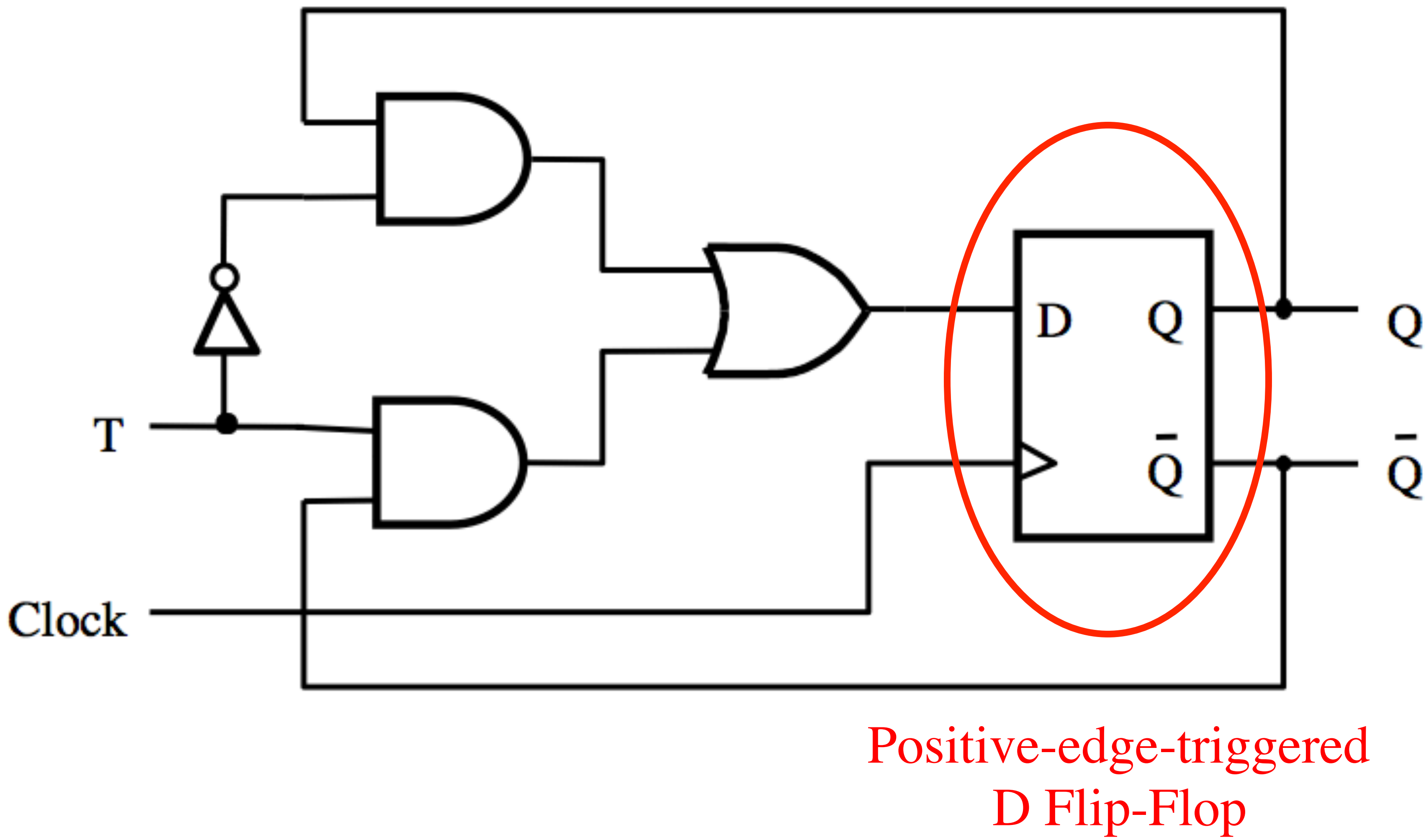
[Figure 5.22 from the textbook]

T Flip-Flop



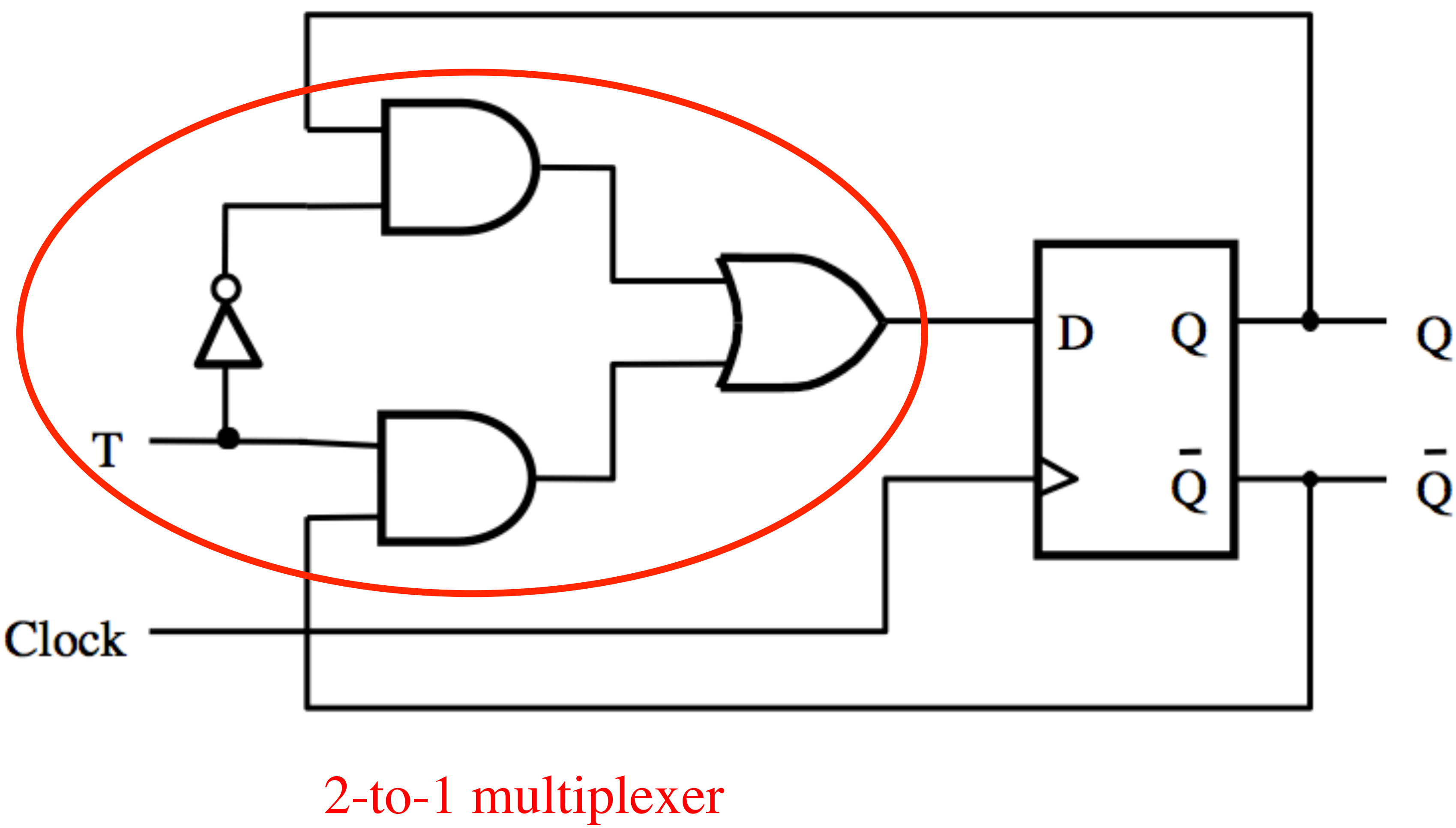
[Figure 5.15a from the textbook]

T Flip-Flop



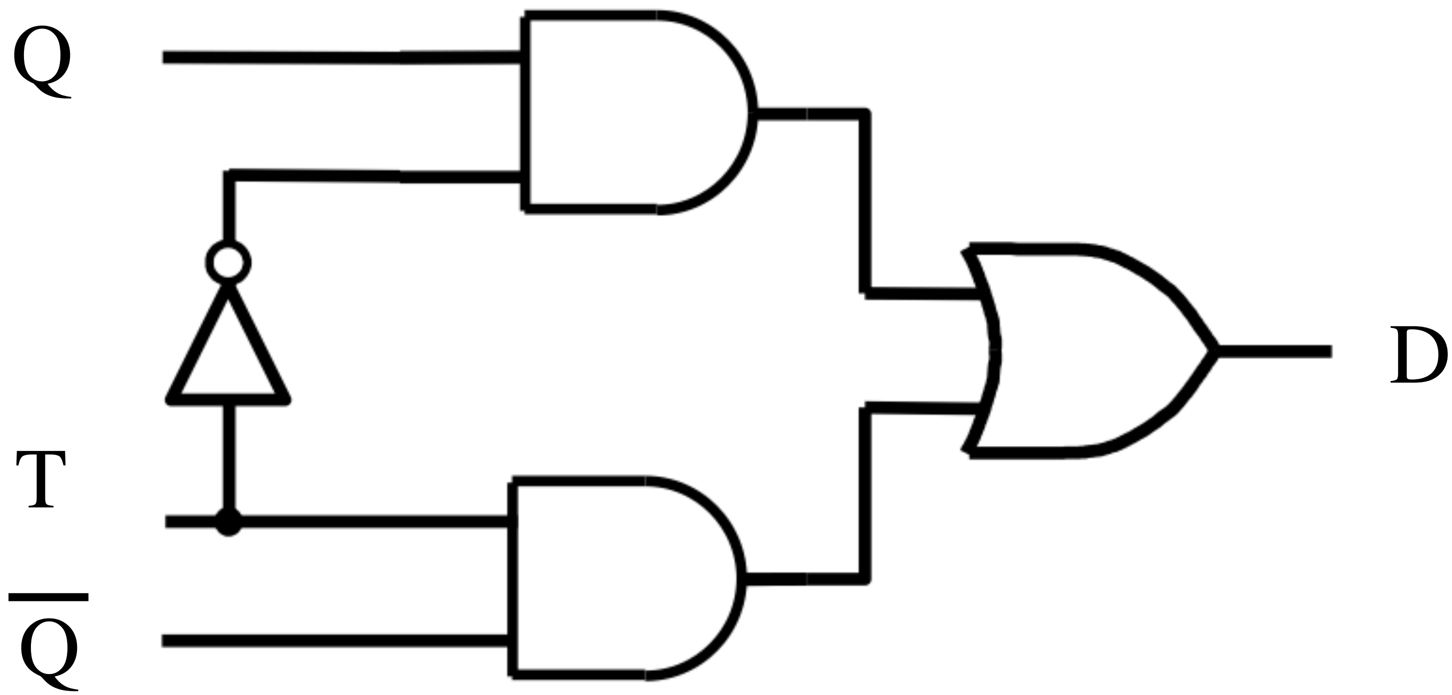
[Figure 5.15a from the textbook]

T Flip-Flop

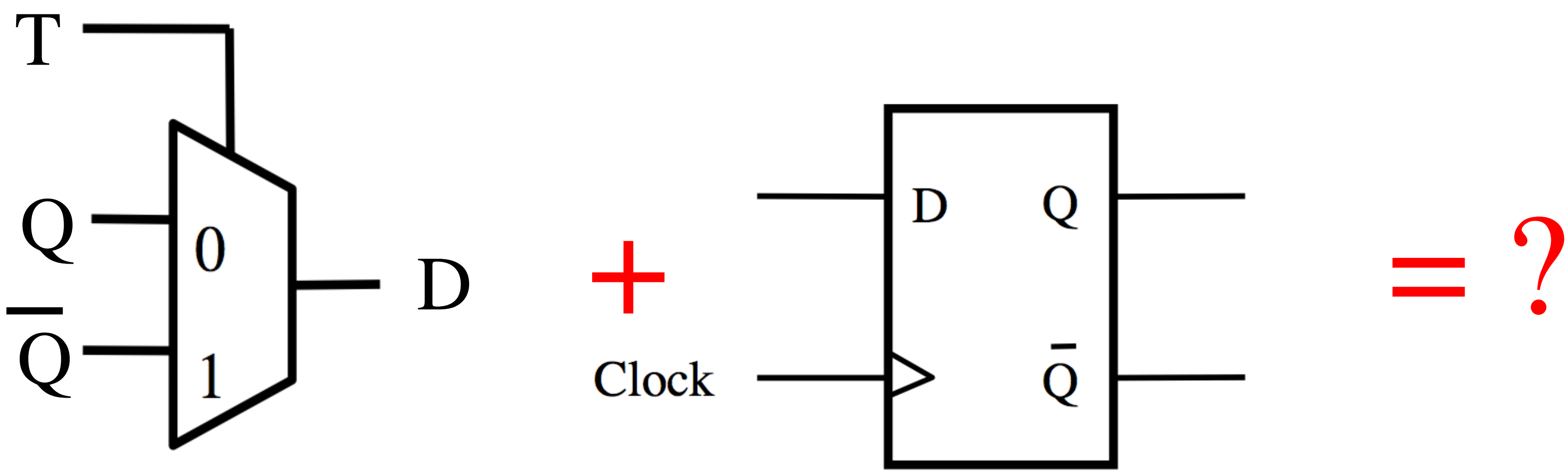


[Figure 5.15a from the textbook]

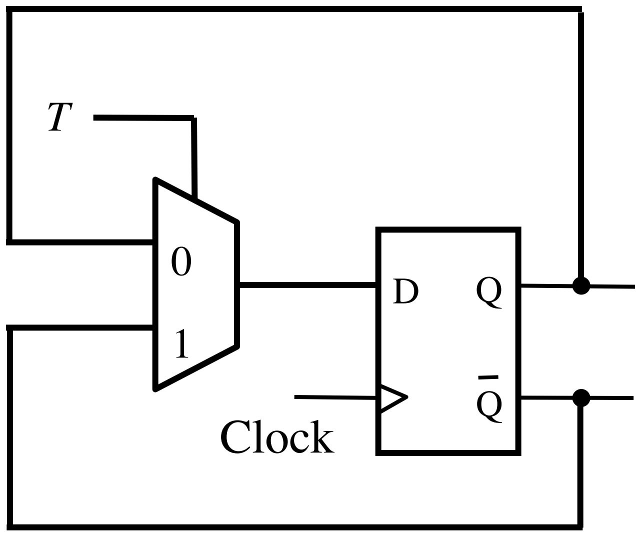
2-to-1 Multiplexer



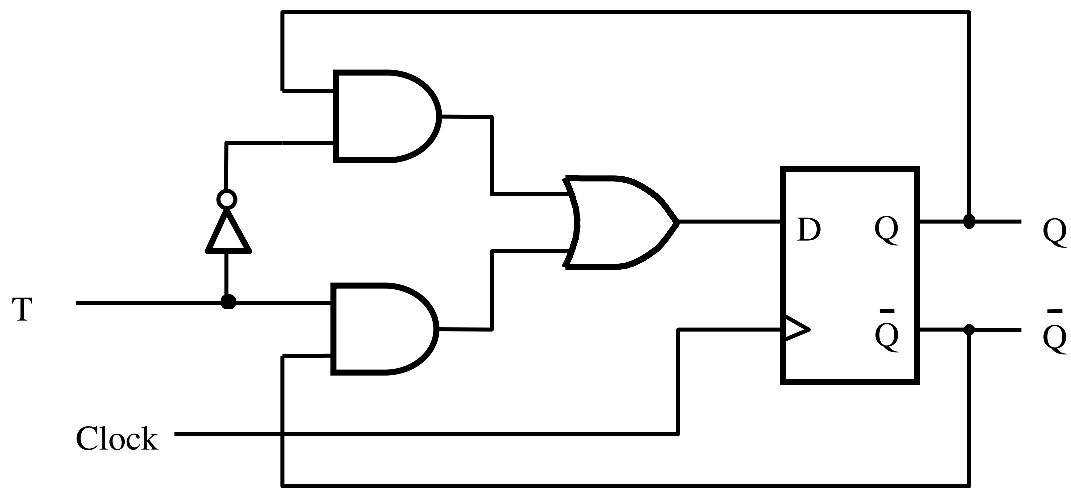
What is this?



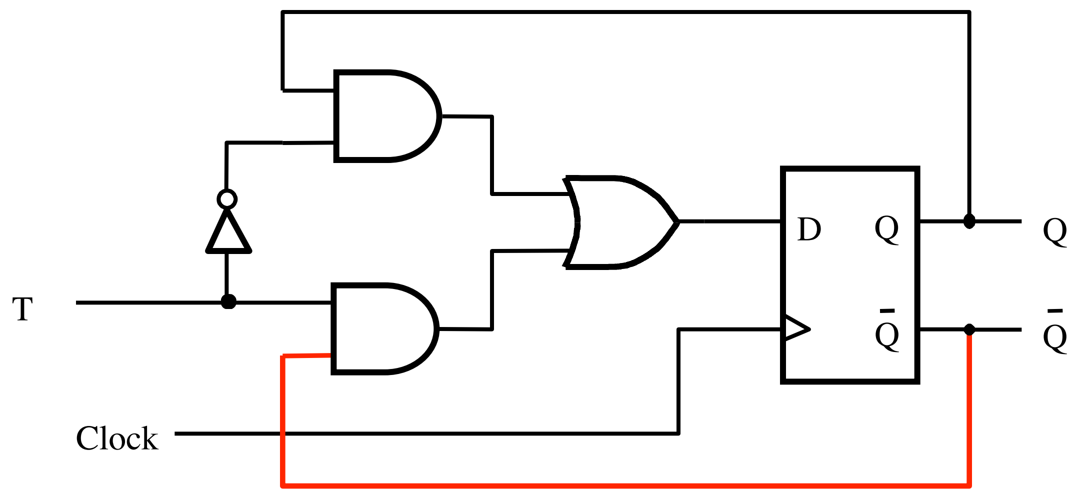
T Flip-Flop



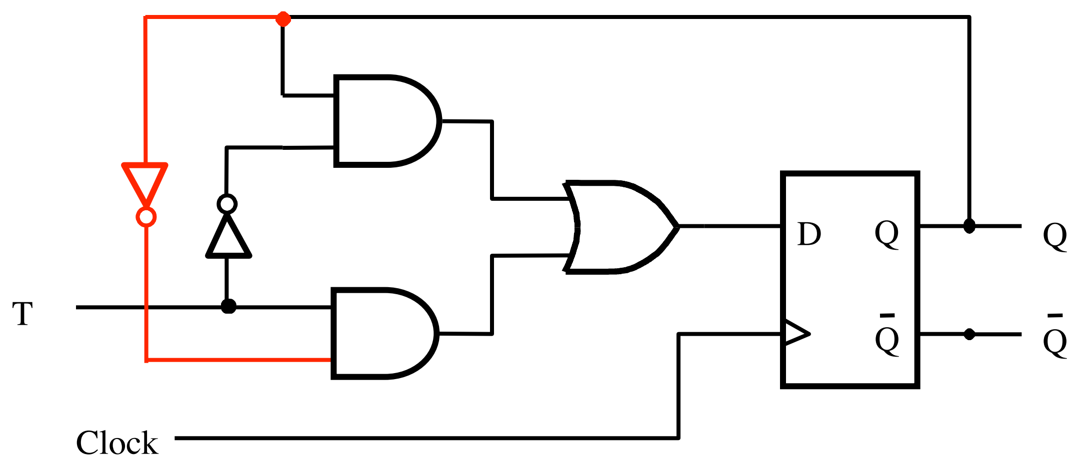
T Flip-Flop



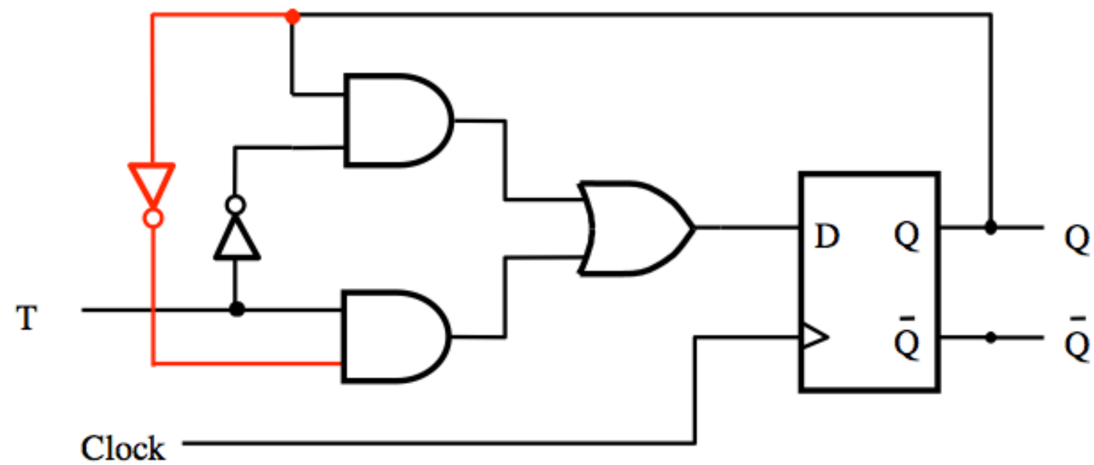
T Flip-Flop

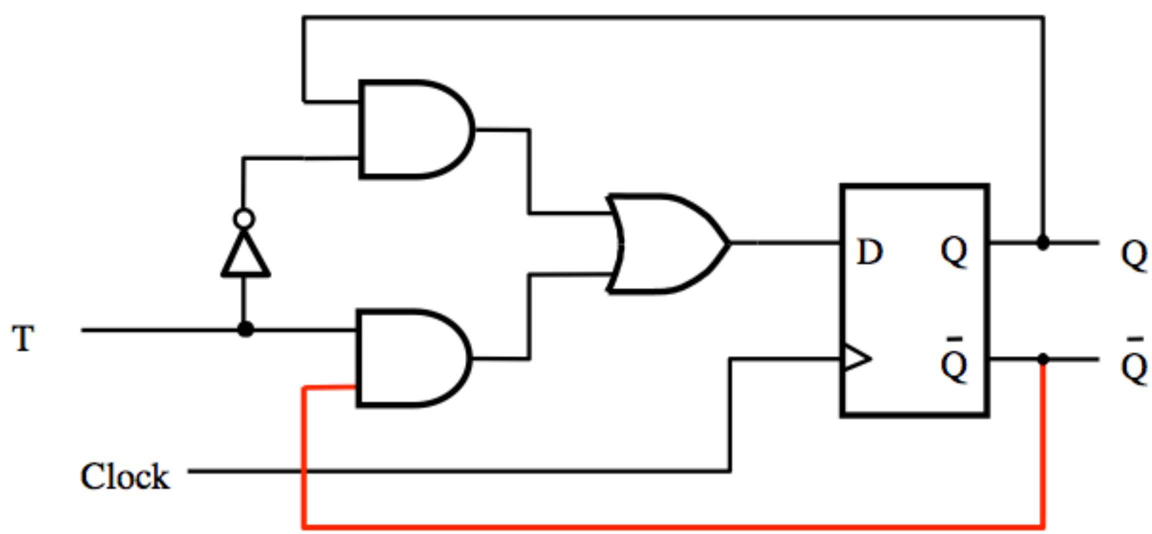


T Flip-Flop

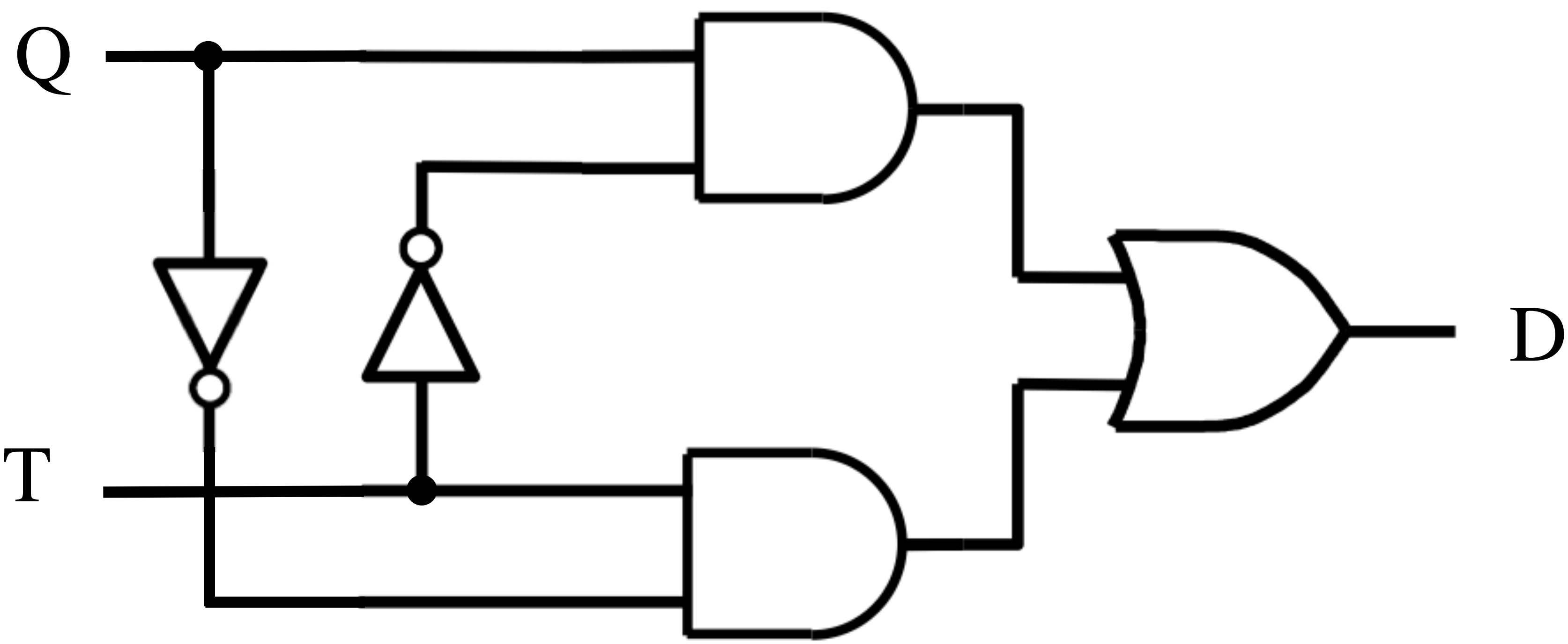


These two circuits are equivalent

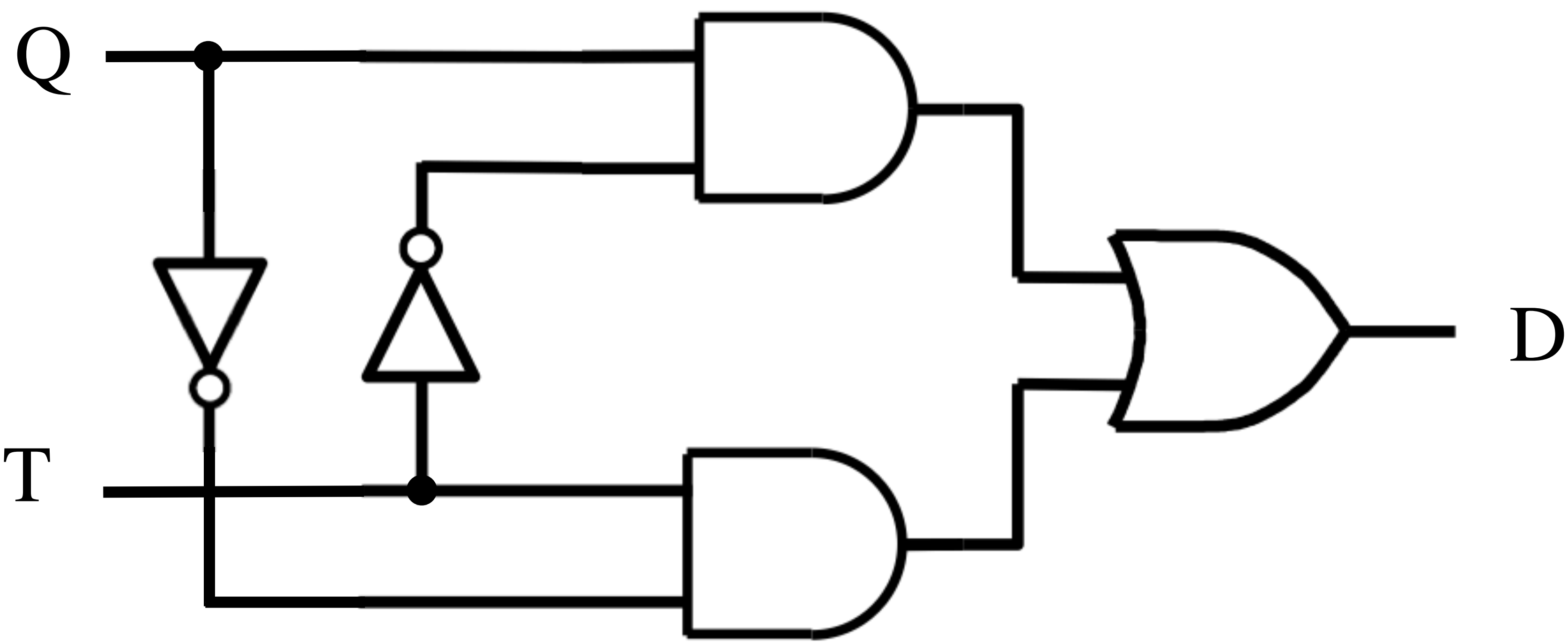




What is this?

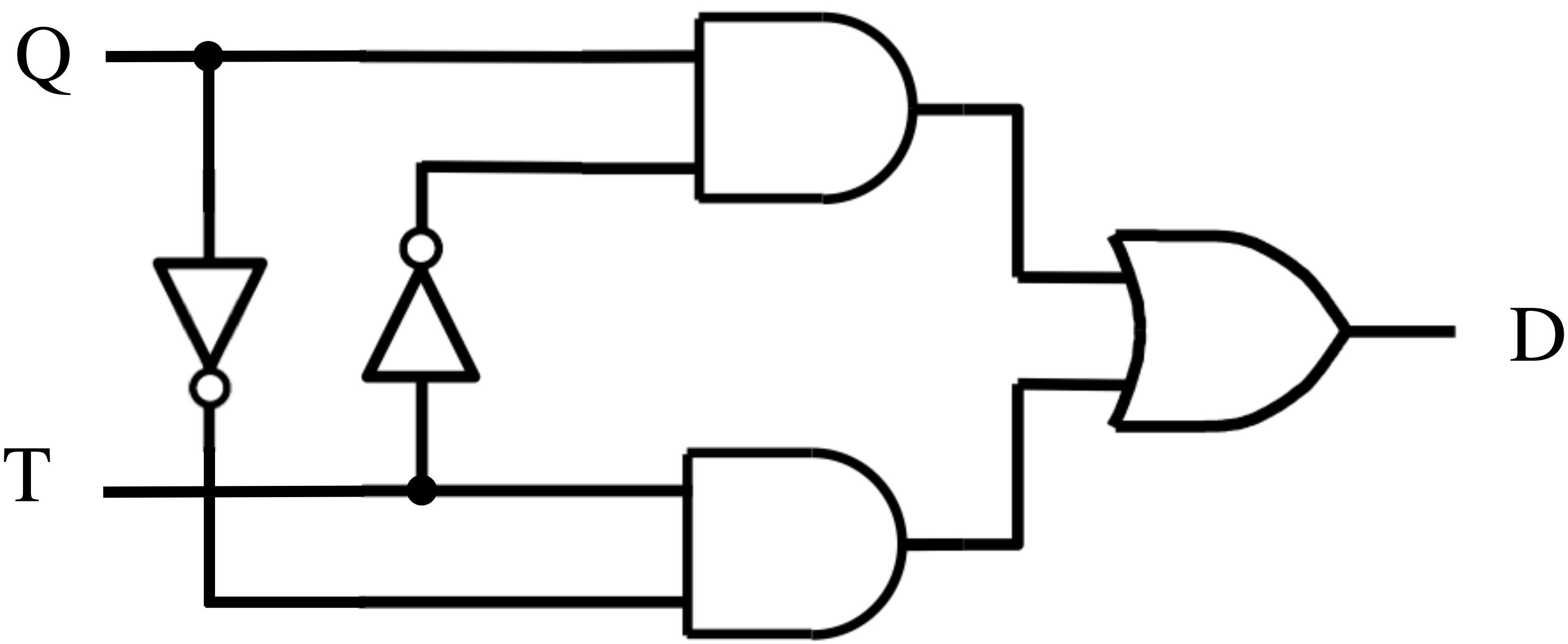


What is this?



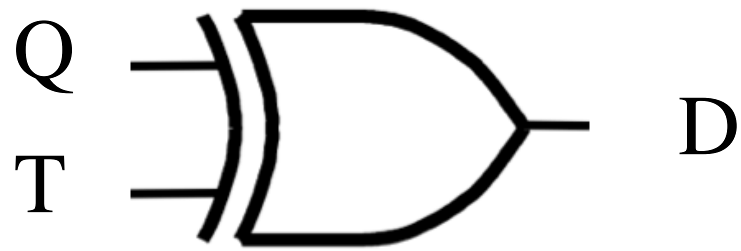
$$D = Q\overline{T} + \overline{Q}T$$

What is this?



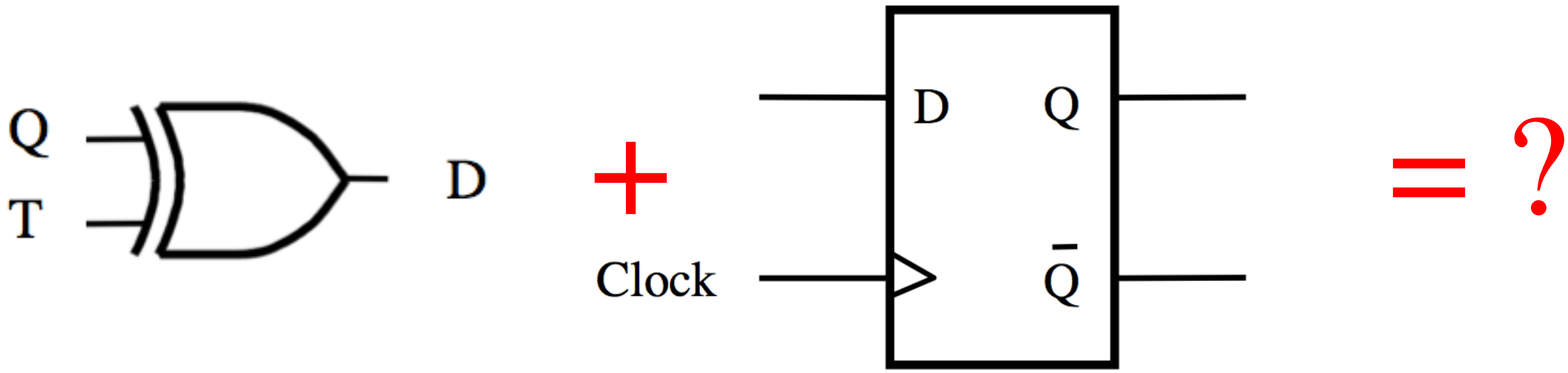
$$D = Q \oplus T$$

What is this?

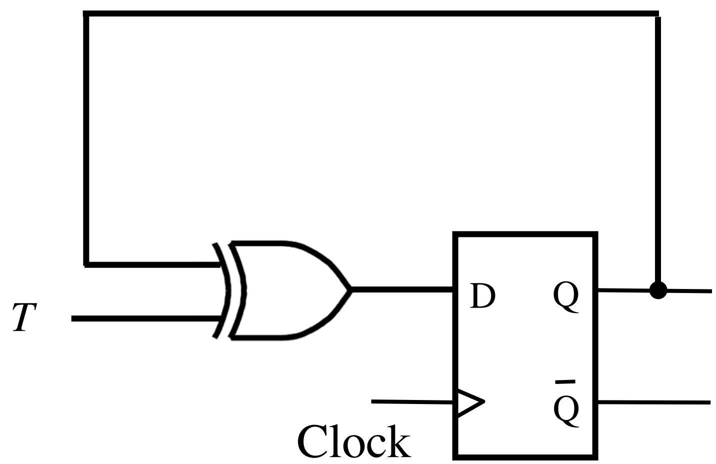


$$D = Q \oplus T$$

What is this?

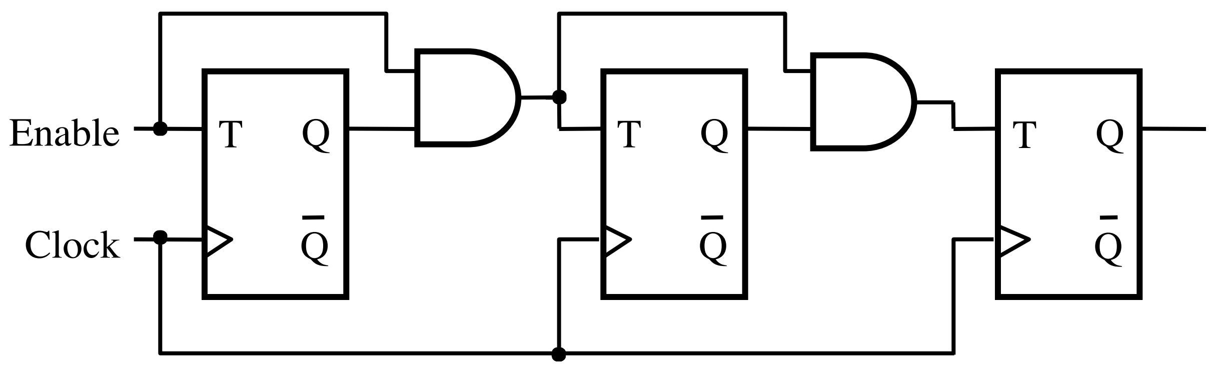


T Flip-Flop

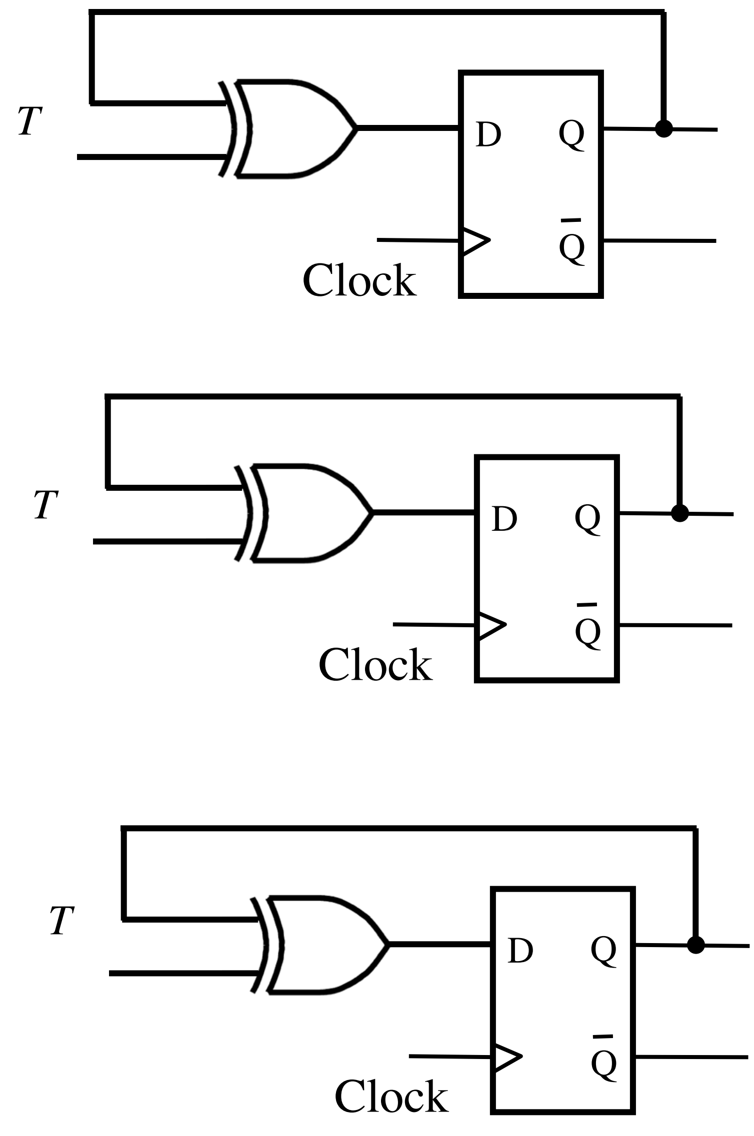


Synchronous Counter with D Flip-Flops

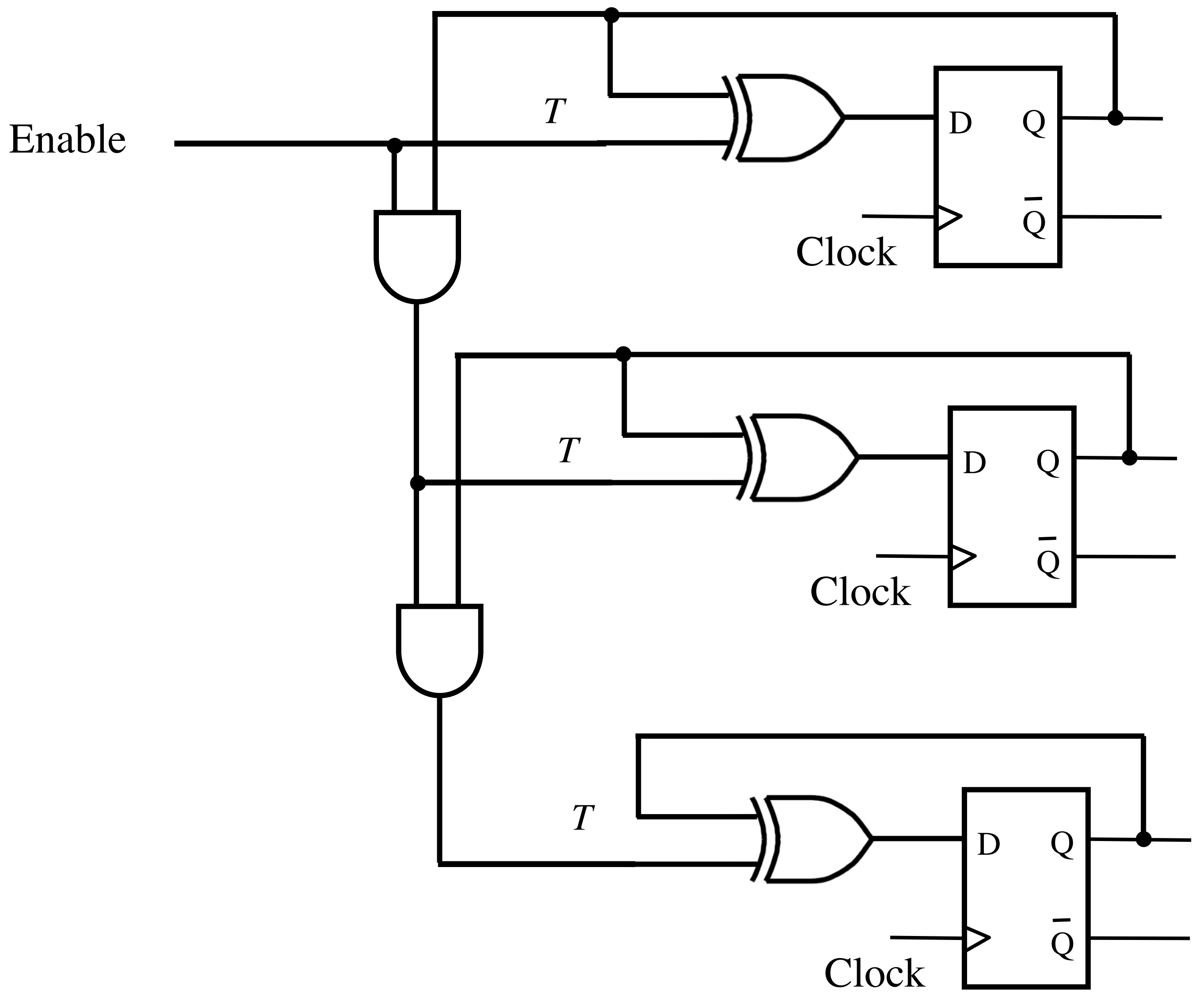
A three-bit up-counter with T flip-flops



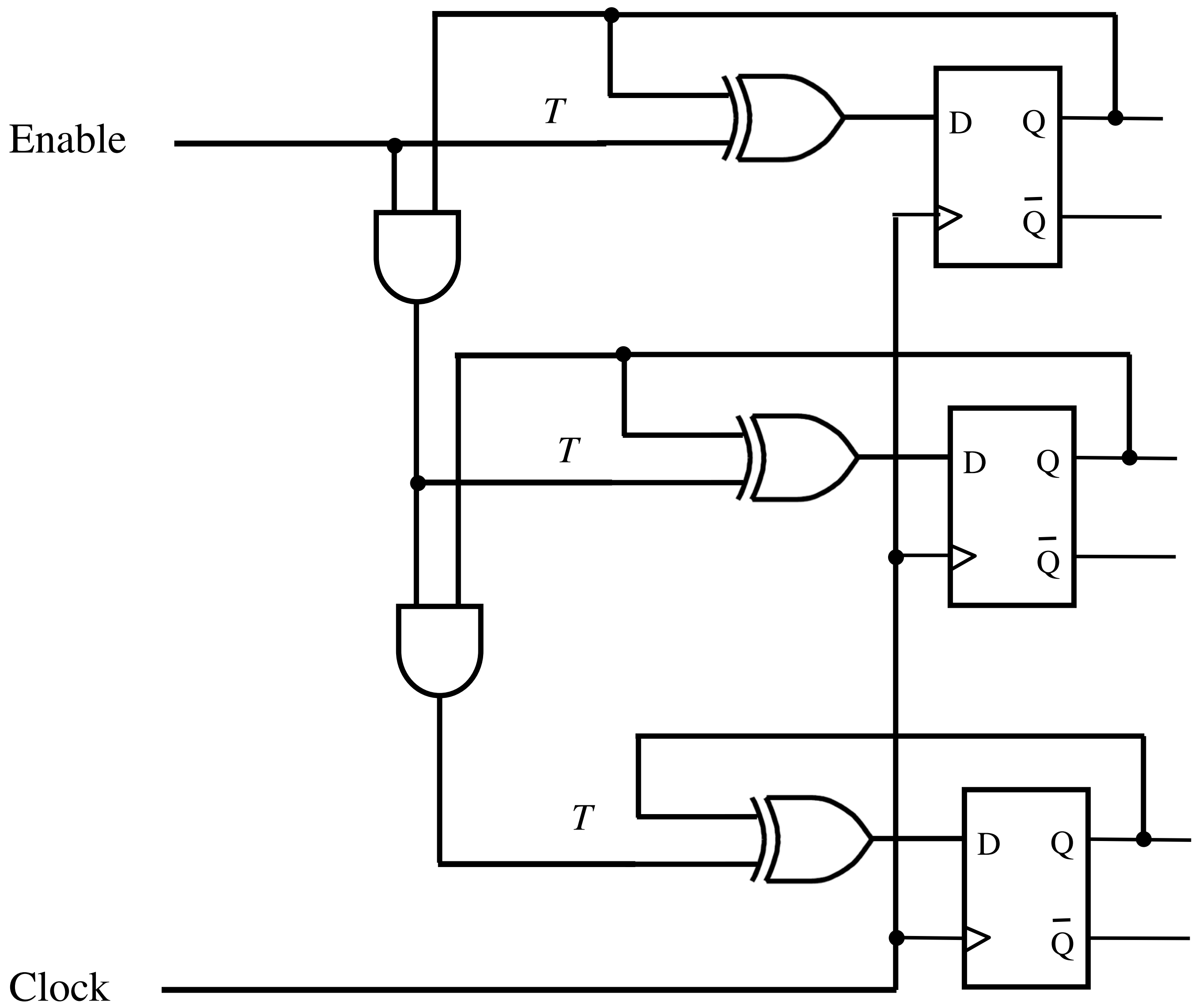
A three-bit up-counter with D flip-flops



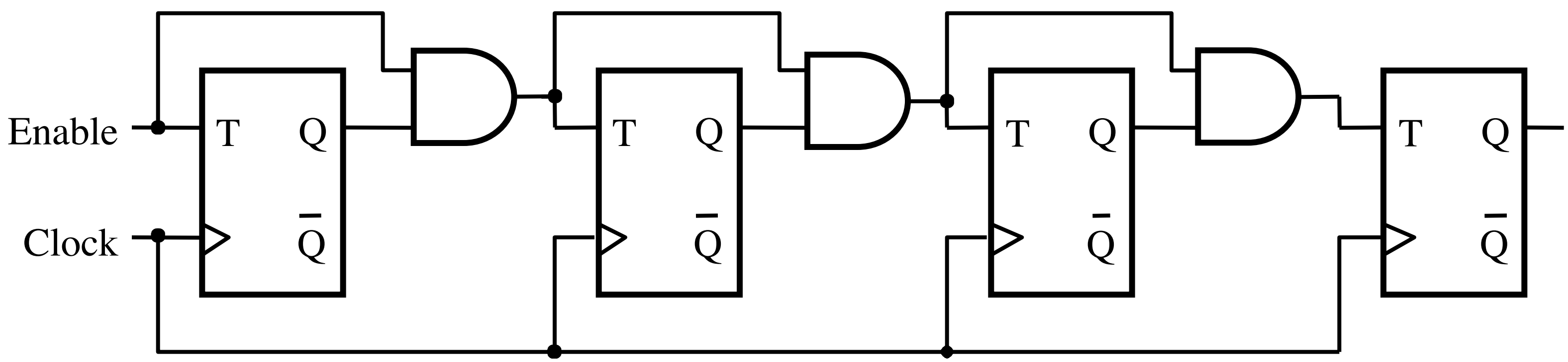
A three-bit up-counter with D flip-flops



A three-bit up-counter with D flip-flops

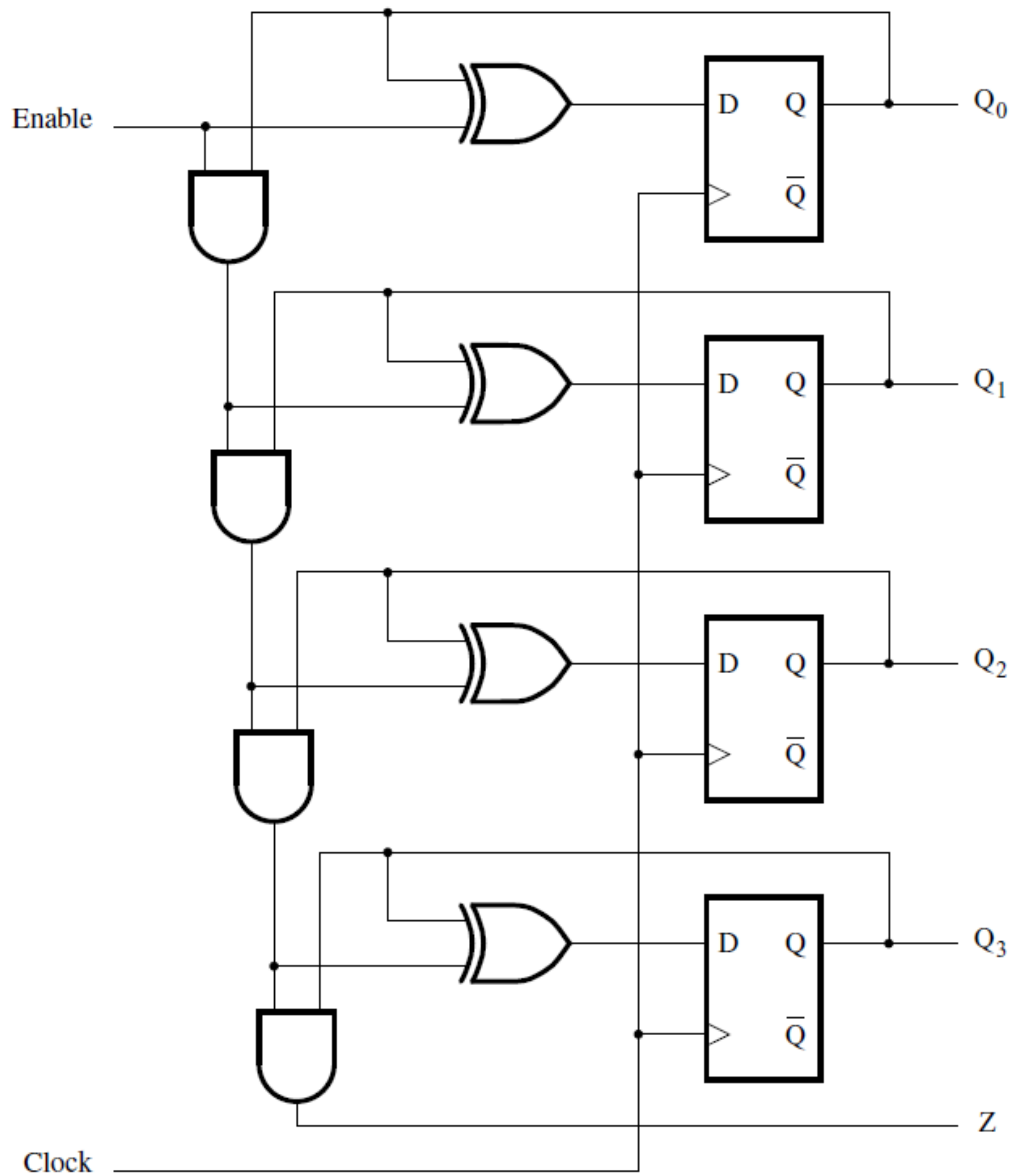


A four-bit up-counter with T flip-flops



[Figure 5.22 from the textbook (Modified)]

A four-bit up-counter with D flip-flops



[Figure 5.23 from the textbook]

End of Mini Review

Goal

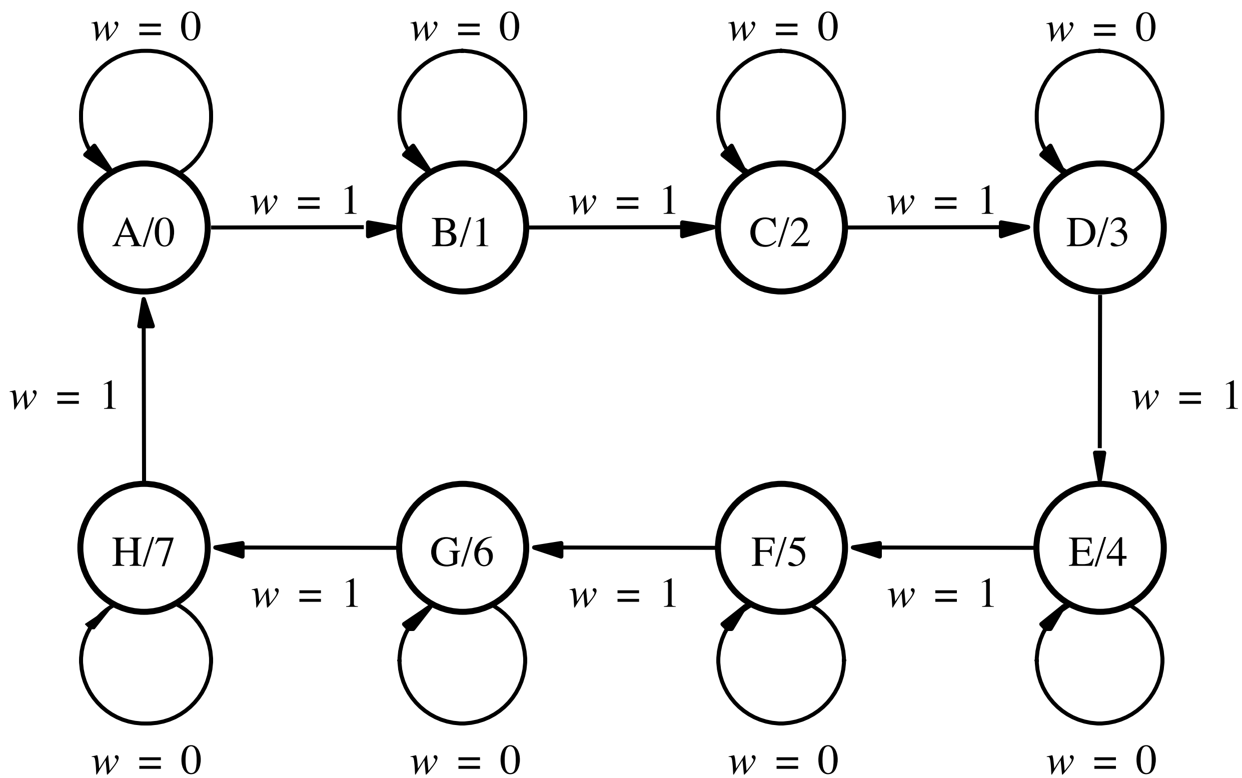
- **Implement a modulo-8 counter using the sequential circuit approach**

- **In other words, the counting sequence must be**

  0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, …

- **The count changes based on the input signal w:**
  - **If w=0, then the count remains the same**
  - **If w=1, then the count is advanced by one**

State diagram for the counter



[Figure 6.60 from the textbook]

State table for the counter

Present state	Next state		Output
	$w = 0$	$w = 1$	
A	A	B	0
B	B	C	1
C	C	D	2
D	D	E	3
E	E	F	4
F	F	G	5
G	G	H	6
H	H	A	7

[Figure 6.61 from the textbook]

State-assigned table for the counter

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	000	001	000
B	001	001	010	001
C	010	010	011	010
D	011	011	100	011
E	100	100	101	100
F	101	101	110	101
G	110	110	111	110
H	111	111	000	111

[Figure 6.62 from the textbook]

K-map for Y_0

	Present state $y_2y_1y_0$	Next state		Count $z_2z_1z_0$
		$w = 0$	$w = 1$	
		$Y_2Y_1Y_0$	$Y_2Y_1Y_0$	
A	000	000	001	000
B	001	001	010	001
C	010	010	011	010
D	011	011	100	011
E	100	100	101	100
F	101	101	110	101
G	110	110	111	110
H	111	111	000	111

wy_2 \ y_1y_0	00	01	11	10
00				
01				
11				
10				

K-map for Y_0

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	1	000
B	001	1	0	001
C	010	0	1	010
D	011	1	0	011
E	100	0	1	100
F	101	1	0	101
G	110	0	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00				
01				
11				
10				

K-map for Y_0

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	1	000
B	001	1	0	001
C	010	0	1	010
D	011	1	0	011
E	100	0	1	100
F	101	1	0	101
G	110	0	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

K-map for Y_0

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	1	000
B	001	1	0	001
C	010	0	1	010
D	011	1	0	011
E	100	0	1	100
F	101	1	0	101
G	110	0	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$$Y_0 = \bar{w}y_0 + w\bar{y}_0$$

K-map for Y_1

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	000	001	000
B	001	001	010	001
C	010	010	011	010
D	011	011	100	011
E	100	100	101	100
F	101	101	110	101
G	110	110	111	110
H	111	111	000	111

wy_2 \ y_1y_0	00	01	11	10
00				
01				
11				
10				

K-map for Y_1

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	0	000
B	001	0	1	001
C	010	1	1	010
D	011	1	0	011
E	100	0	0	100
F	101	0	1	101
G	110	1	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00				
01				
11				
10				

K-map for Y_1

	Present state $y_2y_1y_0$	Next state $w=0$ $Y_2Y_1Y_0$	Next state $w=1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	0	000
B	001	0	1	001
C	010	1	1	010
D	011	1	0	011
E	100	0	0	100
F	101	0	1	101
G	110	1	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	1	0	1

K-map for Y_1

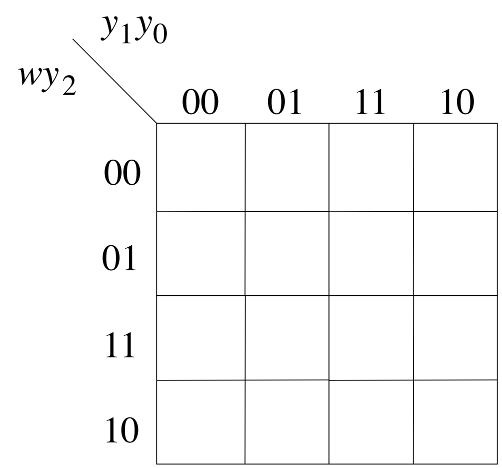
	Present state $y_2 y_1 y_0$	Next state $w = 0$ $Y_2 Y_1 Y_0$	Next state $w = 1$ $Y_2 Y_1 Y_0$	Count $z_2 z_1 z_0$
A	000	0	0	000
B	001	0	1	001
C	010	1	1	010
D	011	1	0	011
E	100	0	0	100
F	101	0	1	101
G	110	1	1	110
H	111	1	0	111

wy_2 \ $y_1 y_0$	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	1	0	1

$$Y_1 = \bar{w} y_1 + y_1 \bar{y}_0 + w y_0 \bar{y}_1$$

K-map for Y_2

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	000	001	000
B	001	001	010	001
C	010	010	011	010
D	011	011	100	011
E	100	100	101	100
F	101	101	110	101
G	110	110	111	110
H	111	111	000	111



K-map for Y_2

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	0	000
B	001	0	0	001
C	010	0	0	010
D	011	0	1	011
E	100	1	1	100
F	101	1	1	101
G	110	1	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00				
01				
11				
10				

K-map for Y_2

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	0	000
B	001	0	0	001
C	010	0	0	010
D	011	0	1	011
E	100	1	1	100
F	101	1	1	101
G	110	1	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	0	1
10	0	0	1	0

K-map for Y_2

	Present state $y_2y_1y_0$	Next state $w = 0$ $Y_2Y_1Y_0$	Next state $w = 1$ $Y_2Y_1Y_0$	Count $z_2z_1z_0$
A	000	0	0	000
B	001	0	0	001
C	010	0	0	010
D	011	0	1	011
E	100	1	1	100
F	101	1	1	101
G	110	1	1	110
H	111	1	0	111

wy_2 \ y_1y_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	0	1
10	0	0	1	0

$$Y_2 = \bar{w}y_2 + \bar{y}_0y_2 + \bar{y}_1y_2 + wy_0y_1\bar{y}_2$$

Karnaugh maps for D flip-flops for the counter

wy_2 \ y_1y_0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$$Y_0 = \bar{w}y_0 + w\bar{y}_0$$

wy_2 \ y_1y_0	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	1	0	1

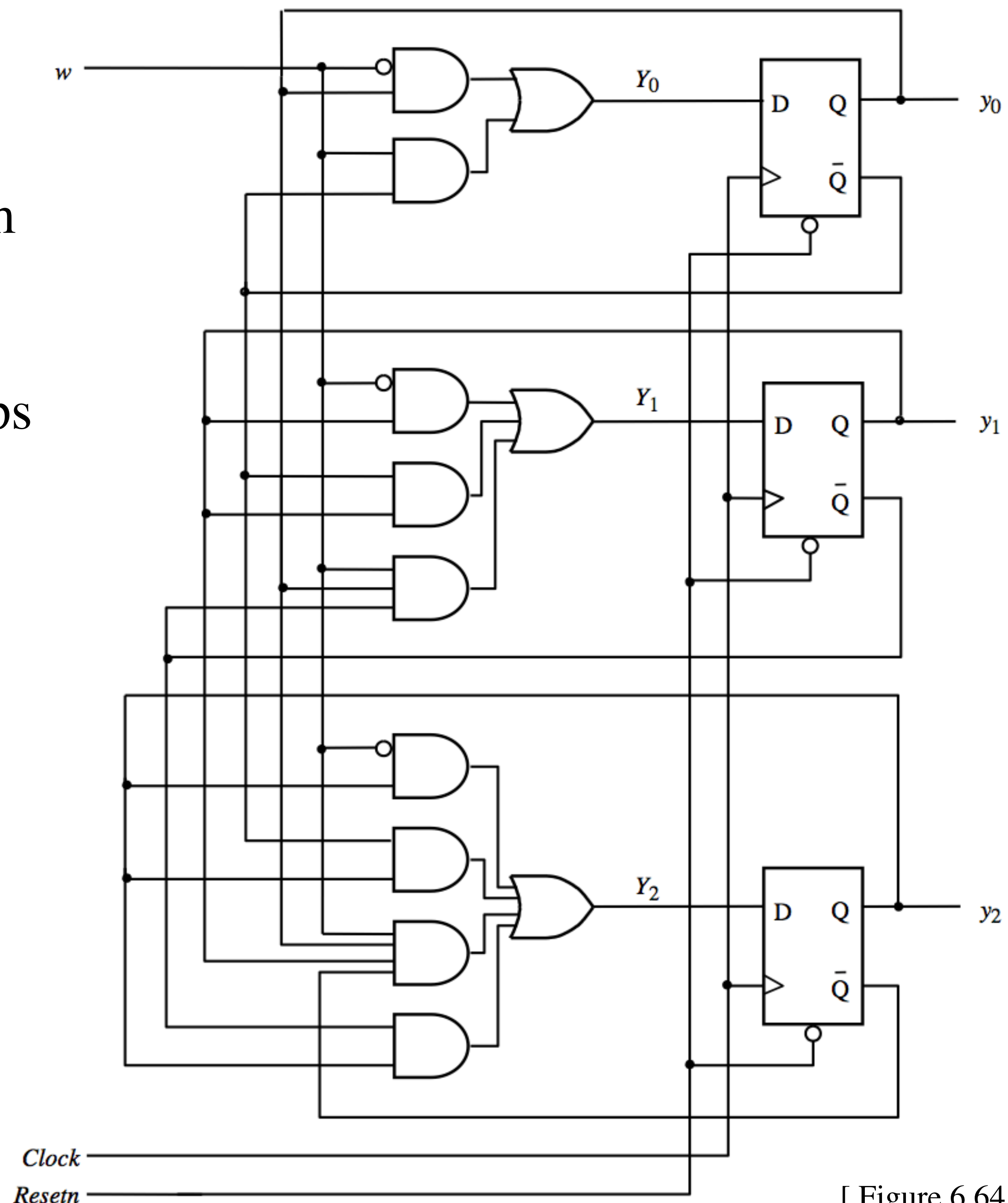
$$Y_1 = \bar{w}y_1 + y_1\bar{y}_0 + wy_0\bar{y}_1$$

wy_2 \ y_1y_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	0	1
10	0	0	1	0

$$Y_2 = \bar{w}y_2 + \bar{y}_0y_2 + \bar{y}_1y_2 + wy_0y_1\bar{y}_2$$

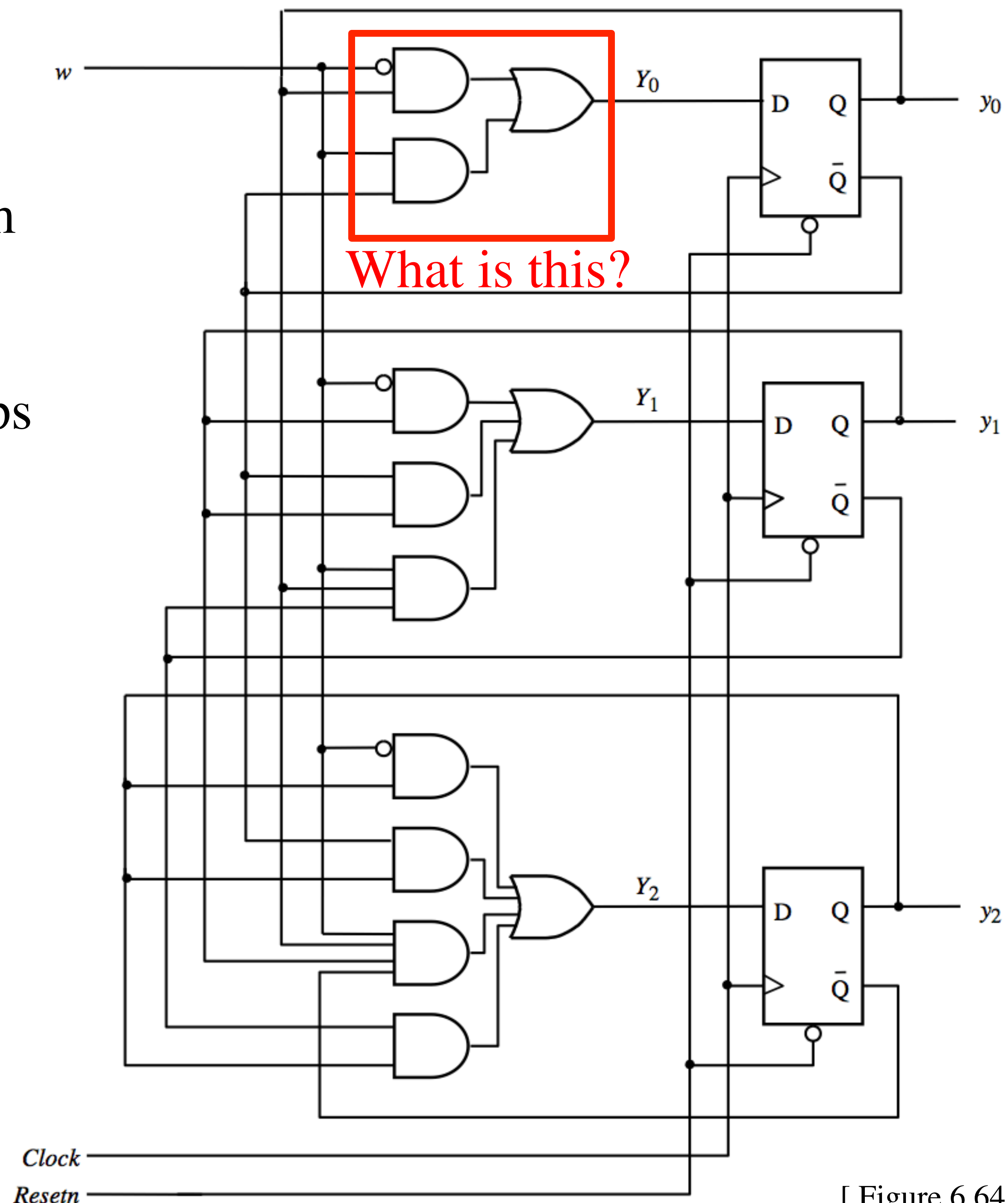
[Figure 6.63 from the textbook]

Circuit diagram for the counter implemented with D flip-flops



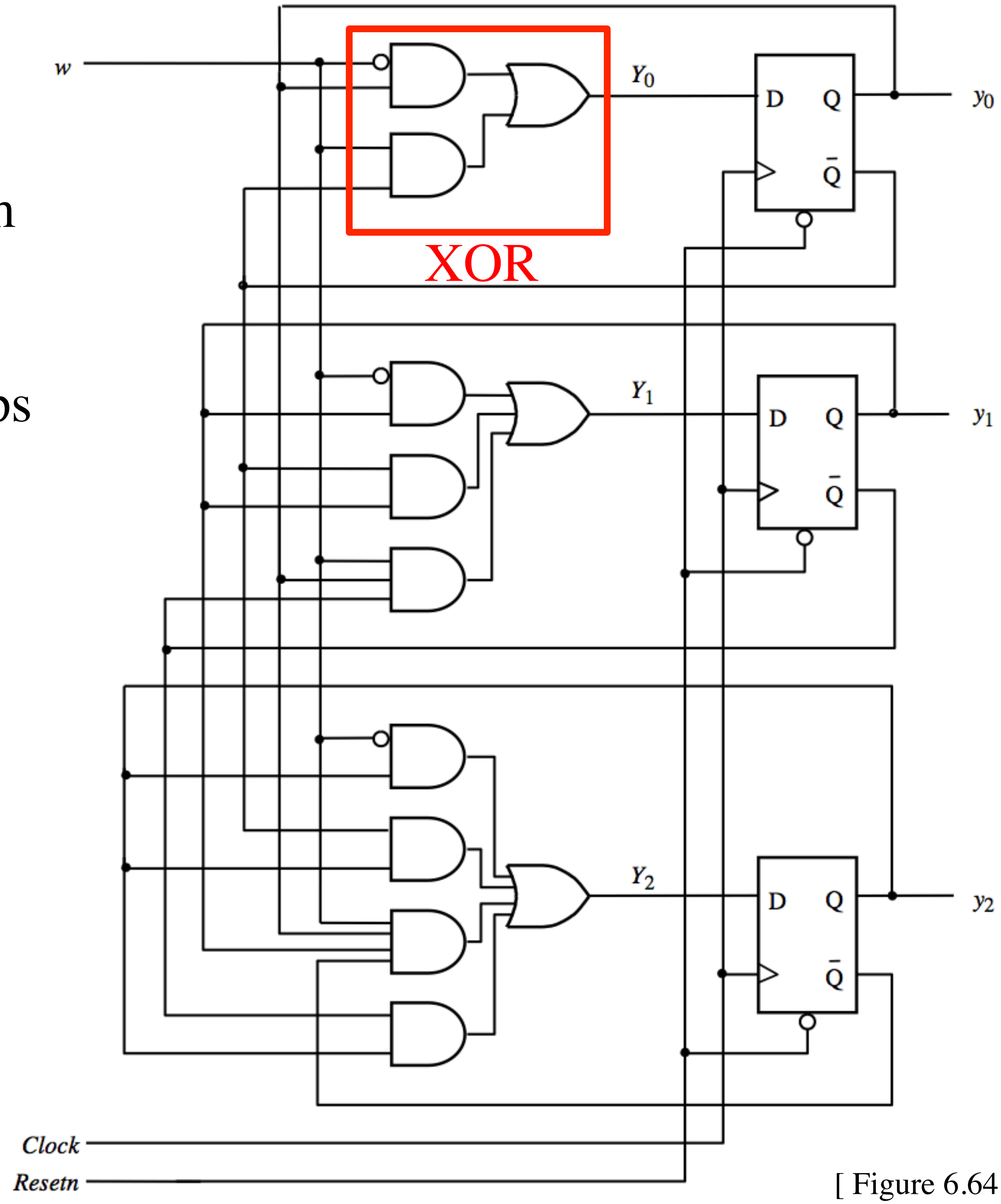
[Figure 6.64 from the textbook]

Circuit diagram for the counter implemented with D flip-flops



[Figure 6.64 from the textbook]

Circuit diagram for the counter implemented with D flip-flops



[Figure 6.64 from the textbook]

We can simplify all three expressions

$$Y_0 = \bar{w}y_0 + w\bar{y}_0$$

$$Y_1 = \bar{w}y_1 + y_1\bar{y}_0 + wy_0\bar{y}_1$$

$$Y_2 = \bar{w}y_2 + \bar{y}_0y_2 + \bar{y}_1y_2 + wy_0y_1\bar{y}_2$$

We can simplify all three expressions

$$Y_0 = \bar{w}y_0 + w\bar{y}_0$$

$$\begin{aligned} D_0 &= \overline{w}y_0 + w\overline{y}_0 \\ &= w \oplus y_0 \end{aligned}$$

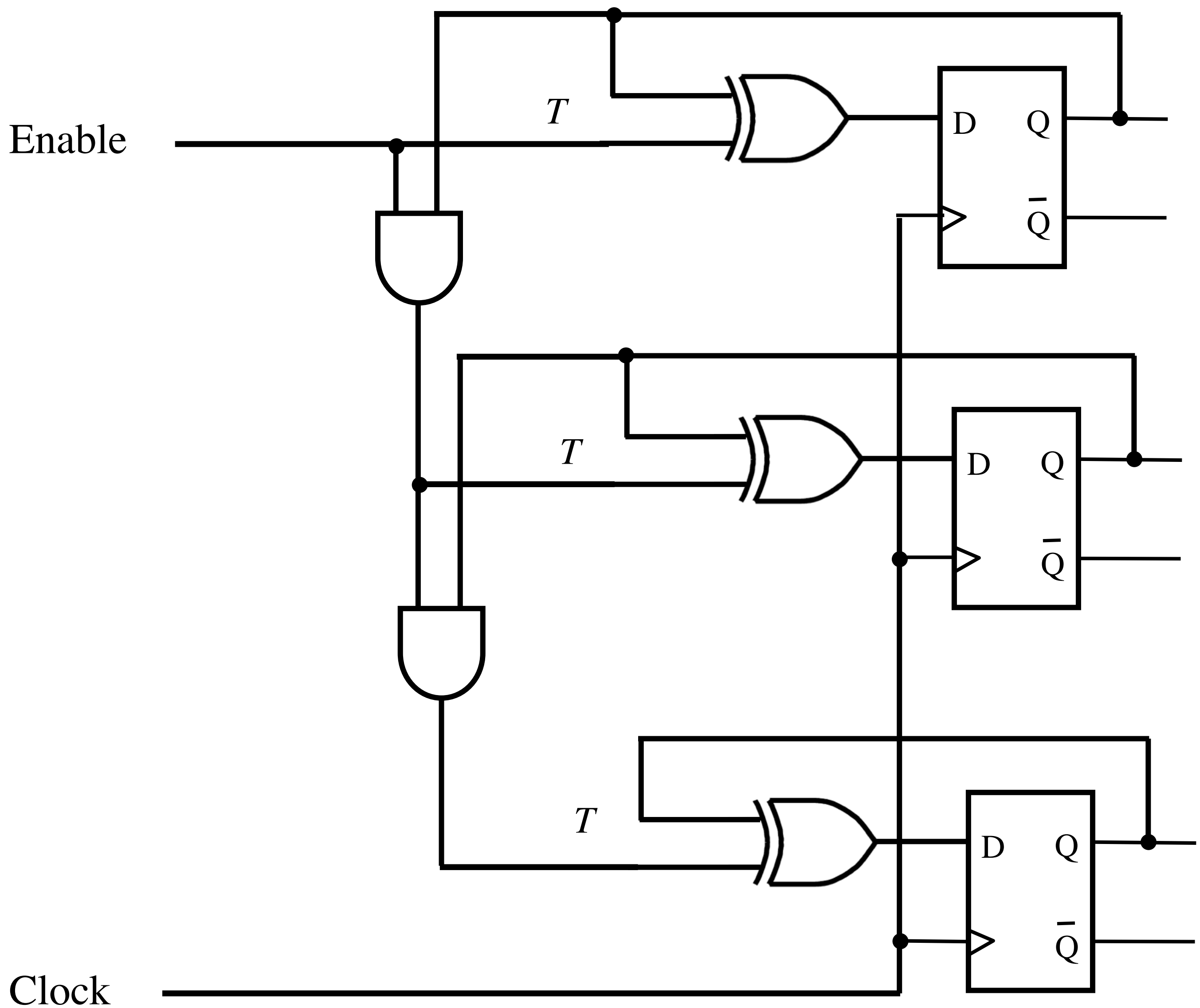
$$Y_1 = \bar{w}y_1 + y_1\bar{y}_0 + wy_0\bar{y}_1$$

$$\begin{aligned} D_1 &= \overline{w}y_1 + y_1\overline{y}_0 + wy_0\overline{y}_1 \\ &= (\overline{w} + \overline{y}_0)y_1 + wy_0\overline{y}_1 \\ &= \overline{wy_0}y_1 + wy_0\overline{y}_1 \\ &= wy_0 \oplus y_1 \end{aligned}$$

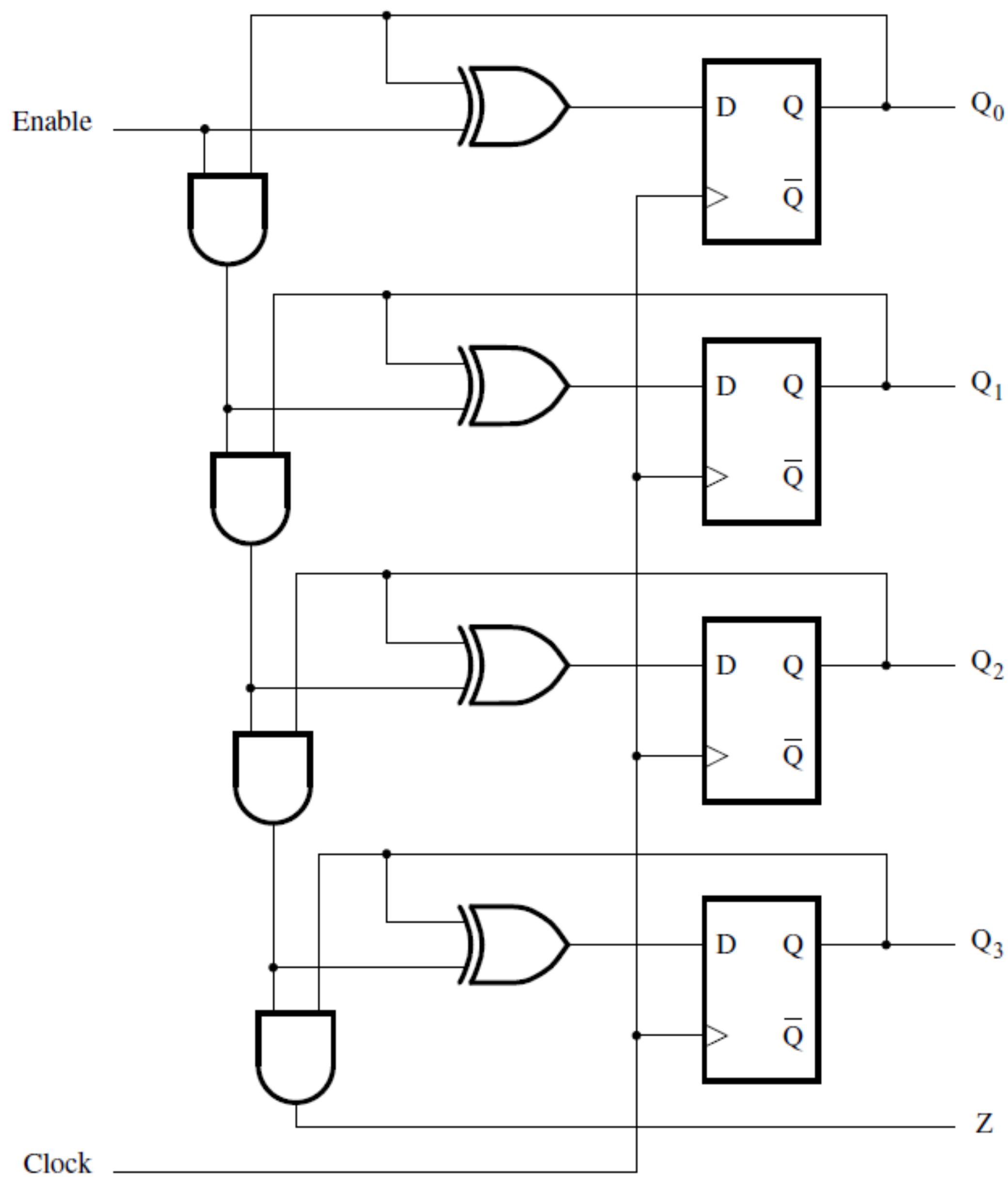
$$Y_2 = \bar{w}y_2 + \bar{y}_0y_2 + \bar{y}_1y_2 + wy_0y_1\bar{y}_2$$

$$\begin{aligned} D_2 &= \overline{w}y_2 + \overline{y}_0y_2 + \overline{y}_1y_2 + wy_0y_1\overline{y}_2 \\ &= (\overline{w} + \overline{y}_0 + \overline{y}_1)y_2 + wy_0y_1\overline{y}_2 \\ &= \overline{wy_0y_1}y_2 + wy_0y_1\overline{y}_2 \\ &= wy_0y_1 \oplus y_2 \end{aligned}$$

A three-bit counter with D flip-flops



A four-bit counter with D flip-flops



[Figure 5.23 from the textbook]

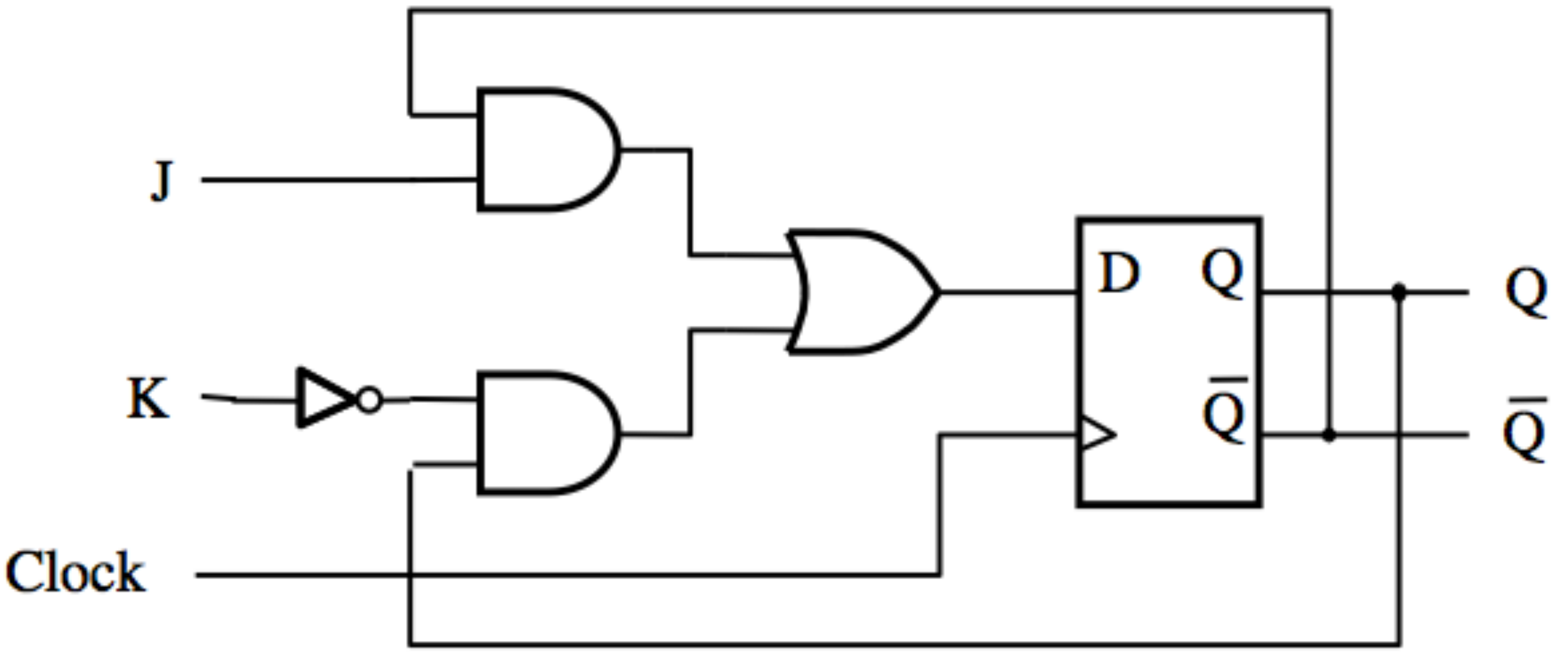
Summary

- The up-counters that we studied in Chapter 5 can now be derived using the sequential circuit approach

- We get the same circuit diagrams as before

Example 2:
Implement a modulo-8 counter using JK Flip-Flops

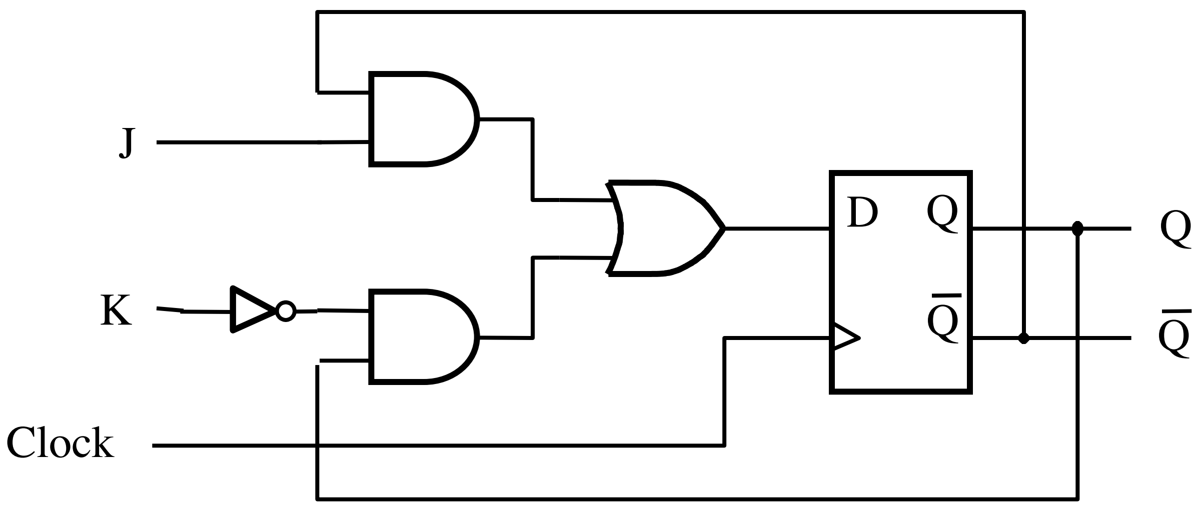
JK Flip-Flop



$$D = J\overline{Q} + \overline{K}Q$$

[Figure 5.16a from the textbook]

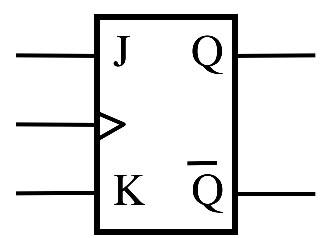
JK Flip-Flop



(a) Circuit

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}(t)$

(b) Truth table



(c) Graphical symbol

[Figure 5.16 from the textbook]

JK Flip-Flop (How it Works)

A versatile circuit that can be used both as a SR flip-flop and as a T flip flop

If J=0 and K =0 it stays in the same state

Just like SR It can be set and reset

J=S and K=R

If J=K then it behaves as a T flip-flop

Transition Rules in terms of J and K

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

Current State of the Flip-flop: Q(t)

Next State of the Flip-flop: Q(t+1)

- **From 0 to 0** **J=0 and K= d**
- **From 0 to 1** **J=1 and K= d**
- **From 1 to 0** **J=d and K= 1**
- **From 1 to 1** **J=d and K= 0**

Transition Rules in terms of J and K

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}$(t)

Current State of the Flip-flop: Q(t)

Next State of the Flip-flop: Q(t+1)

- **From 0 to 0** **J=0 and K= d**
- **From 0 to 1** **J=1 and K= d**
- **From 1 to 0** **J=d and K= 1**
- **From 1 to 1** **J=d and K= 0**

Q(t) → Q(t+1)	J K
0 → 0	0 d
0 → 1	1 d
1 → 0	d 1
1 → 1	d 0

Excitation table for the counter with JK flip-flops

	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

[Figure 6.65 from the textbook]

Excitation table for the counter with JK flip-flops

	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

$Q(t) \rightarrow Q(t+1)$	J K
$0 \rightarrow 0$	0 d
$0 \rightarrow 1$	1 d
$1 \rightarrow 0$	d 1
$1 \rightarrow 1$	d 0

[Figure 6.65 from the textbook]

Karnaugh maps for the first JK flip-flop

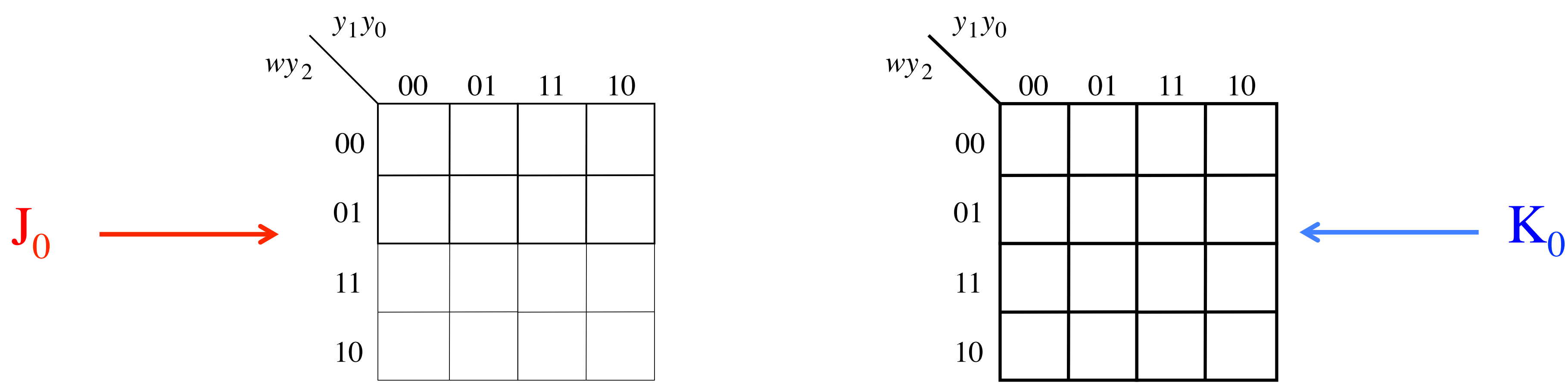
	Present state	Flip-flop inputs								Count
		$w = 0$				$w = 1$				
	$y_2 y_1 y_0$	$Y_2 Y_1 Y_0$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$	$Y_2 Y_1 Y_0$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$	$z_2 z_1 z_0$
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

wy_2 \ $y_1 y_0$	00	01	11	10
00				
01				
11				
10				

wy_2 \ $y_1 y_0$	00	01	11	10
00				
01				
11				
10				

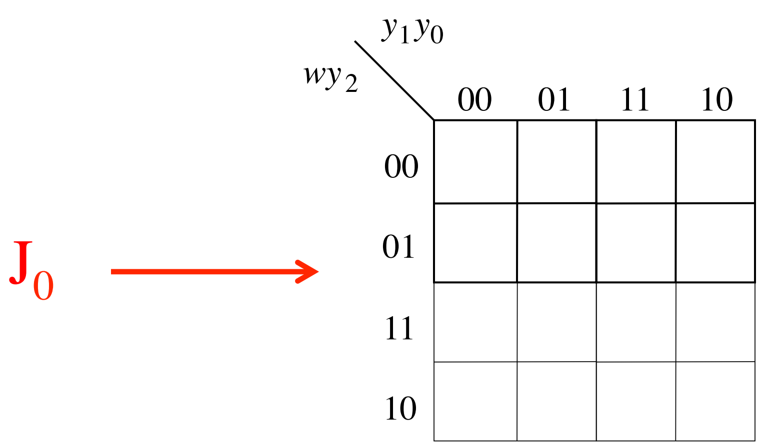
Karnaugh maps for the first JK flip-flop

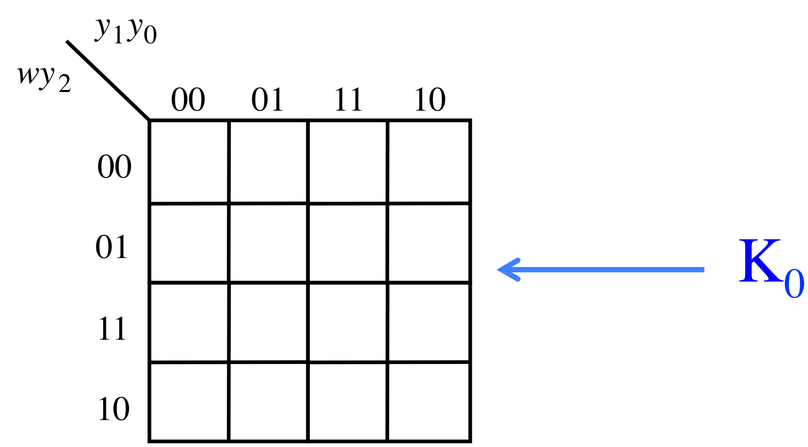
	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111



Karnaugh maps for the first JK flip-flop

	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111





Karnaugh maps for the first JK flip-flop

	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

J_0 →

wy_2 \ y_1y_0	00	01	11	10
00	0	d	d	0
01	0	d	d	0
11	1	d	d	1
10	1	d	d	1

← K_0

wy_2 \ y_1y_0	00	01	11	10
00				
01				
11				
10				

Karnaugh maps for the first JK flip-flop

	Present state	Flip-flop inputs								Count
		$w = 0$				$w = 1$				
	$y_2y_1y_0$	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$z_2z_1z_0$
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

J_0 →

wy_2 \ y_1y_0	00	01	11	10
00	0	d	d	0
01	0	d	d	0
11	1	d	d	1
10	1	d	d	1

← K_0

wy_2 \ y_1y_0	00	01	11	10
00	d	0	0	d
01	d	0	0	d
11	d	1	1	d
10	d	1	1	d

Karnaugh maps for the first JK flip-flop

	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

J_0

wy_2 \ y_1y_0	00	01	11	10
00	0	d	d	0
01	0	d	d	0
11	1	d	d	1
10	1	d	d	1

K_0

wy_2 \ y_1y_0	00	01	11	10
00	d	0	0	d
01	d	0	0	d
11	d	1	1	d
10	d	1	1	d

Karnaugh maps for the first JK flip-flop

	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

J_0 →

wy_2 \ y_1y_0	00	01	11	10
00	0	d	d	0
01	0	d	d	0
11	1	d	d	1
10	1	d	d	1

$J_0 = w$

← K_0

wy_2 \ y_1y_0	00	01	11	10
00	d	0	0	d
01	d	0	0	d
11	d	1	1	d
10	d	1	1	d

$K_0 = w$

Karnaugh maps for the first JK flip-flop

J_0

wy_2 \ y_1y_0	00	01	11	10
00	0	d	d	0
01	0	d	d	0
11	1	d	d	1
10	1	d	d	1

$J_0 = w$

K_0

wy_2 \ y_1y_0	00	01	11	10
00	d	0	0	d
01	d	0	0	d
11	d	1	1	d
10	d	1	1	d

$K_0 = w$

[Figure 6.66 from the textbook]

Karnaugh maps for the second JK flip-flop

J_1

wy_2 \ y_1y_0	00	01	11	10
00	0	0	d	d
01	0	0	d	d
11	0	1	d	d
10	0	1	d	d

$J_1 = wy_0$

K_1

wy_2 \ y_1y_0	00	01	11	10
00	d	d	0	0
01	d	d	0	0
11	d	d	1	0
10	d	d	1	0

$K_1 = wy_0$

[Figure 6.66 from the textbook]

Karnaugh maps for the third JK flip-flop

J_2

wy_2 \ y_1y_0	00	01	11	10
00	0	0	0	0
01	d	d	d	d
11	d	d	d	d
10	0	0	1	0

$$J_2 = wy_0y_1$$

K_2

wy_2 \ y_1y_0	00	01	11	10
00	d	d	d	d
01	0	0	0	0
11	0	0	1	0
10	d	d	d	d

$$K_2 = wy_0y_1$$

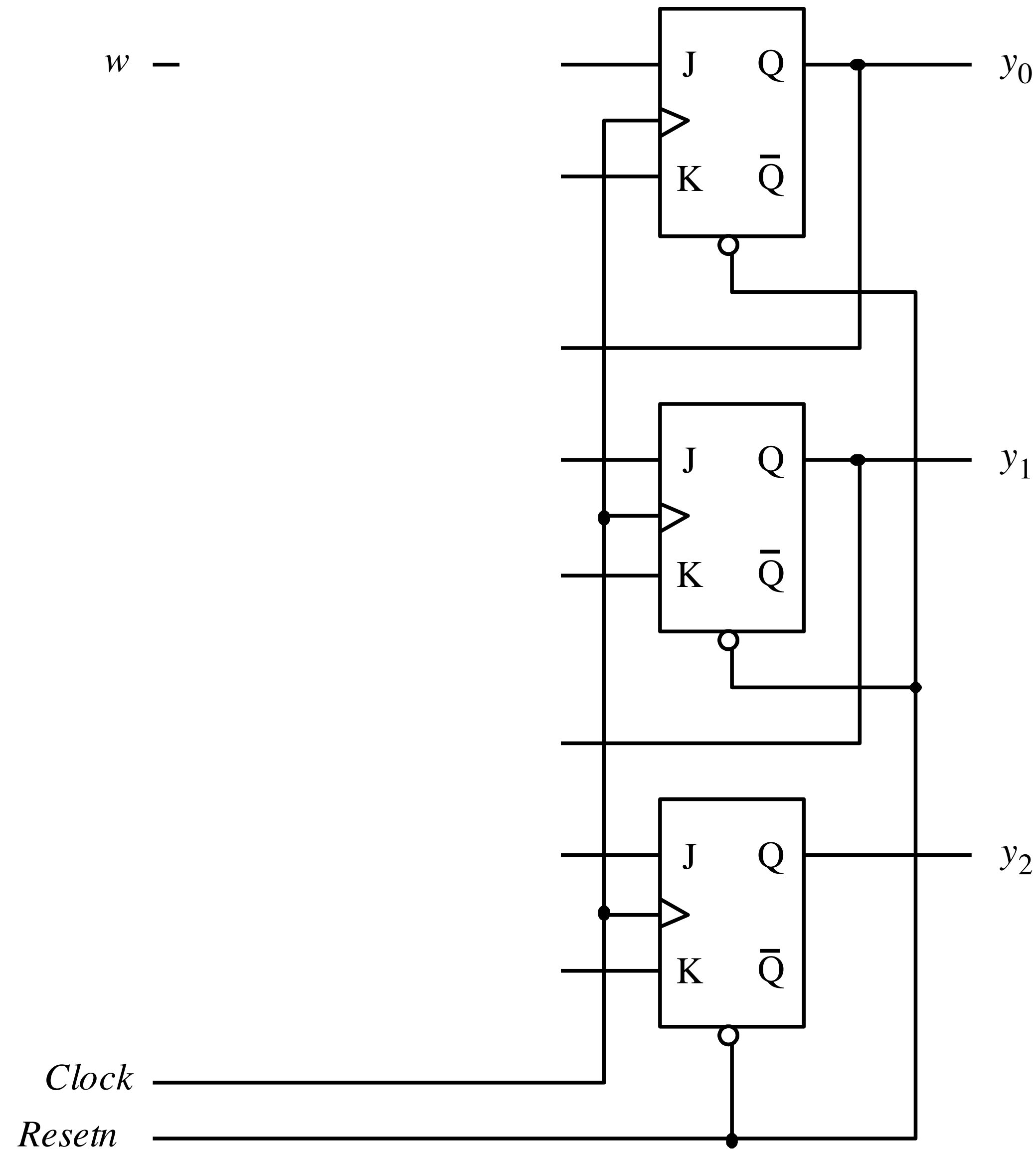
[Figure 6.66 from the textbook]

Circuit diagram using JK flip-flops

$$J_0 = w$$
$$K_0 = w$$

$$J_1 = wy_0$$
$$K_1 = wy_0$$

$$J_2 = wy_0y_1$$
$$K_2 = wy_0y_1$$

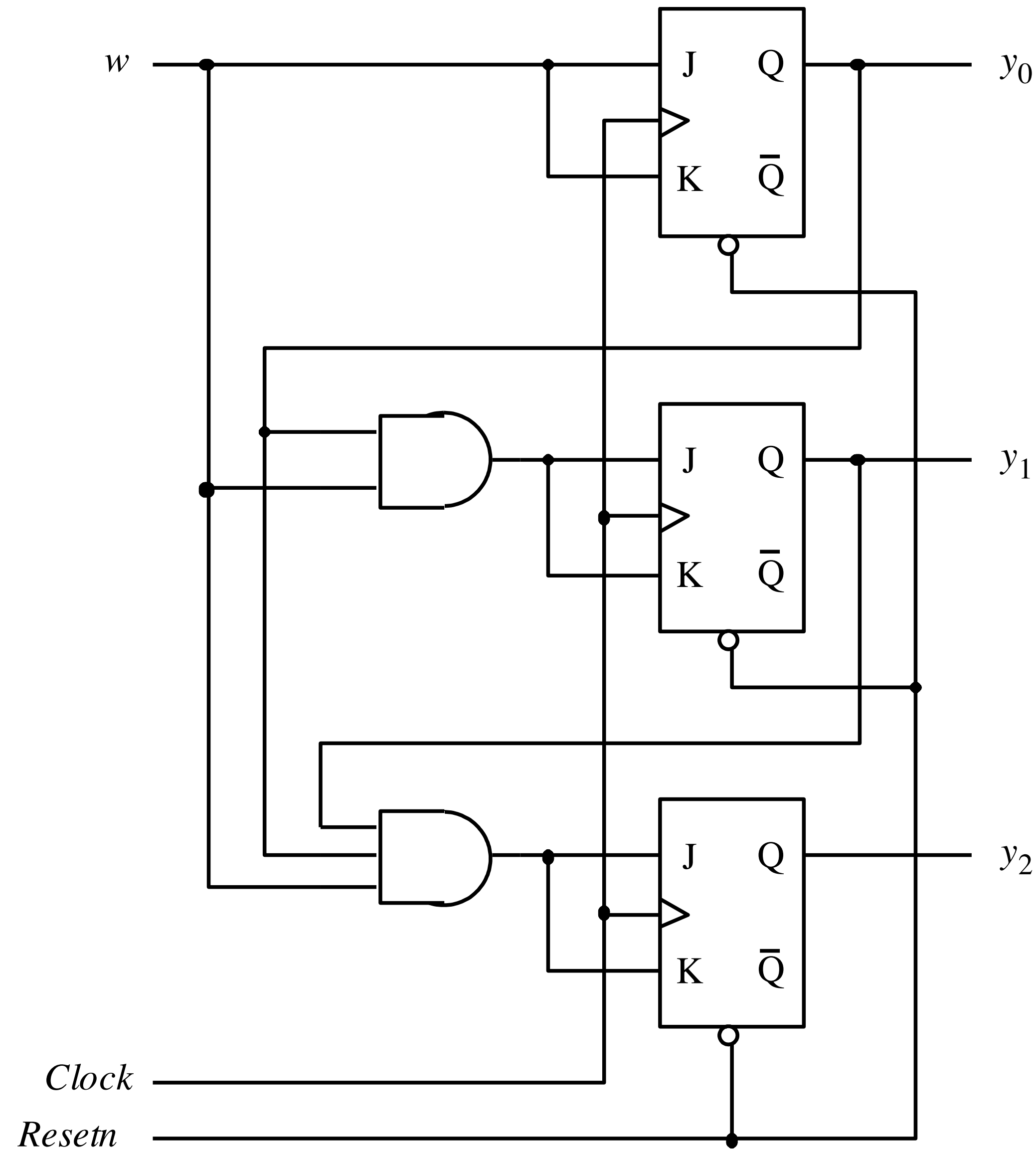


Circuit diagram using JK flip-flops

$$J_0 = w$$
$$K_0 = w$$

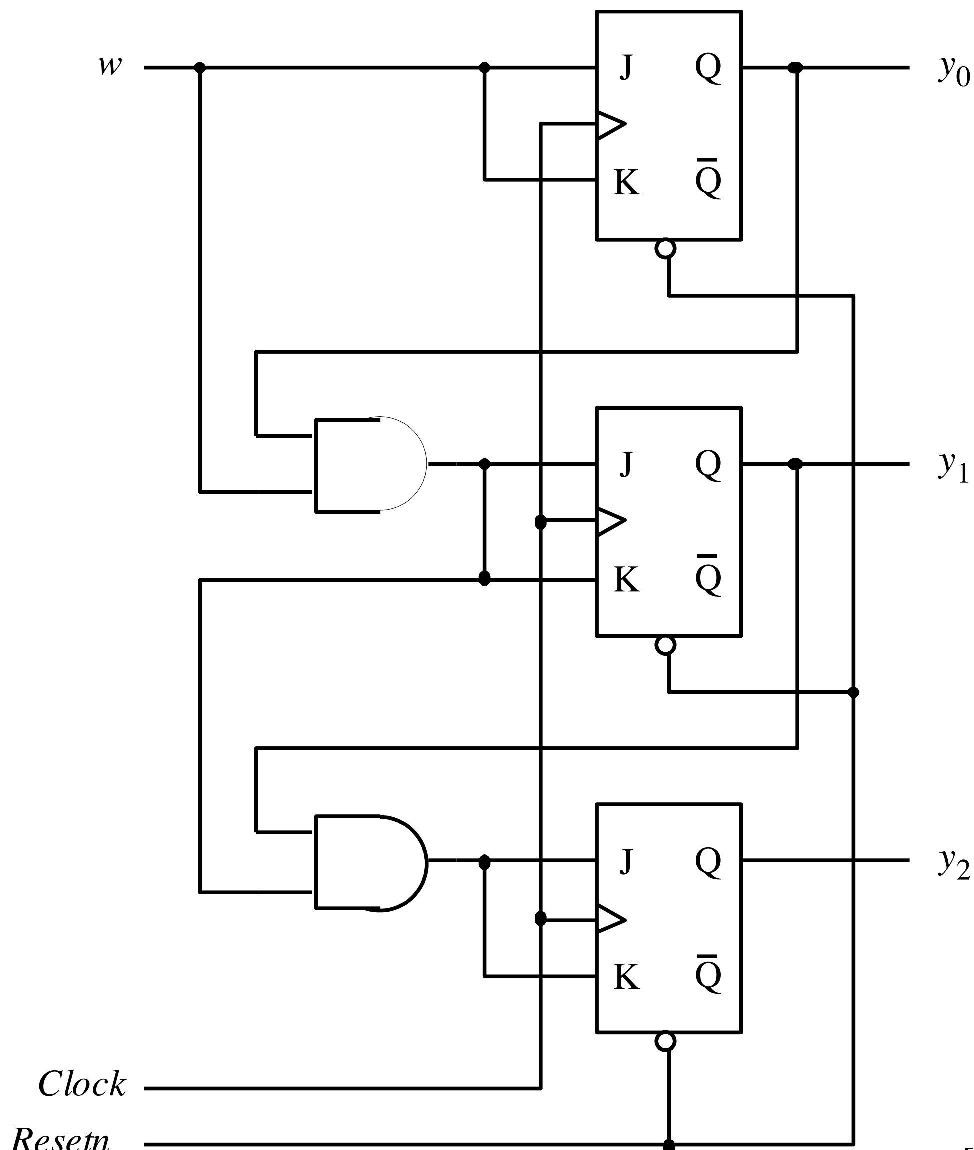
$$J_1 = wy_0$$
$$K_1 = wy_0$$

$$J_2 = wy_0y_1$$
$$K_2 = wy_0y_1$$



[Figure 6.67 from the textbook]

Factored-form implementation of the counter



[Figure 6.68 from the textbook]

Another Example
(A Different “Counter”)

Goal

- Implement a 3-bit counter using the sequential circuit approach that counts the pulses on the input line w.

- The counter must count in the following sequence:

  0, 4, 2, 6, 1, 5, 3, 7, 0, 4, 2, …

- The count must be represented directly by the flip-flop values. No extra gates are allowed.

- In other words, count = Q_2 Q_1 Q_0

- The count changes based on the input signal w:
  - If w=0, then the count remains the same
  - If w=1, then the count is advanced by one

Goal

- **Implement a 3-bit counter using the sequential circuit approach that counts the pulses on the input line w.**
- **The counter must count in the following sequence:**

  0, 4, 2, 6, 1, 5, 3, 7, 0, 4, 2, …

- **The count must be represented directly by the flip-flop values. No extra gates are allowed.**
- **In other words, count = Q_2 Q_1 Q_0**
- **The count changes based on the input signal w:**
  - **If w=0, then the count remains the same**
  - **If w=1, then the count is advanced by one**

Clock = w

By flipping the order of the bits we get

000	→	000
001	→	100
010		010
011		110
100		001
101		101
110		011
111	→	111

By flipping the order of the bits we get

0	000	000	0
1	001	100	4
2	010	010	2
3	011	110	6
4	100	001	1
5	101	101	5
6	110	011	3
7	111	111	7

State table for the counterlike example

Present state	Next state	Output $z_2z_1z_0$
A	B	000
B	C	100
C	D	010
D	E	110
E	F	001
F	G	101
G	H	011
H	A	111

[Figure 6.69 from the textbook]

State-assigned table for this example

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

[Figure 6.70 from the textbook]

K-maps for Y_2, Y_1, and Y_0

Present state $y_2 y_1 y_0$	Next state $Y_2 Y_1 Y_0$	Output $z_2 z_1 z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ $y_1 y_0$	00	01	11	10
0				
1				

K-maps for Y_2, Y_1, and Y_0

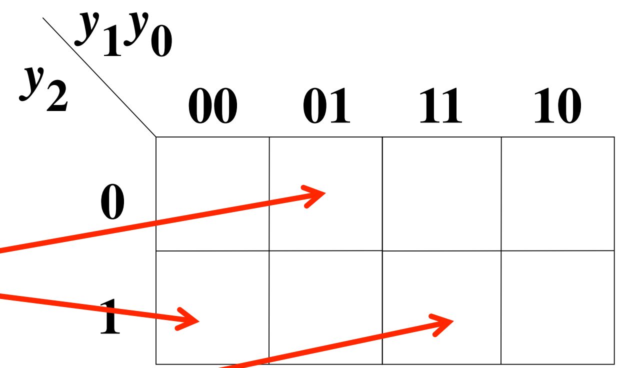
Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

Notice that these are scrambled

y_2 \ y_1y_0	00	01	11	10
0				
1				

K-maps for Y_2, Y_1, and Y_0

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111



Notice that these
are scrambled

K-map for Y_2

Present state $y_2 y_1 y_0$	Next state $Y_2 Y_1 Y_0$	Output $z_2 z_1 z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

$y_2 \backslash y_1 y_0$	00	01	11	10
0				
1				

K-map for Y_2

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0				
1				

K-map for Y_2

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0	1	1	1	1
1	0	0	0	0

K-map for Y_2

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0	1	1	1	1
1	0	0	0	0

$$Y_2 = \overline{y_2}$$

K-map for Y_1

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0				
1				

K-map for Y_1

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0				
1				

K-map for Y_1

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	**00**	**01**	**11**	**10**
0	**0**	**0**	**1**	**1**
1	**1**	**1**	**0**	**0**

K-map for Y_1

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0	0	0	1	1
1	1	1	0	0

$$Y_1 = y_2\overline{y_1} + \overline{y_2}\, y_1$$

XOR

K-map for Y_0

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0				
1				

K-map for Y_0

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0	**0**	**1**	**1**	**0**
1	**0**	**1**	**0**	**1**

K-map for Y_0

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0	0	1	1	0
1	0	1	0	1

$$Y_0 = \overline{y_1}\,y_0 + \overline{y_2}\,y_0 + y_2\,y_1\,\overline{y_0}$$

K-map for Y_0

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$	Output $z_2z_1z_0$
000	100	000
100	010	100
010	110	010
110	001	110
001	101	001
101	011	101
011	111	011
111	000	111

y_2 \ y_1y_0	00	01	11	10
0	0	1	1	0
1	0	1	0	1

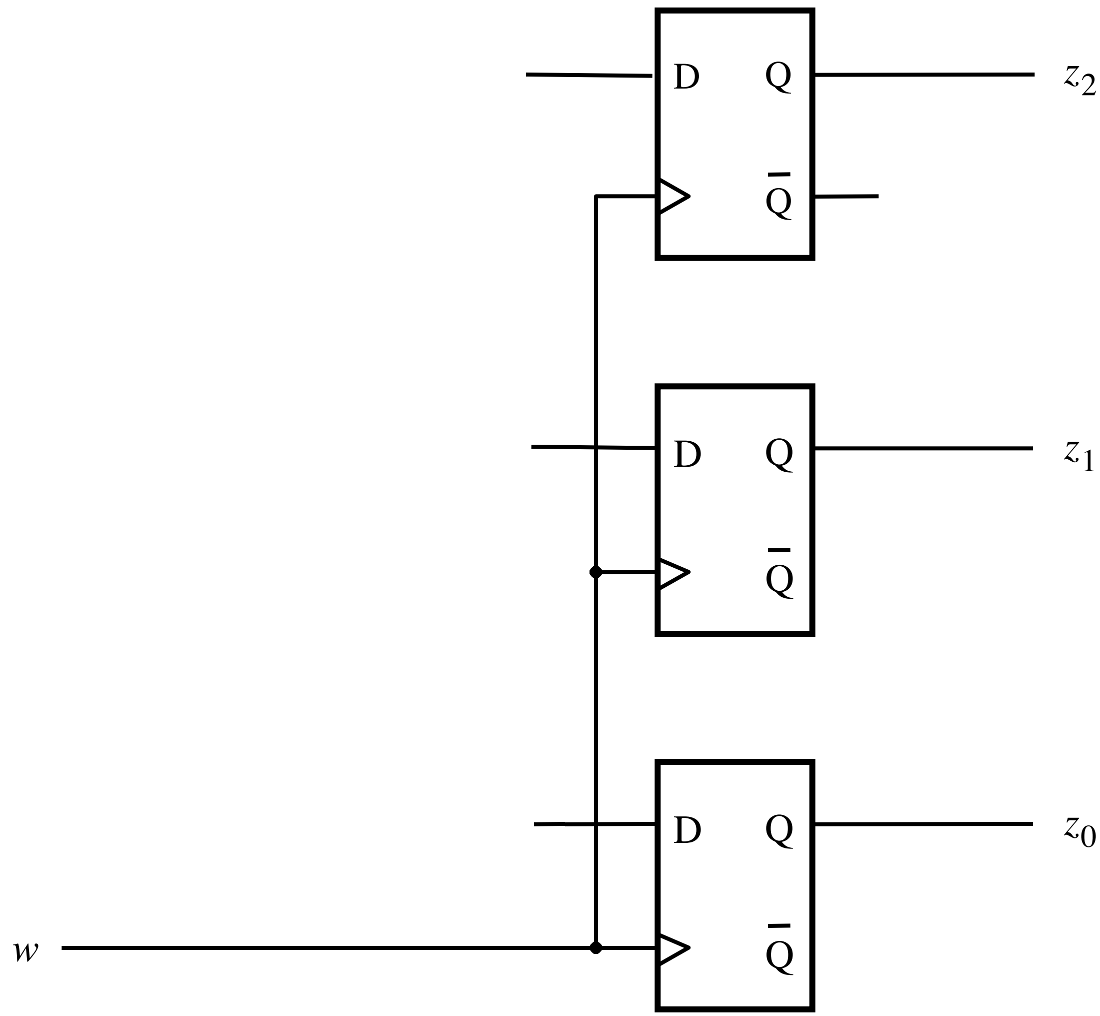
$$Y_0 = \overline{y_1} y_0 + \overline{y_2}\, y_0 + y_2\, y_1\, \overline{y_0}$$

$$= (\,\overline{y_1} + \overline{y_2}\,)\, y_0 + y_2\, y_1\, \overline{y_0}$$

$$= (\,\overline{y_1\, y_2}\,)\, y_0 + (y_2\, y_1)\, \overline{y_0}$$

$$= (\, y_1\, y_2\,) \oplus y_0$$

Let’s Draw the Circuit for this example

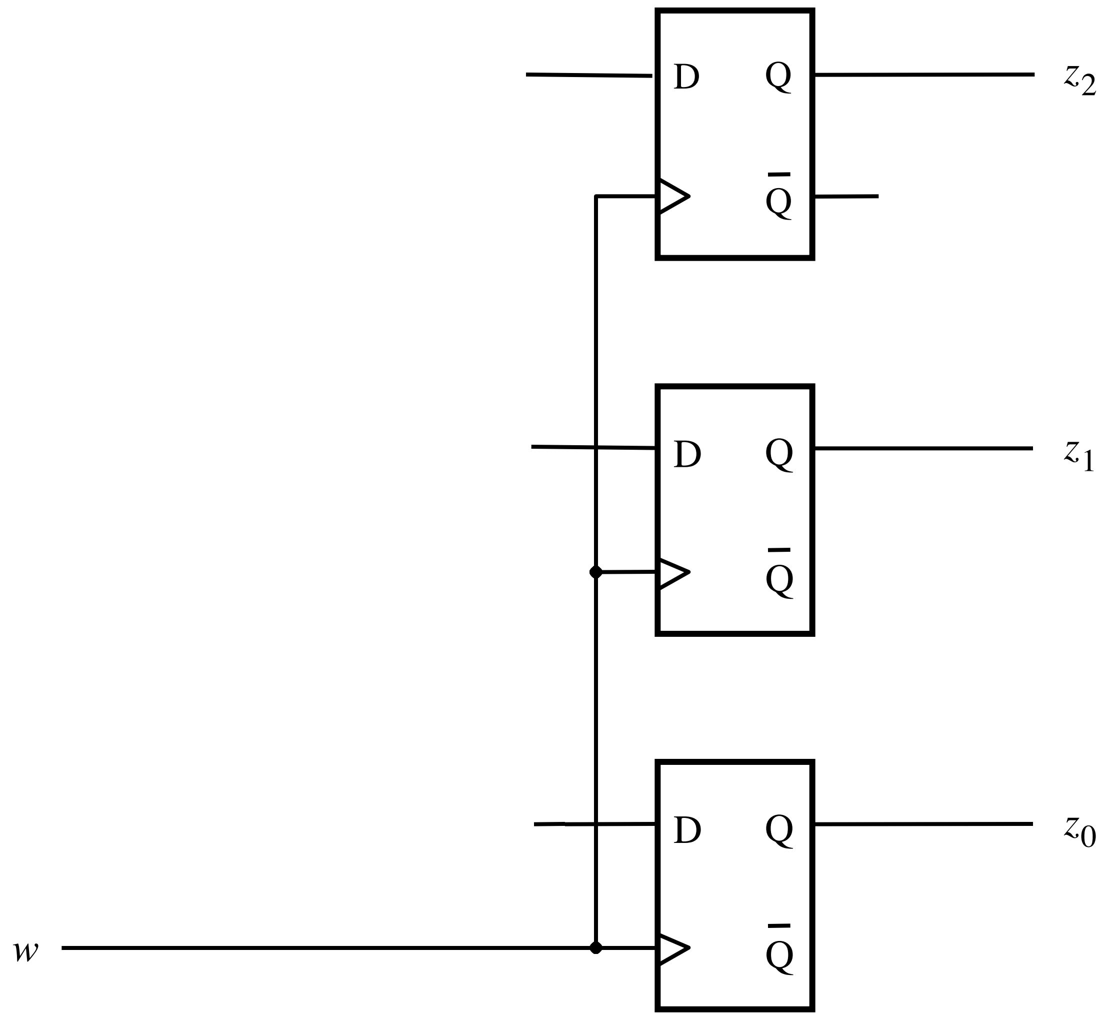


Let's Draw the Circuit for this example

$$Y_2 = \overline{y_2}$$

$$Y_1 = y_1 \oplus y_2$$

$$Y_0 = (y_1 y_2) \oplus y_0$$

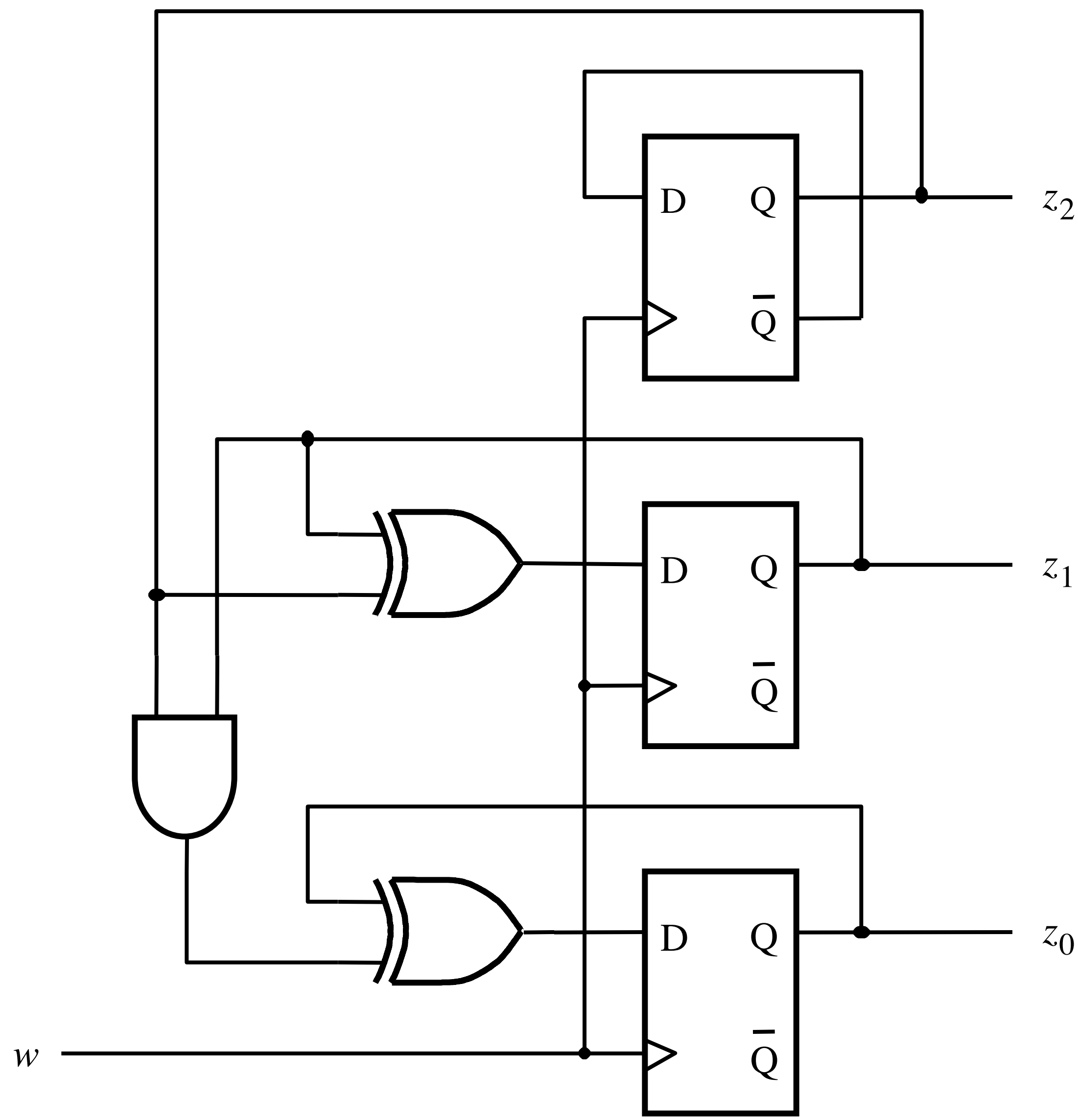


The Circuit for this example

$Y_2 = \overline{y_2}$

$Y_1 = y_1 \oplus y_2$

$Y_0 = (y_1 y_2) \oplus y_0$



[Figure 6.71 from the textbook]

Questions?

THE END