Cpr E 281 LAB 09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Designing Latches and Flip-Flops

PRELAB!

Read the entire lab, and **complete** the prelab questions (Q1-Q5) on the answer sheet **before** coming to the laboratory.

1.0 Objectives

In this Lab you will design the following storage elements:

- Basic SR Latch
- D Latch
- D Flip-Flop

The objective is to observe, analyze and understand the working and the timing behavior of these devices. You will do all the designs in this lab using a schematic block diagram. Refer to Sections 5.1 through 5.4, and complete the circuit diagrams before you come to the lab.

2.0 Basic SR Latches

Information on a Basic SR Latch can be found in Section 5.1 of the textbook. For the first step ***lab9step1***, build a Basic SR Latch with NOR gates using a block diagram/schematic file. This circuit is given in Figure 5.4a of your textbook. Name the inputs ***S*** and ***R***; name the outputs ***Q*** and ***~Q***.

Use the DE2-115 board to observe the behavior of the latch. (Recommend R=SW0, S=SW1, Q=LEDR0, ~Q=LEDG7). Use the results to complete the characteristic table on the answer sheet. When you are convinced that the latch is performing as predicted, and you are confident you understand its behavior, demonstrate your circuit to the TA.

Since latches and other memory devices can be built using either NAND or NOR gates, build another SR latch by replacing the NOR gates with NAND gates. Change the ***R*** input to ***S*** and the ***S*** input to ***R***. Place an inverter on each input to create the ~S~R case. Use the DE2-115 board to observe the behavior of the latch. Use the results to complete the characteristic table on the answer sheet. When you are convinced that the latch is performing as predicted, and you are confident you understand its behavior, demonstrate your circuit to the TA.

3.0 D Latches

In a new project ***lab9step2*** build a Gated D Latch using NAND gates and a NOT gate. Refer to Section 5.3 for a detailed explanation of D Latches. Figure 5.7a shows how to build a D Latch using NAND gates and a NOT gate. Once you have built the latch, label

the inputs ***Clk*** and ***D***, and outputs ***Q*** and ***~Q***. Use the DE2-115 board to observe the behavior of the latch. Since the pushbuttons can be a bit inconsistent it would be better to use a toggle switch to manually control the clock signal. (Recommend Clk=SW0, D=SW1, Q=LEDR0, ~Q=LEDG7). When you are convinced that the latch is performing as predicted, and you are confident you understand its behavior, complete the timing diagram on the answer sheet, (*pulse your clock signal once with D low before you start*), and demonstrate your circuit to the TA.

Create a **Symbol** for this Latch.

4.0 D Flip-Flops

Refer to Section 5.4 for a detailed explanation of D Flip-Flops.

In a new project, ***lab9step3a,*** use the Gated D Latch you built to design a Negative-Edge-Triggered Master-Slave D Flip-Flop. Section 5.4.1 discusses this design. Refer to Figure 5.9a. Use the DE2-115 board to observe the behavior of the latch. When you are convinced that the latch is performing as predicted, and you are confident you understand its behavior, complete the timing diagram on the answer sheet, (*pulse your clock signal once with D low before you start*), and demonstrate your circuit to the TA.

In a new project (***lab9step3b***) you will design a Positive-Edge-Triggered D Flip-Flop using NAND gates. Section 5.4.2 discusses this design. Please use Figure 5.11a as a guide for this step. Use the DE2-115 board to observe the behavior of the latch. When you are convinced that the latch is performing as predicted, and you are confident you understand its behavior, complete the timing diagram on the answer sheet, and demonstrate your circuit to the TA.

5.0 Complete

You are done with this lab. Close all lab files, exit Quartus Prime, log off the computer, power down the DE2-115 board, and hand in your answer sheet. **Don't forget to write down your name and your lab section number**.