

CprE 281: Digital Logic

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http://www.ece.iastate.edu/~alexs/classes/

Examples of Solved Problems

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Administrative Stuff

- HW5 is out
- It is due on Monday Oct 2 @ 4pm.
- Please write clearly on the first page (in block capital letters) the following three things:
 - Your First and Last Name
 - Your Student ID Number
 - Your Lab Section Letter
- Also, staple all of your pages together

Administrative Stuff

No homework is due next week.

Administrative Stuff

Midterm Exam #1

When: Friday Sep 22.

Where: This classroom

What: Chapter 1 and Chapter 2 plus number systems

 The exam will be open book and open notes (you can bring up to 3 pages of handwritten notes).

Topics for the Midterm Exam

- Binary Numbers
- Octal Numbers
- Hexadecimal Numbers
- Conversion between the different number systems
- Truth Tables
- Boolean Algebra
- Logic Gates
- Circuit Synthesis with AND, OR, NOT
- Circuit Synthesis with NAND, NOR
- Converting an AND/OR/NOT circuit to NAND circuit
- Converting an AND/OR/NOT circuit to NOR circuit
- SOP and POS expressions

Topics for the Midterm Exam

- Mapping a Circuit to Verilog code
- Mapping Verilog code to a circuit
- Multiplexers
- Venn Diagrams
- K-maps for 2, 3, and 4 variables
- Minimization of Boolean expressions using theorems
- Minimization of Boolean expressions with K-maps
- Incompletely specified functions (with don't cares)
- Functions with multiple outputs

Example 1

Determine if the following equation is valid

$$\bar{x}_1\bar{x}_3 + x_2x_3 + x_1\bar{x}_2 = \bar{x}_1x_2 + x_1x_3 + \bar{x}_2\bar{x}_3$$

$$\frac{?}{\bar{x}_1\bar{x}_3 + x_2x_3 + x_1\bar{x}_2} = \bar{x}_1x_2 + x_1x_3 + \bar{x}_2\bar{x}_3$$

$$\bar{x}_1 \bar{x}_3 + x_2 x_3 + x_1 \bar{x}_2 = \bar{x}_1 x_2 + x_1 x_3 + \bar{x}_2 \bar{x}_3$$

LHS RHS

Left-Hand Side (LHS)

Row number	x_1	x_2	x_3	$-\frac{1}{x_1}$	x_2x_3	$x_{1} x_{2}$	f
$0 \\ 1$	$\begin{array}{c} 0 \\ 0 \end{array}$	$0 \\ 0$	0 1				
$\frac{2}{3}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	1	$\begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}$	-			
$egin{array}{c} 4 \ 5 \ 6 \end{array}$	1 1 1	0 0 1	$egin{array}{c} 0 \\ 1 \\ 0 \end{array}$				
7	1	1	$\stackrel{\circ}{1}$				

Left-Hand Side (LHS)

Row number	x_1	x_2	x_3	$\frac{1}{x_1}\frac{1}{x_3}$	x_2x_3	$x_1 \overline{x_2}$	f
$egin{array}{c} 0 \ 1 \ 2 \ 3 \end{array}$	0 0 0 0	0 0 1 1	0 1 0 1	$\begin{bmatrix} 1 \\ 0 \\ 1 \\ 0 \end{bmatrix}$	0 0 0	0 0 0	
$egin{array}{c} 3 \\ 4 \\ 5 \\ 6 \\ 7 \end{array}$	1 1 1 1	0 0 1 1	0 1 0 1	0 0 0 0	0 0 0 0	0 1 1 0 0	

Left-Hand Side (LHS)

Row number	x_1	x_2	x_3	$-\frac{1}{x_1}$	$x_2 x_3$	$x_{1}x_{2}$	f
$egin{array}{cccccccccccccccccccccccccccccccccccc$	0 0 0 0 1 1	0 0 1 1 0 0	0 1 0 1 0	1 0 1 0 0	0 0 0 1 0 0	0 0 0 0 1 1	1 0 1 1 1
6 7	1	1	0 1	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$0 \\ 1$	$0 \\ 0$	$\begin{bmatrix} 0 \\ 1 \end{bmatrix}$

Right-Hand Side (RHS)

Row number	x_1	x_2	x_3	$-\frac{1}{x_1x_2}$	x_1x_3	$\overline{x_2} \overline{x_3}$	f
$egin{array}{c} 0 \ 1 \ 2 \end{array}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$	$egin{array}{c} 0 \ 0 \ 1 \end{array}$	0 1 0				
$rac{3}{4}$	$egin{array}{c} 0 \\ 1 \end{array}$	$\begin{array}{c} 1 \\ 1 \\ 0 \\ \end{array}$	0 1 0				
$egin{array}{c} 5 \ 6 \ 7 \end{array}$	1 1 1	0 1 1	1 0 1				

Right-Hand Side (RHS)

Row number	x_1	x_2	x_3	$-\frac{1}{x_1x_2}$	x_1x_3	$\frac{-}{x_2} \frac{-}{x_3}$	f
$egin{array}{c} 0 \ 1 \ 2 \ 3 \ 4 \ 5 \ 6 \ \end{array}$	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1	$egin{bmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}$	0 0 0 0 0 1	$egin{array}{c} 1 \\ 0 \\ 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{array}$	
7	1	1	1	0	1	$\overset{\circ}{0}$	

Right-Hand Side (RHS)

Row number	x_1	x_2	x_3	$-\frac{1}{x_1x_2}$	x_1x_3	$\frac{-}{x_2} \frac{-}{x_3}$	f
$egin{array}{c} 0 \ 1 \ 2 \ 3 \ 4 \ \end{array}$	0 0 0 0 1	0 0 1 1 0	0 1 0 1 0	$egin{pmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ \end{bmatrix}$	0 0 0 0 0	$egin{array}{c} 1 \\ 0 \\ 0 \\ 0 \\ 1 \end{array}$	1 0 1 1
$egin{array}{c} 5 \ 6 \ 7 \end{array}$	1 1 1	0 1 1	$egin{array}{c} 1 \ 0 \ 1 \end{array}$	0 0 0	$egin{array}{c} 1 \ 0 \ 1 \end{array}$	0 0 0	$\begin{array}{ c c } & 1 \\ & 0 \\ & 1 \end{array}$

$$\overline{x}_1\overline{x}_3 + x_2x_3 + x_1\overline{x}_2 = \overline{x}_1x_2 + x_1x_3 + \overline{x}_2\overline{x}_3$$
LHS
RHS

f		f
1		1
0		0
1		1
1		1
1		1
1		1
0	There are agreed	0
1	They are equal.	1

Example 2

Design the minimum-cost product-of-sums expression for the function

$$f(x_1, x_2, x_3) = \sum m(0, 2, 4, 5, 6, 7)$$

Minterms and Maxterms (with three variables)

Row number	$ x_1 $	x_2	x_3	Minterm	Maxterm
$egin{array}{c} 0 \ 1 \ 2 \ 3 \ 4 \ 5 \ 6 \ 7 \ \end{array}$	$egin{bmatrix} 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \$	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0	$egin{array}{ c c c c } m_0 &= \overline{x}_1 \overline{x}_2 \overline{x}_3 \ m_1 &= \overline{x}_1 \overline{x}_2 x_3 \ m_2 &= \overline{x}_1 x_2 \overline{x}_3 \ m_3 &= \overline{x}_1 x_2 x_3 \ m_4 &= x_1 \overline{x}_2 \overline{x}_3 \ m_5 &= x_1 \overline{x}_2 x_3 \ m_6 &= x_1 x_2 \overline{x}_3 \ m_7 &= x_1 x_2 x_3 \ \end{array}$	$M_0 = x_1 + x_2 + x_3$ $M_1 = x_1 + x_2 + \overline{x_3}$ $M_2 = x_1 + \overline{x_2} + x_3$ $M_3 = x_1 + \overline{x_2} + \overline{x_3}$ $M_4 = \overline{x_1} + x_2 + x_3$ $M_5 = \overline{x_1} + x_2 + \overline{x_3}$ $M_6 = \overline{x_1} + \overline{x_2} + x_3$ $M_7 = \overline{x_1} + \overline{x_2} + \overline{x_3}$

Minterms and Maxterms (with three variables)

Row number	$ x_1 $	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0=\overline{x}_1\overline{x}_2\overline{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	$1 \mid$	$m_1 = \overline{x}_1 \overline{x}_2 x_3$	$M_1 = x_1 + x_2 + \overline{x}_3$
2	0	1	0	$m_2 = \overline{x}_1 x_2 \overline{x}_3$	$M_2 = x_1 + \overline{x}_2 + x_3$
3	0	1	$1 \mid$	$m_3 = \overline{x}_1 x_2 x_3$	$M_3 = x_1 + \overline{x}_2 + \overline{x}_3$
4	1	0	0	$m_4 = x_1 \overline{x}_2 \overline{x}_3$	$M_4 = \overline{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1 \overline{x}_2 x_3$	$M_5 = \overline{x}_1 + x_2 + \overline{x}_3$
6	1	1	0	$m_6 = x_1 x_2 \overline{x}_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$
7	1	1	1	$m_7 = x_1 x_2 x_3$	$M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

The function is 1 for these rows

Minterms and Maxterms (with three variables)

Row number	$ x_1 $	x_2	x_3	Minterm	Maxterm
0	0	0	0 1	$m_0 = \overline{x}_1 \overline{x}_2 \overline{x}_3$ $m_1 = \overline{x}_1 \overline{x}_2 x_3$	$M_0 = x_1 + x_2 + x_3$ $M_1 = x_1 + x_2 + \overline{x}_3$
3	0	1 1	0 1	$m_2 = \overline{x}_1 x_2 \overline{x}_3$ $m_3 = \overline{x}_1 x_2 x_3$	$M_2 = x_1 + \overline{x}_2 + x_3$ $M_3 = x_1 + \overline{x}_2 + \overline{x}_3$
5	1 1	0	0 1	$m_4 = x_1 \overline{x}_2 \overline{x}_3$ $m_5 = x_1 \overline{x}_2 x_3$	$M_4 = \overline{x}_1 + x_2 + x_3$ $M_5 = \overline{x}_1 + x_2 + \overline{x}_3$
6 7	1	1 1	0	$m_6 = x_1 x_2 \overline{x}_3$ $m_7 = x_1 x_2 x_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$ $M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

The function is 1 for these rows

The function is 0 for these rows

Two different ways to specify the same function f of three variables

$$f(x_1, x_2, x_3) = \sum m(0, 2, 4, 5, 6, 7)$$

$$f(x_1, x_2, x_3) = \Pi M(1, 3)$$

The POS Expression

$$M_1 = x_1 + x_2 + \overline{x}_3$$

$$M_3 = x_1 + \overline{x}_2 + \overline{x}_3$$

$$f(x_1, x_2, x_3) = \Pi M(1, 3)$$

$$= M_1 \cdot M_3$$

$$= (x_1 + x_2 + \overline{x_3}) \cdot (x_1 + \overline{x_2} + \overline{x_3})$$

The Minimum POS Expression

$$f(x_1, x_2, x_3) = (x_1 + x_2 + \overline{x_3}) \cdot (x_1 + \overline{x_2} + \overline{x_3})$$

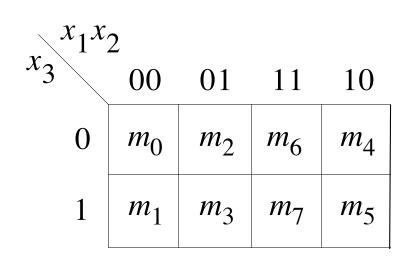
$$= (x_1 + \overline{x_3} + x_2) \cdot (x_1 + \overline{x_3} + \overline{x_2})$$

$$= (x_1 + \overline{x_3})$$

Hint: Use the following Boolean Algebra theorem

14b.
$$(x + y) \cdot (x + \overline{y}) = x$$

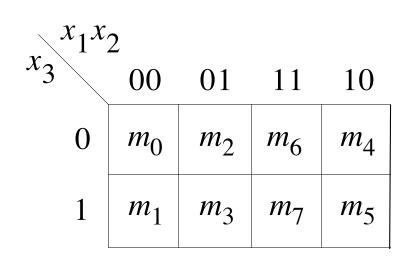
x_1	x_2	x_3	
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7
			I



(b) Karnaugh map

(a) Truth table

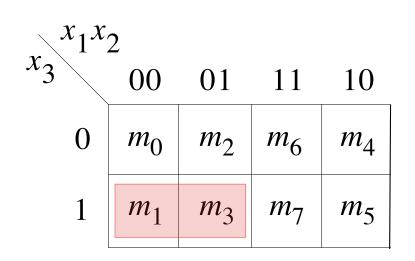
$\frac{x_1}{x_1}$	x_2	x_3	
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7
		'	1



(b) Karnaugh map

(a) Truth table

$\underline{x_1}$	x_2	x_3	
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7
			l

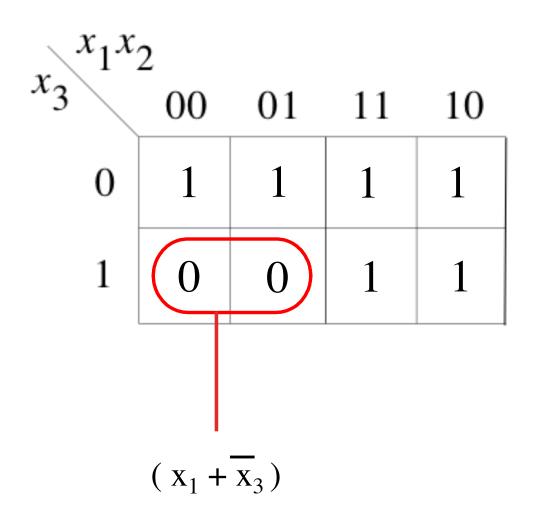


(b) Karnaugh map

(a) Truth table

x_1x_2							
x_3	00	01	11	10			
0	m_0	m_2	m_6	m_4			
1	m_1	m_3	m_7	m_5			

x_1x_2							
x_3	00	01	11	10			
0	1	1	1	1			
1	0	0	1	1			



Example 3

Problem: A circuit that controls a given digital system has three inputs: x_1 , x_2 , and x_3 . It has to recognize three different conditions:

- Condition A is true if x_3 is true and either x_1 is true or x_2 is false
- Condition B is true if x_1 is true and either x_2 or x_3 is false
- Condition C is true if x_2 is true and either x_1 is true or x_3 is false

The control circuit must produce an output of 1 if at least two of the conditions A, B, and C are true. Design the simplest circuit that can be used for this purpose.

Condition A

Condition A is true if x_3 is true and either x_1 is true or x_2 is false

Condition A

Condition A is true if x_3 is true and either x_1 is true or x_2 is false

$$A = x_3(x_1 + \overline{x}_2) = x_3x_1 + x_3\overline{x}_2$$

Condition B

Condition B is true if x_1 is true and either x_2 or x_3 is false

Condition B

Condition B is true if x_1 is true and either x_2 or x_3 is false

$$B = x_1(\bar{x}_2 + \bar{x}_3) = x_1\bar{x}_2 + x_1\bar{x}_3$$

Condition C

Condition C is true if x_2 is true and either x_1 is true or x_3 is false

Condition C

Condition C is true if x_2 is true and either x_1 is true or x_3 is false

$$C = x_2(x_1 + \bar{x}_3) = x_2x_1 + x_2\bar{x}_3$$

The output of the circuit can be expressed as f = AB + AC + BC

$$AB = (x_3x_1 + x_3\bar{x}_2)(x_1\bar{x}_2 + x_1\bar{x}_3)$$

$$= x_3x_1x_1\bar{x}_2 + x_3x_1x_1\bar{x}_3 + x_3\bar{x}_2x_1\bar{x}_2 + x_3\bar{x}_2x_1\bar{x}_3$$

$$= x_3x_1\bar{x}_2 + 0 + x_3\bar{x}_2x_1 + 0$$

$$= x_1\bar{x}_2x_3$$

The output of the circuit can be expressed as f = AB + AC + BC

$$AC = (x_3x_1 + x_3\overline{x}_2)(x_2x_1 + x_2\overline{x}_3)$$

$$= x_3x_1x_2x_1 + x_3x_1x_2\overline{x}_3 + x_3\overline{x}_2x_2x_1 + x_3\overline{x}_2x_2\overline{x}_3$$

$$= x_3x_1x_2 + 0 + 0 + 0$$

$$= x_1x_2x_3$$

The output of the circuit can be expressed as f = AB + AC + BC

$$BC = (x_1 \overline{x}_2 + x_1 \overline{x}_3)(x_2 x_1 + x_2 \overline{x}_3)$$

$$= x_1 \overline{x}_2 x_2 x_1 + x_1 \overline{x}_2 x_2 \overline{x}_3 + x_1 \overline{x}_3 x_2 x_1 + x_1 \overline{x}_3 x_2 \overline{x}_3$$

$$= 0 + 0 + x_1 \overline{x}_3 x_2 + x_1 \overline{x}_3 x_2$$

$$= x_1 x_2 \overline{x}_3$$

Finally, we get

$$f = x_1 \overline{x}_2 x_3 + x_1 x_2 x_3 + x_1 x_2 \overline{x}_3$$

$$= x_1 (\overline{x}_2 + x_2) x_3 + x_1 x_2 (x_3 + \overline{x}_3)$$

$$= x_1 x_3 + x_1 x_2$$

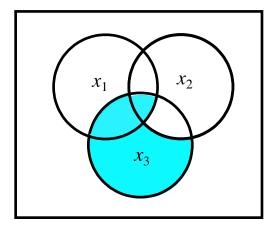
$$= x_1 (x_3 + x_2)$$

Example 4

Solve the previous problem using Venn diagrams.

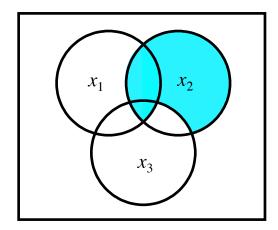
Venn Diagrams

(find the areas that are shaded at least two times)



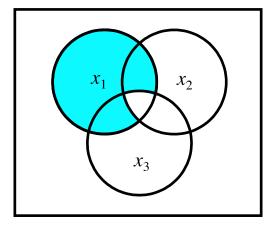
(a) Function A:

$$x_3x_1 + x_3\bar{x}_2$$



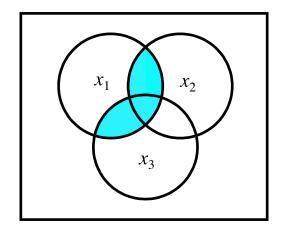
(c) Function C

$$x_2x_1 + x_2\bar{x}_3$$



(b) Function B

$$x_1\bar{x}_2 + x_1\bar{x}_3$$



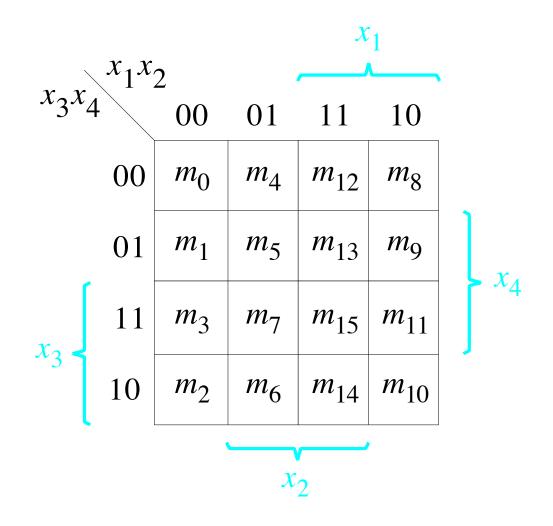
(d) Function f

$$x_1(x_3 + x_2)$$

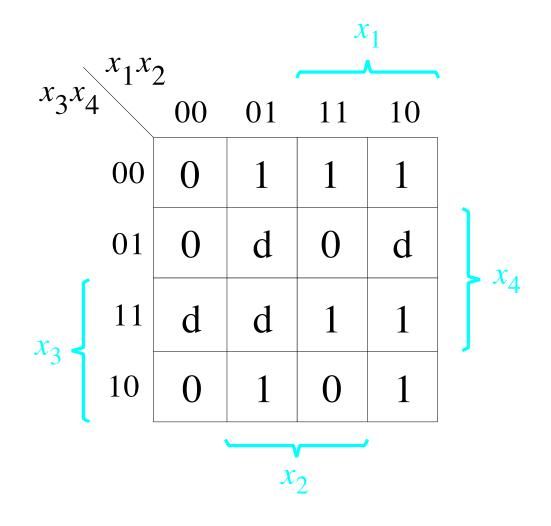
Example 5

Design the minimum-cost SOP and POS expression for the function

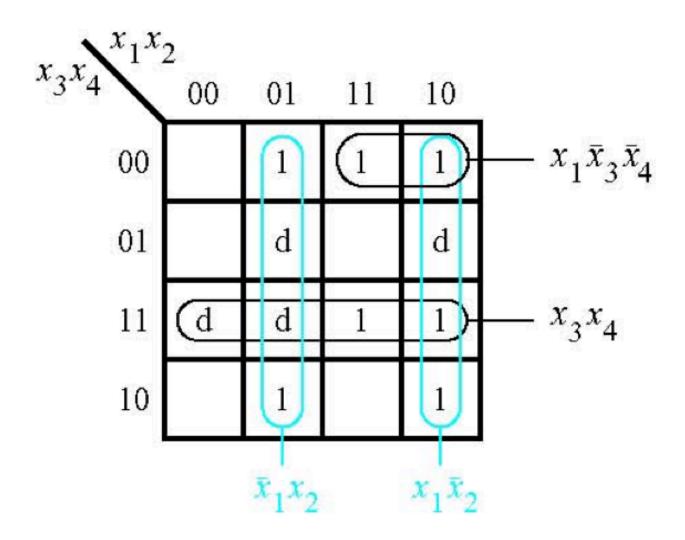
Let's Use a K-Map



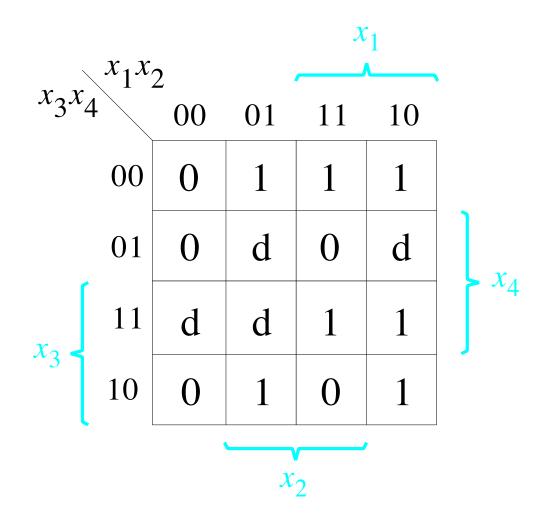
Let's Use a K-Map



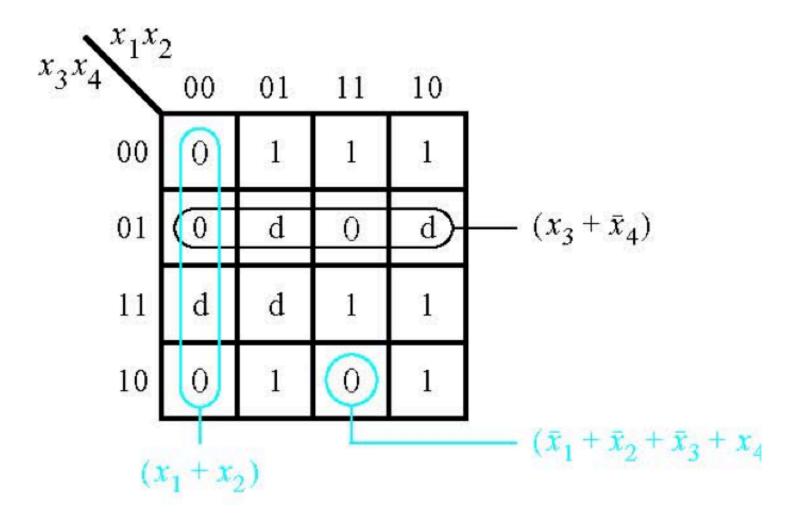
The SOP Expression



What about the POS Expression?



The POS Expression



Example 6

Use K-maps to find the minimum-cost SOP and POS expression for the function

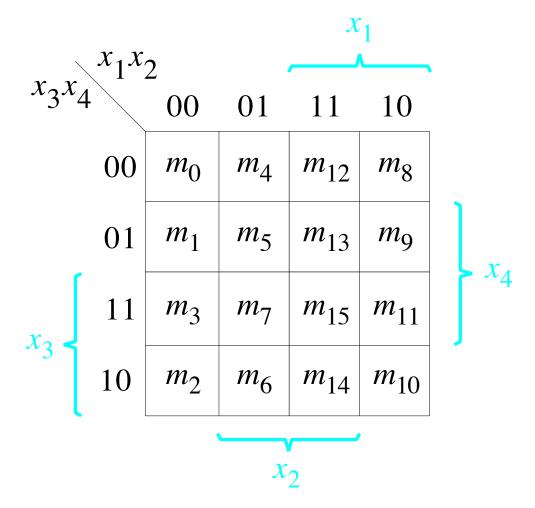
$$f(x_1, \ldots, x_4) = \overline{x}_1 \overline{x}_3 \overline{x}_4 + x_3 x_4 + \overline{x}_1 \overline{x}_2 x_4 + x_1 x_2 \overline{x}_3 x_4$$

assuming that there are also don't-cares defined as $D = \sum (9, 12, 14)$.

Let's map the expression to the K-Map

$$f(x_1, \dots, x_4) = \overline{x}_1 \overline{x}_3 \overline{x}_4 + x_3 x_4 + \overline{x}_1 \overline{x}_2 x_4 + x_1 x_2 \overline{x}_3 x_4$$

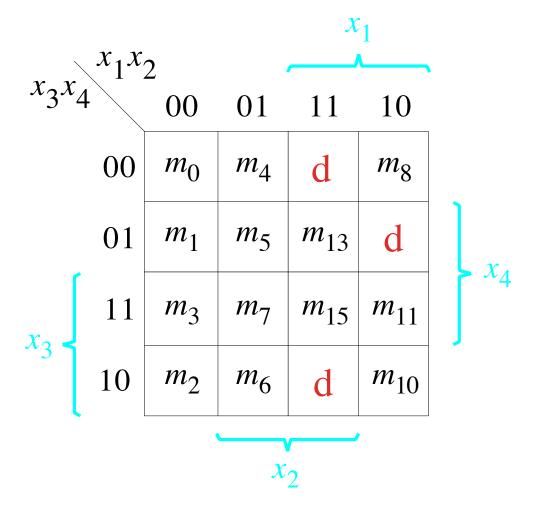
 $D = \sum (9, 12, 14).$



Let's map the expression to the K-Map

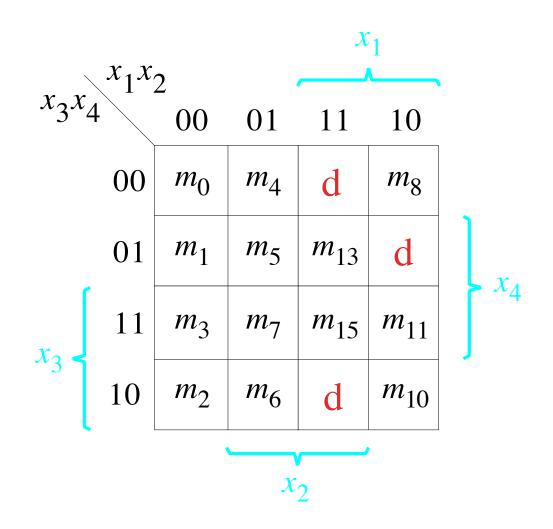
$$f(x_1, \dots, x_4) = \overline{x}_1 \overline{x}_3 \overline{x}_4 + x_3 x_4 + \overline{x}_1 \overline{x}_2 x_4 + x_1 x_2 \overline{x}_3 x_4$$

 $D = \sum (9, 12, 14).$



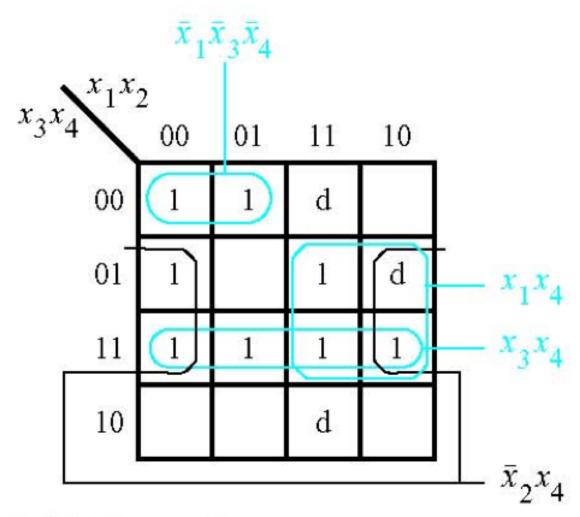
Let's map the expression to the K-Map

$$f(x_1, \ldots, x_4) = \overline{x}_1 \overline{x}_3 \overline{x}_4 + x_3 x_4 + \overline{x}_1 \overline{x}_2 x_4 + x_1 x_2 \overline{x}_3 x_4$$



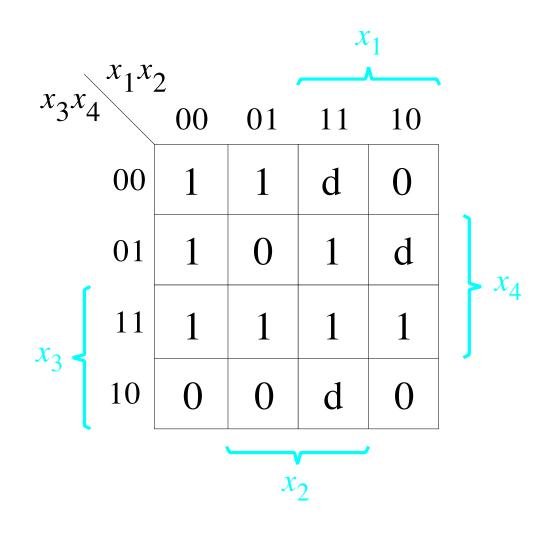
The SOP Expression

$$f(x_1, \ldots, x_4) = \overline{x}_1 \overline{x}_3 \overline{x}_4 + x_3 x_4 + \overline{x}_1 \overline{x}_2 x_4 + x_1 x_2 \overline{x}_3 x_4$$

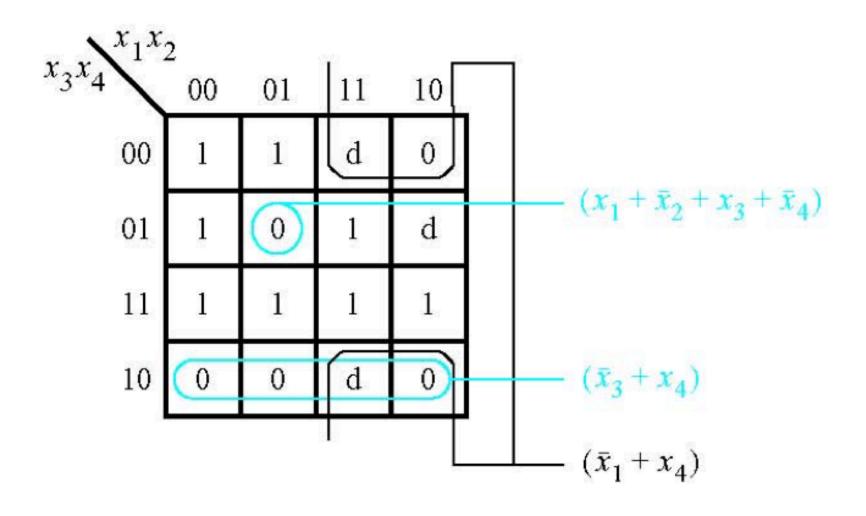


$$f = x_3 x_4 + \overline{x}_1 \overline{x}_3 \overline{x}_4 + \overline{x}_2 x_4 + x_1 x_4$$

What about the POS Expression?



The POS Expression



$$f = (\overline{x}_3 + x_4)(\overline{x}_1 + x_4)(x_1 + \overline{x}_2 + x_3 + \overline{x}_4)$$

Example 7

Derive the minimum-cost SOP expression for

$$f = s_3(\bar{s}_1 + \bar{s}_2) + s_1s_2$$

First, expand the expression using property 12a

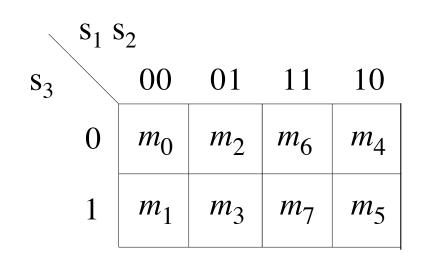
$$f = s_3(\bar{s}_1 + \bar{s}_2) + s_1s_2$$

$$f = \bar{s}_1 s_3 + \bar{s}_2 s_3 + s_1 s_2$$

Construct the K-Map for this expression

$$f = \bar{s}_1 s_3 + \bar{s}_2 s_3 + s_1 s_2$$

\mathbf{S}_1	S_2	S_3	
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7
			I

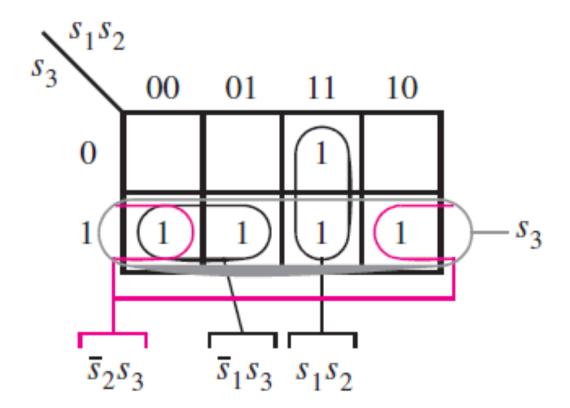


(b) Karnaugh map

(a) Truth table

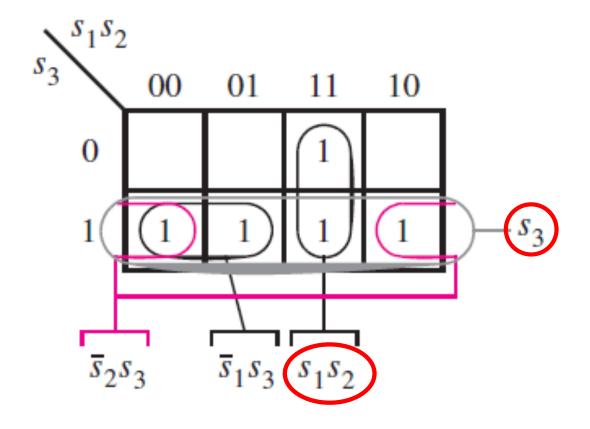
Construct the K-Map for this expression

$$f = \bar{s}_1 s_3 + \bar{s}_2 s_3 + s_1 s_2$$



Construct the K-Map for this expression

$$f = \bar{s}_1 s_3 + \bar{s}_2 s_3 + s_1 s_2$$

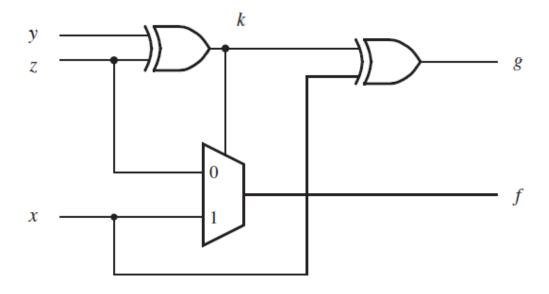


Simplified Expression: $f = s_3 + s_1 s_2$

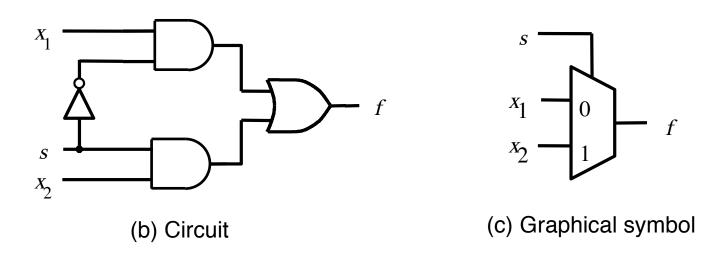
Example 8

Write the Verilog code for the following circuit ...

Logic Circuit

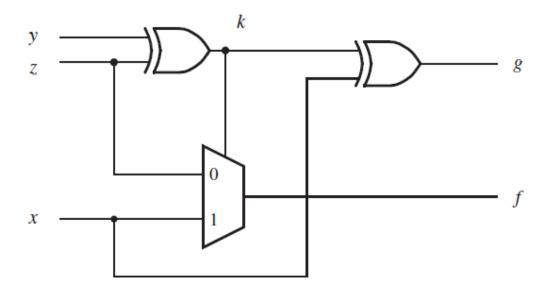


Circuit for 2-1 Multiplexer



$$f(s, x_1, x_2) = \overline{s} x_1 + s x_2$$

Logic Circuit vs Verilog Code



```
module f_g (x, y, z, f, g);

input x, y, z;

output f, g;

wire k;

assign k = y \ z;

assign g = k \ x;

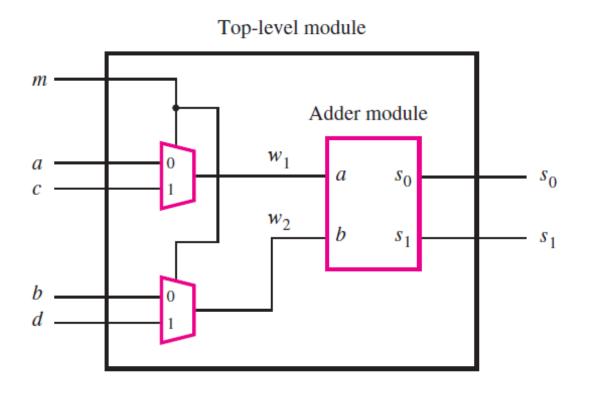
assign f = (\sim k \& z) | (k \& x);
```

endmodule

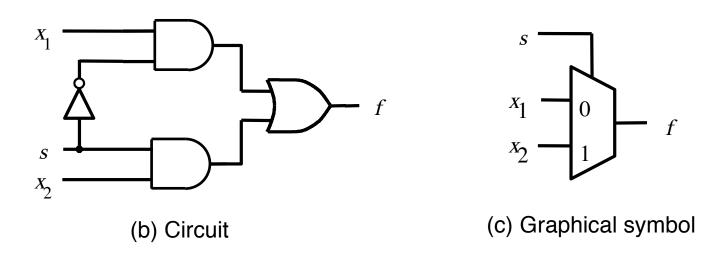
Example 9

Write the Verilog code for the following circuit ...

The Logic Circuit for this Example

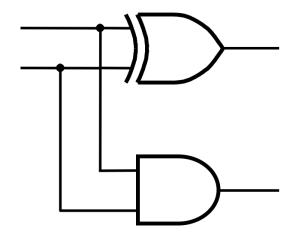


Circuit for 2-1 Multiplexer



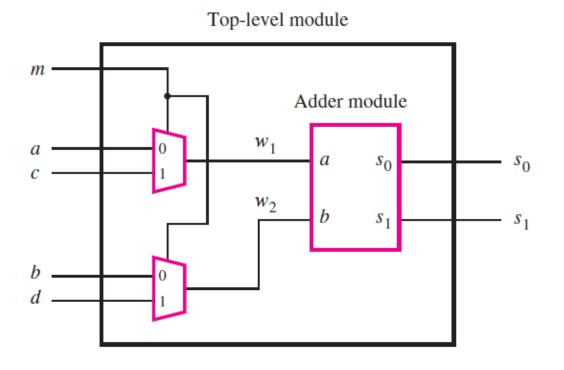
$$f(s, x_1, x_2) = \overline{s} x_1 + s x_2$$

Addition of Binary Numbers



a	b	<i>s</i> ₁	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

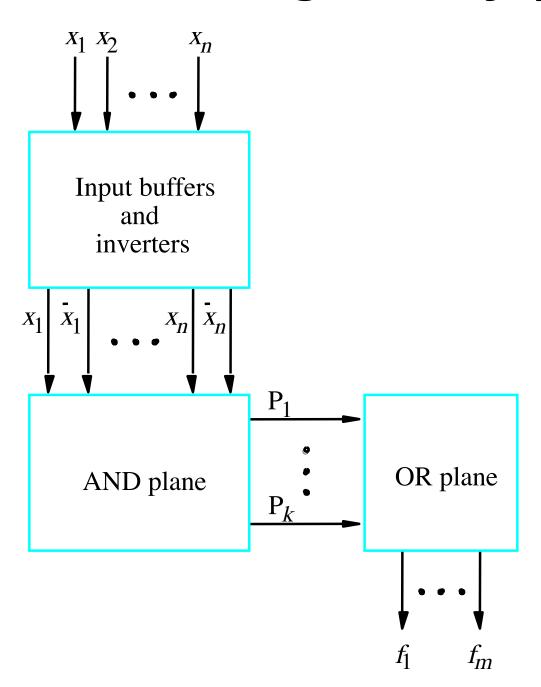
Logic Circuit vs Verilog Code



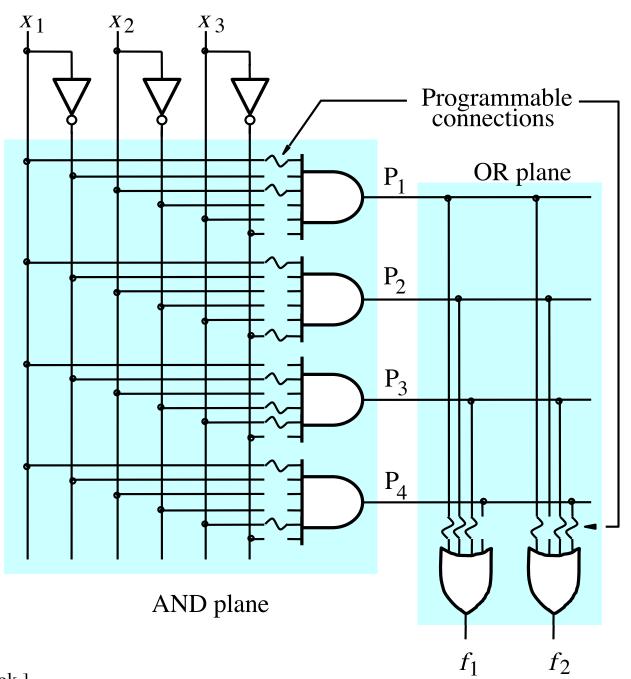
```
module shared (a, b, c, d, m, s1, s0);
   input a, b, c, d, m;
   output s1, s0;
   wire w1, w2;
   mux2to1 U1 (a, c, m, w1);
   mux2to1 U2 (b, d, m, w2);
   adder U3 (w1, w2, s1, s0);
endmodule
module mux2to1(x1, x2, s, f);
   input x1, x2, s;
   output f;
   assign f = (\sim s \& x1) | (s \& x2);
endmodule
module adder (a, b, s1, s0);
   input a, b;
   output s1, s0;
   assign s1 = a \& b;
  assign s0 = a ^ b;
endmodule
```

Some material form Appendix B

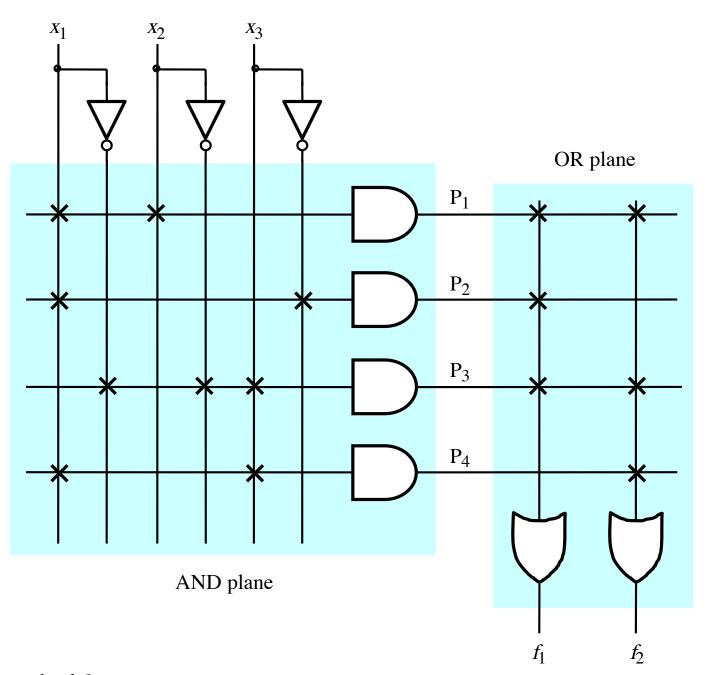
Programmable Logic Array (PLA)



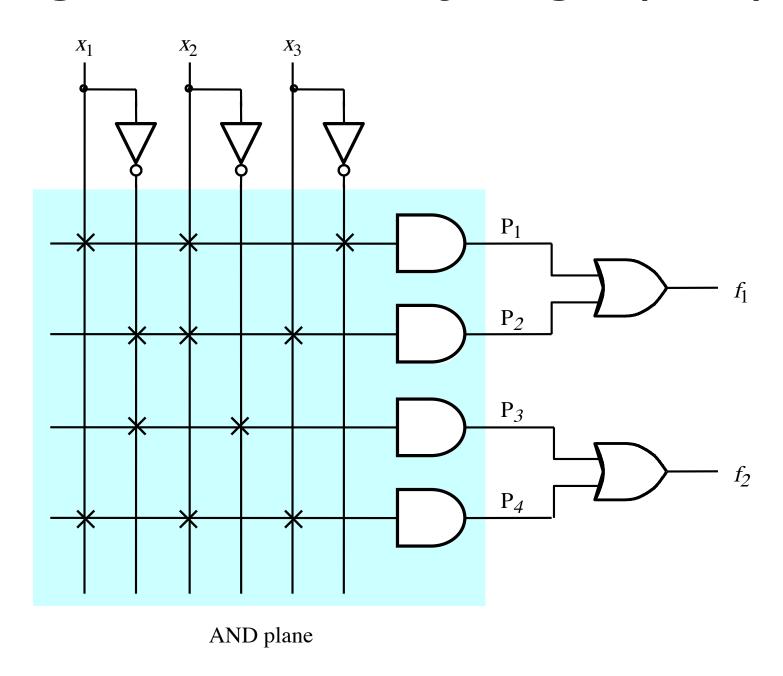
Gate-Level Diagram of a PLA



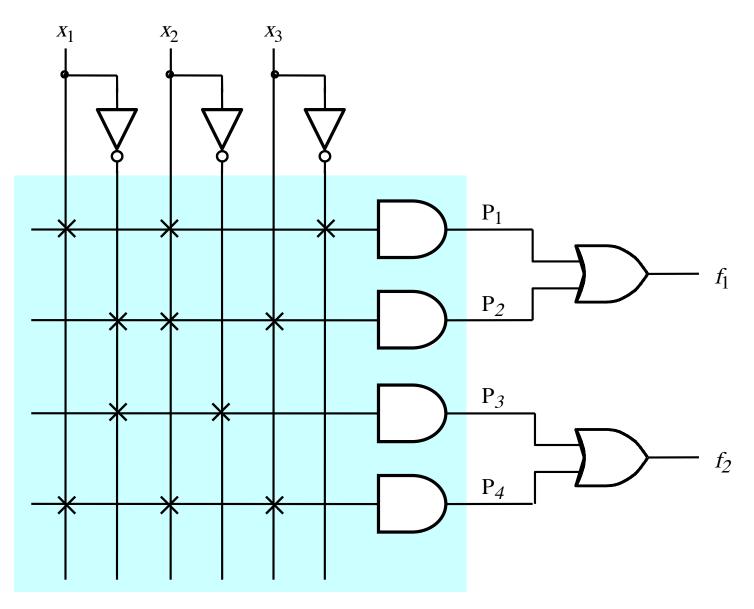
Customary Schematic for PLA



Programmable Array Logic (PAL)



Programmable Array Logic (PAL)



AND plane

Only the AND plane is programmable. The OR plane is fixed.

Questions?

THE END