



CprE 281: Digital Logic

Instructor: Alexander Stoytchev

<http://www.ece.iastate.edu/~alexs/classes/>

Mealy State Model

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Iowa State University, Ames, IA
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Administrative Stuff

- **Homework 10 is out**
- **It is due on Monday Nov 13 @ 4pm**

Administrative Stuff

- **Final Project**
- **Posted on the class web page (Labs section)**
- **Pick one of the problems and solve it.**
- **Your grade will not depend on which project you pick**
- **By next Wednesday you need to select your project and send an e-mail to your lab TAs**

Sample E-mail

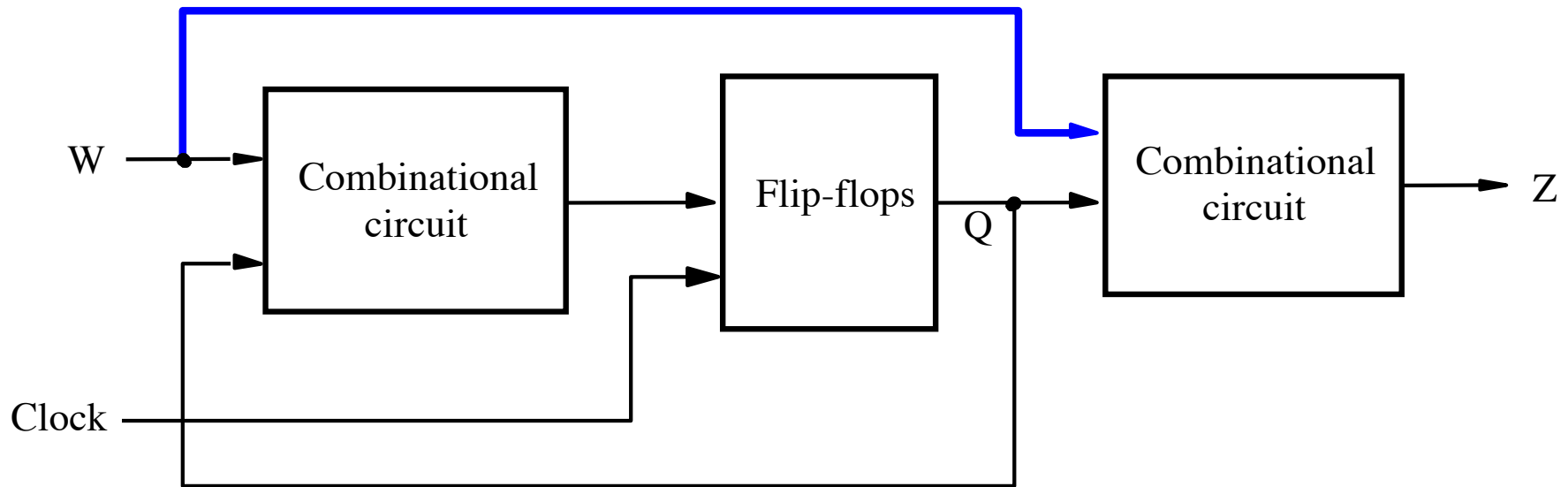
Hello TAs,

I decided to pick problem number x for my final project in CprE 281.

Thanks,

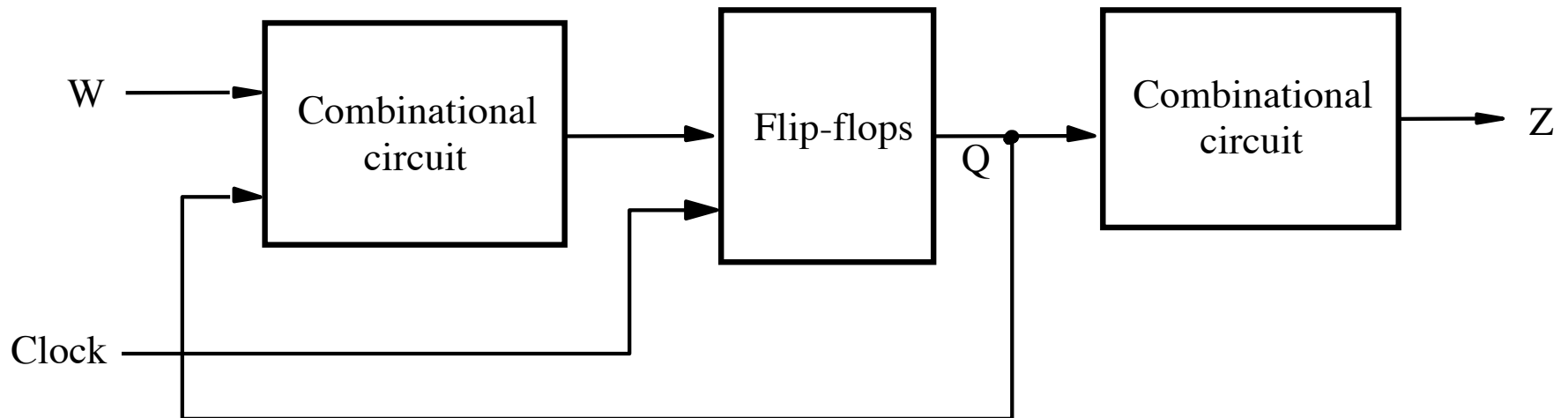
[your name, your lab section]

The general form of a synchronous sequential circuit

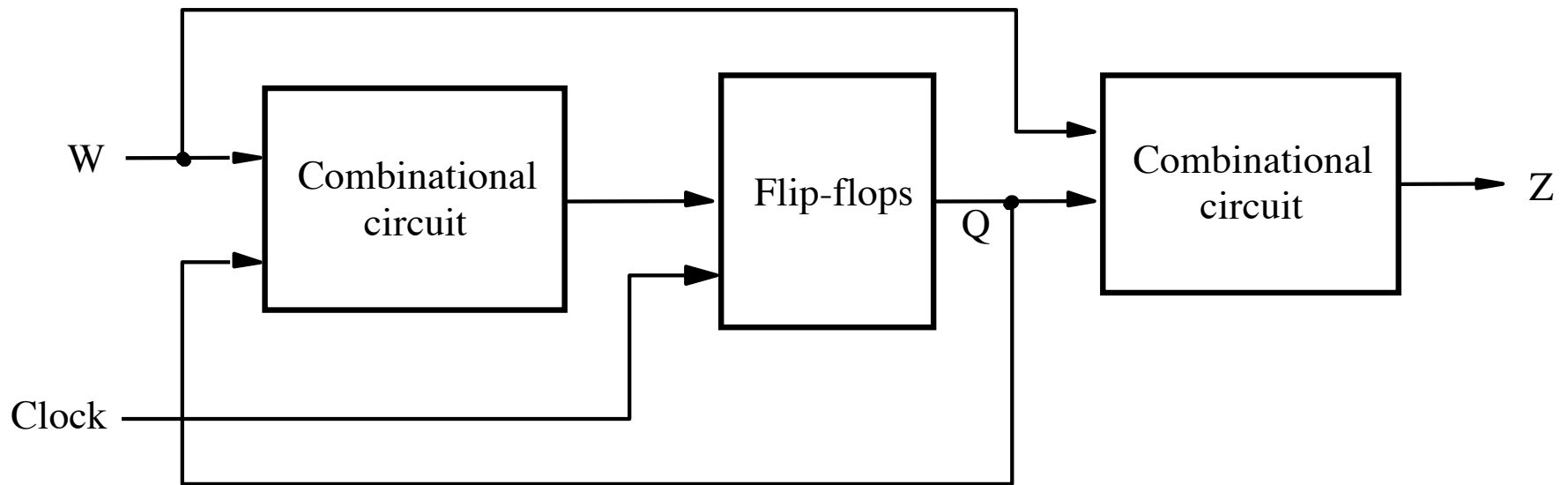


[Figure 6.1 from the textbook]

Moore Type



Mealy Type



Sample Problem

Implement a 11 detector. In other words, the output should be equal to 1 if two consecutive 1's have been detected on the input line.

The output should become 1 as soon as the second 1 is detected in the input.

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w :	0	1	0	1	1	0	1	1	1	0	1
z :	0	0	0	0	1	0	0	1	1	0	0

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

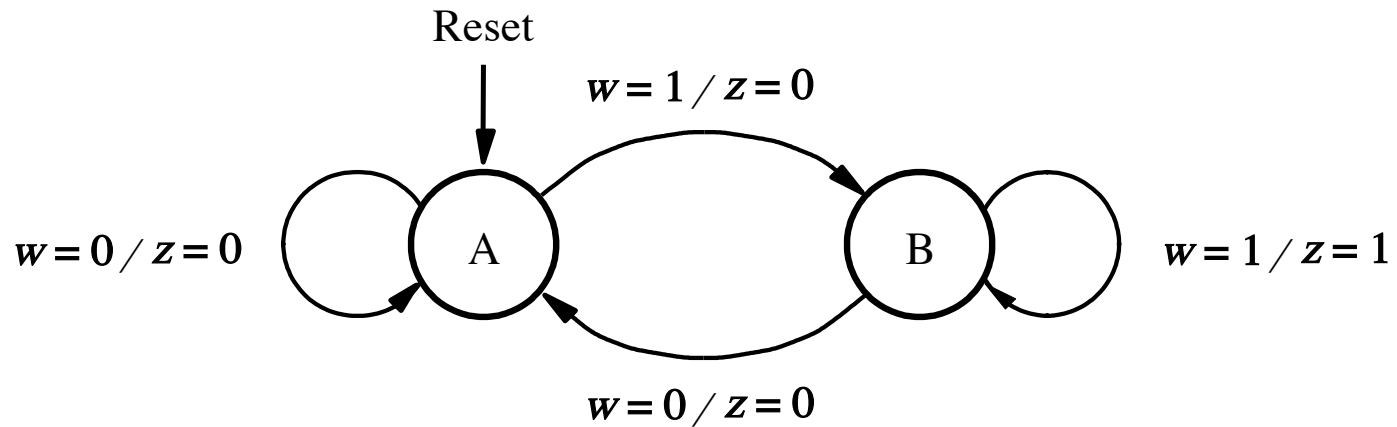
Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

Sequences of input and output signals

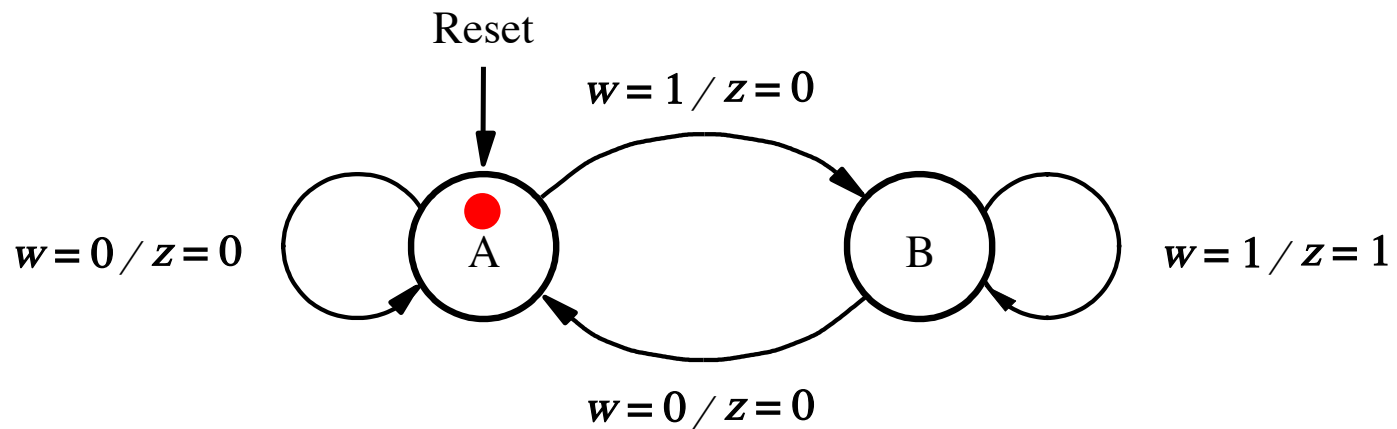
Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

State diagram of an FSM that realizes the task



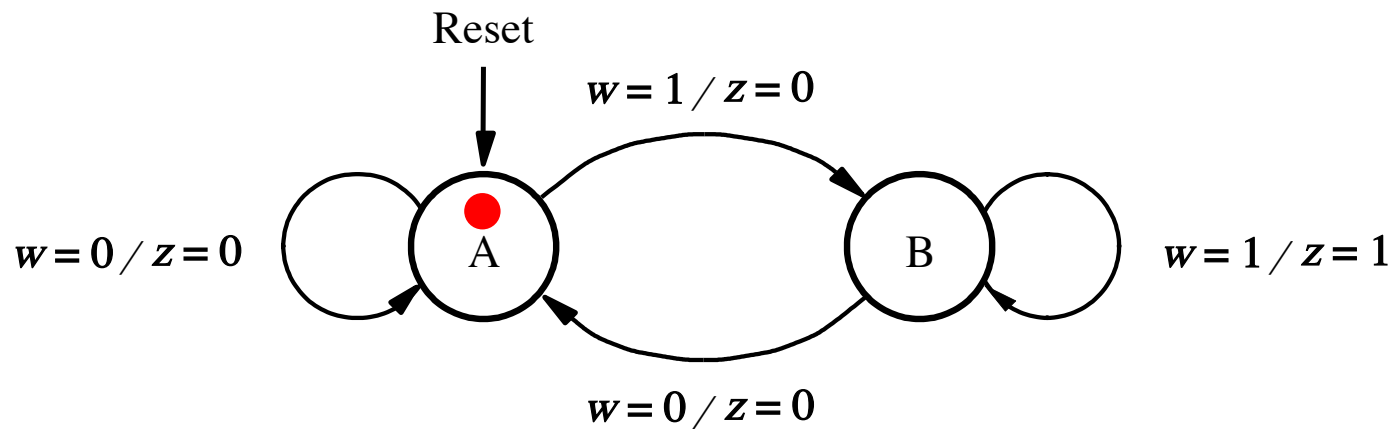
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	<input type="checkbox"/> 0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



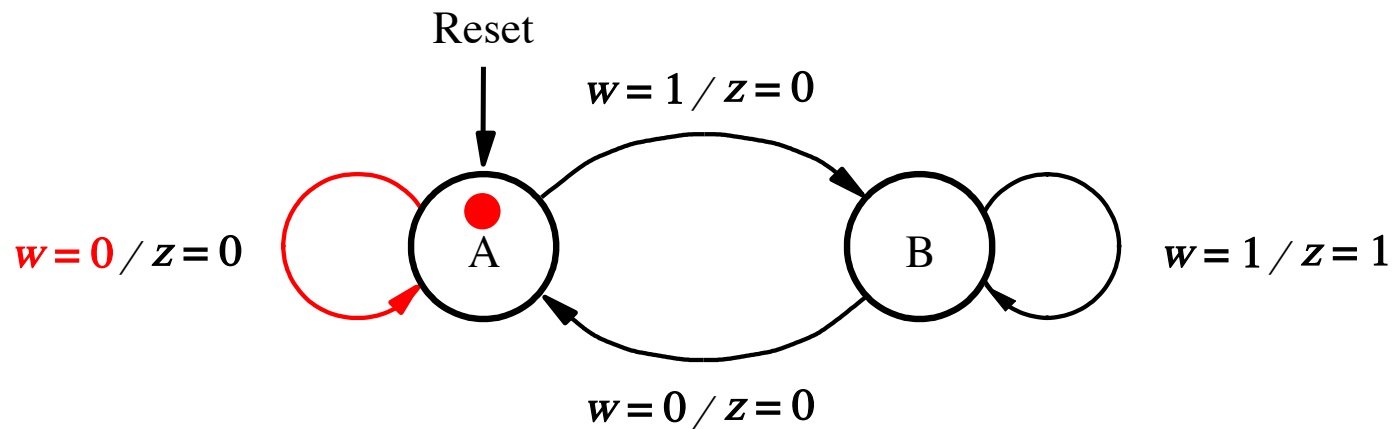
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



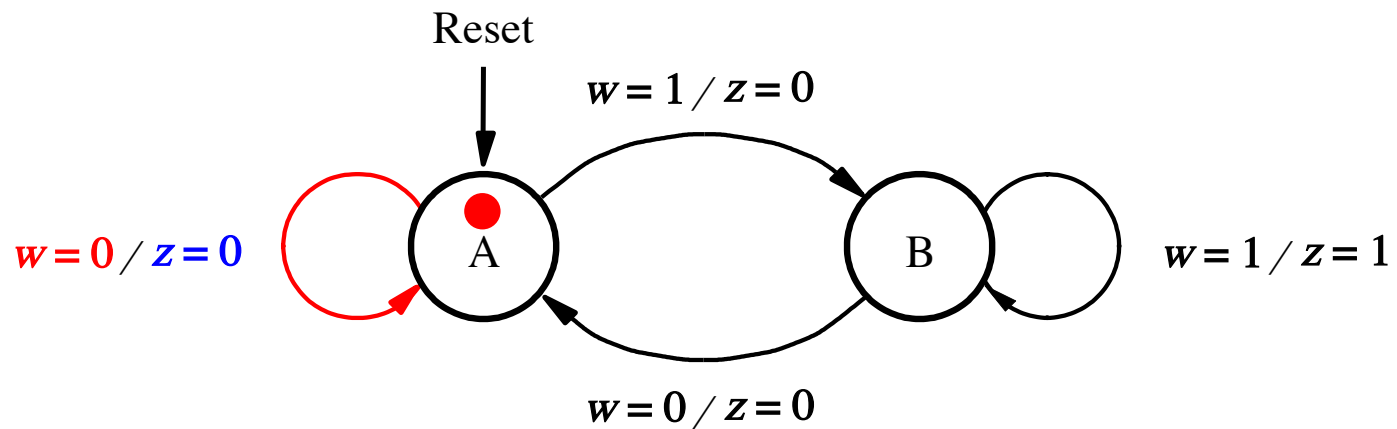
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



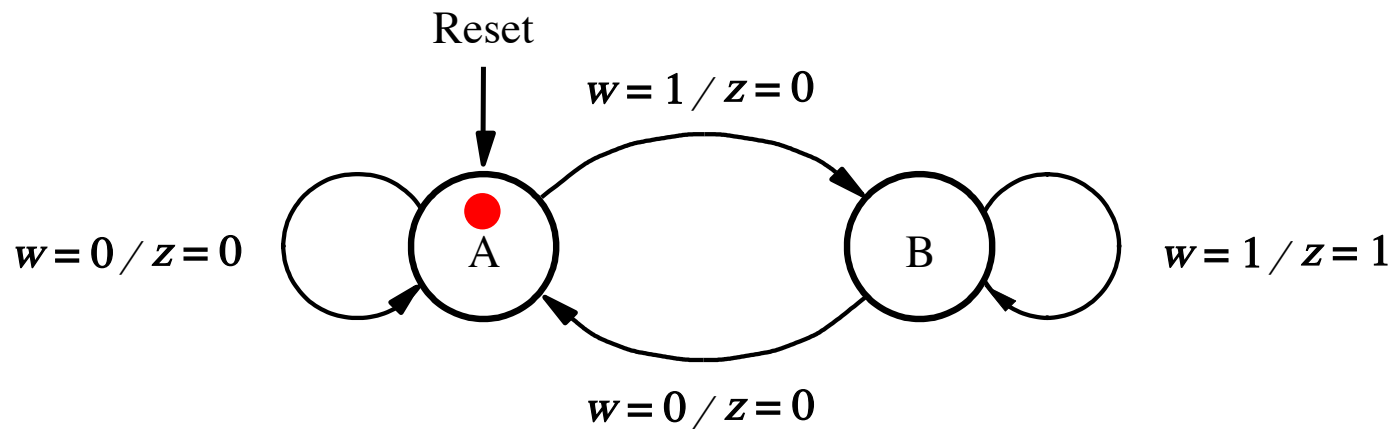
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input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



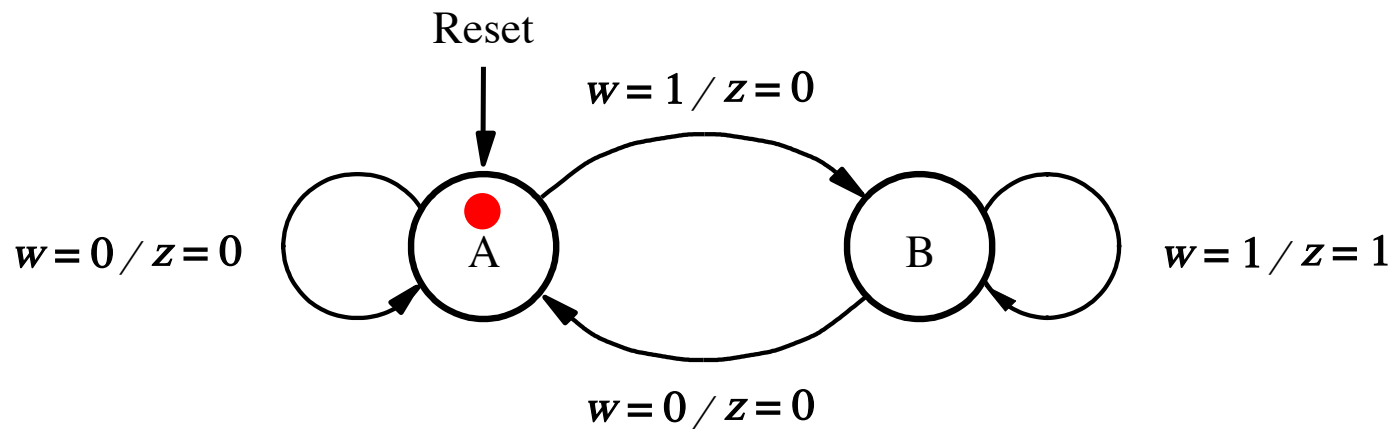
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input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



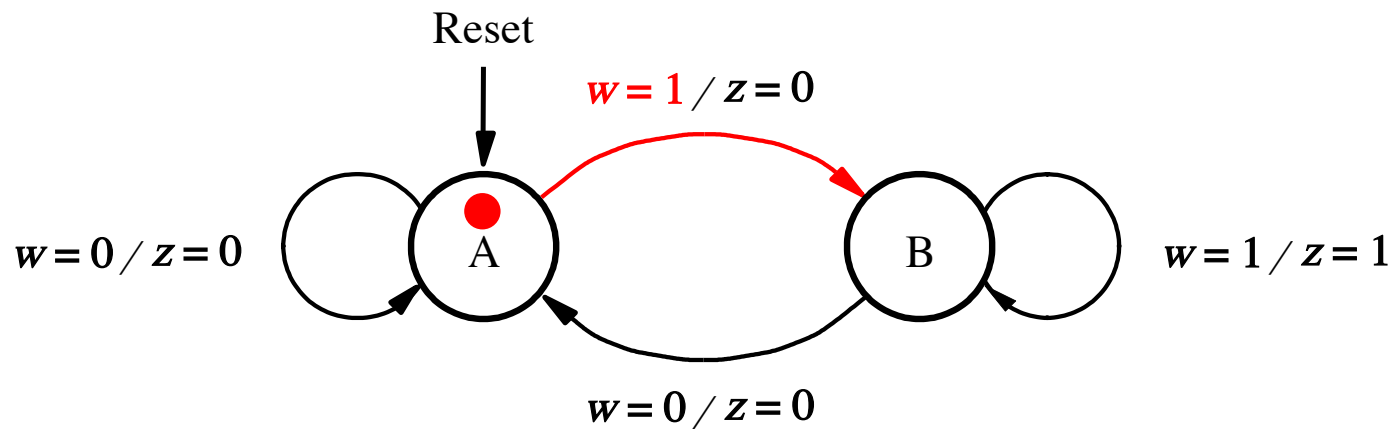
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



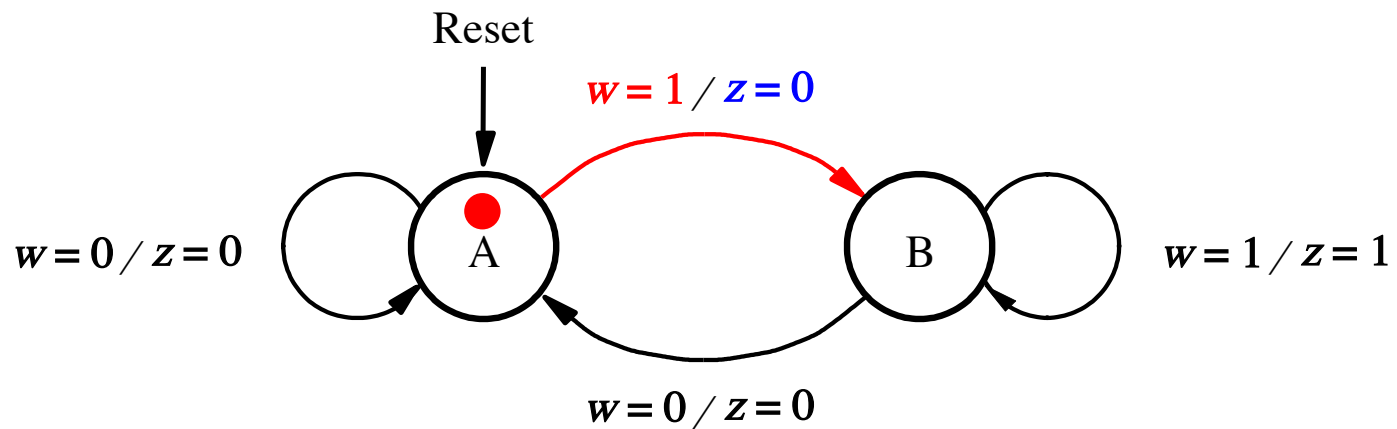
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



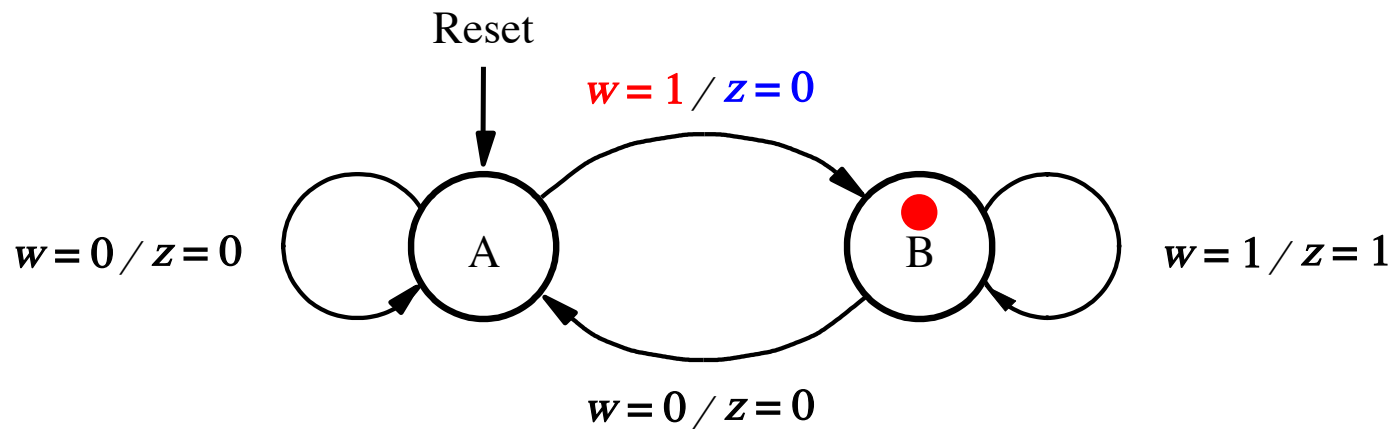
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



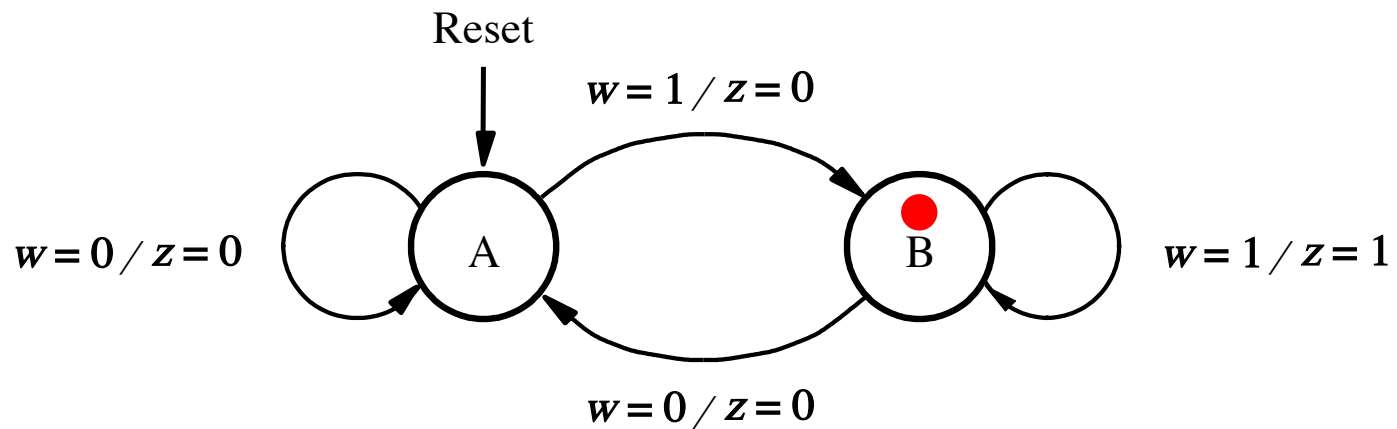
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



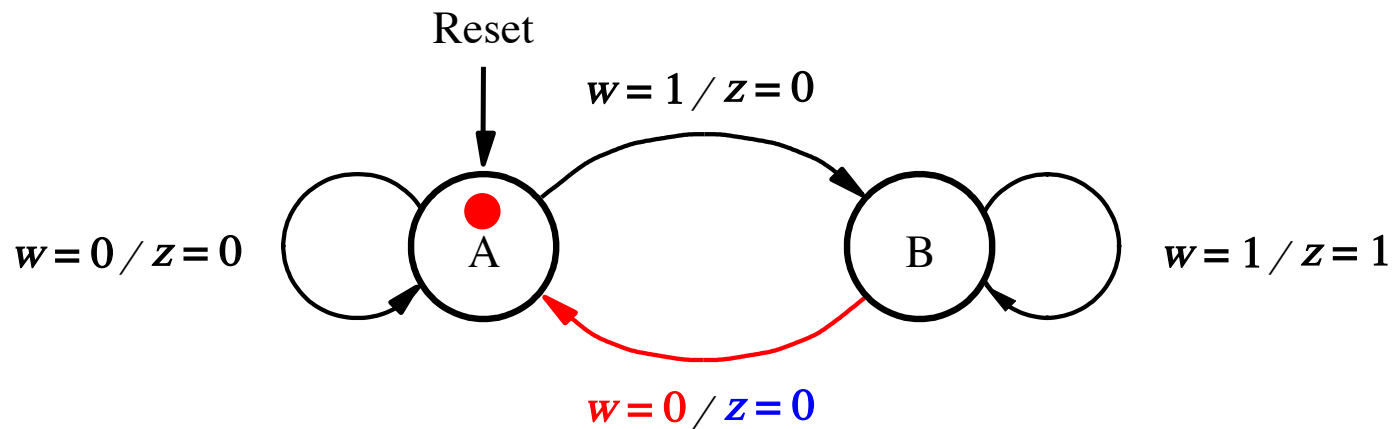
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Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



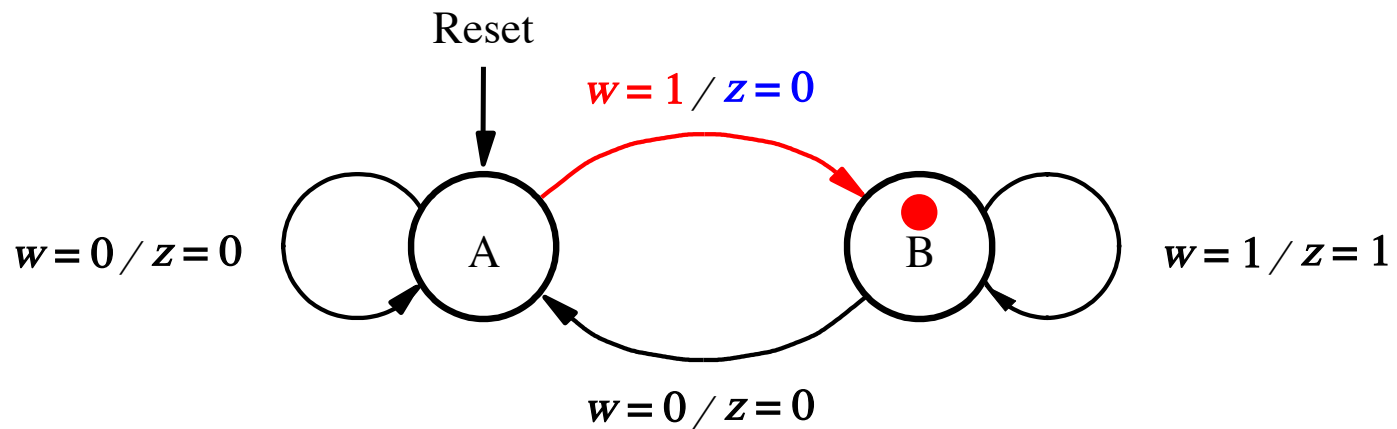
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



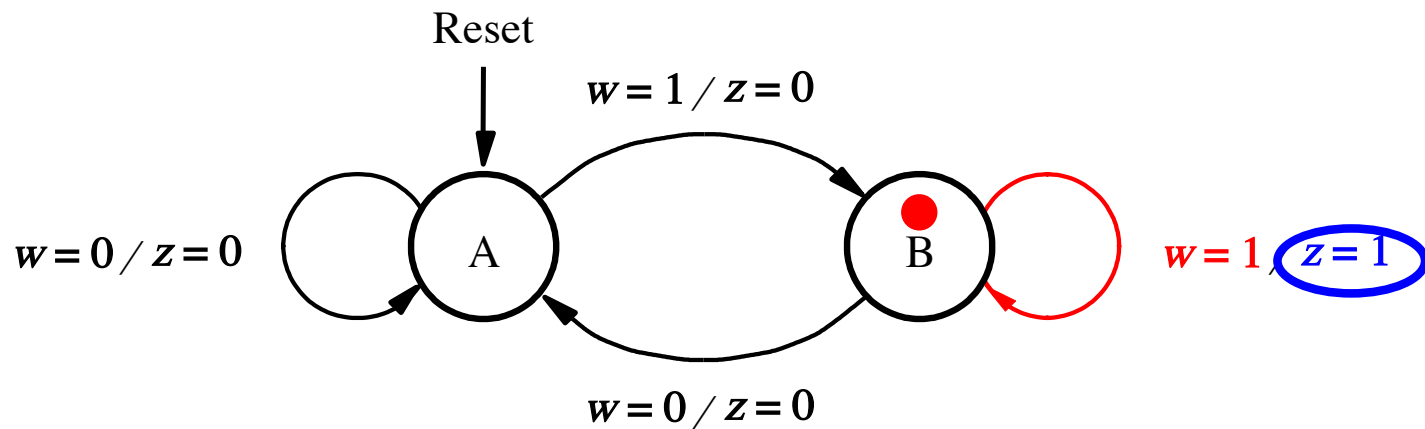
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Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



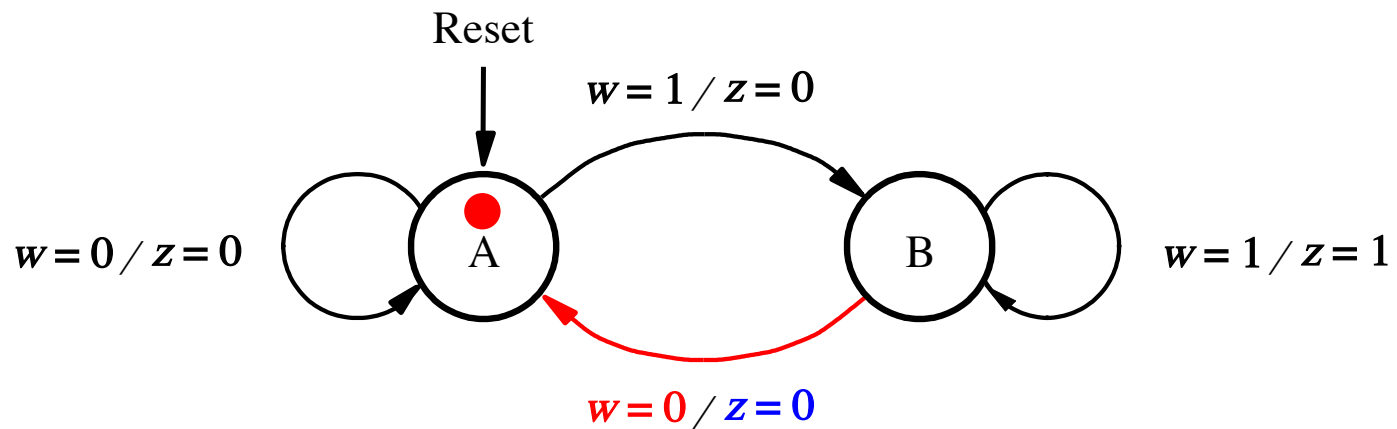
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Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



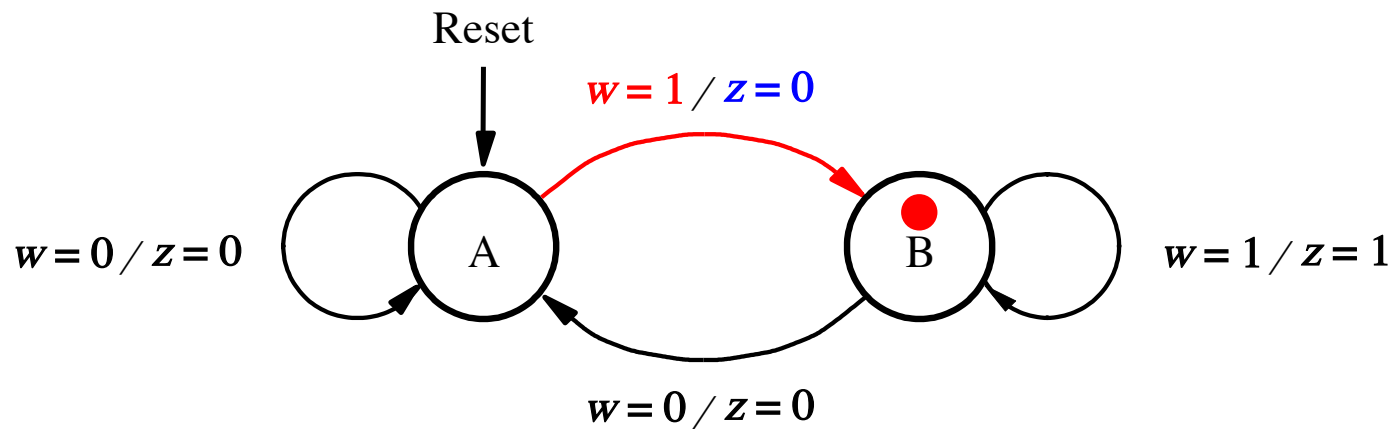
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input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



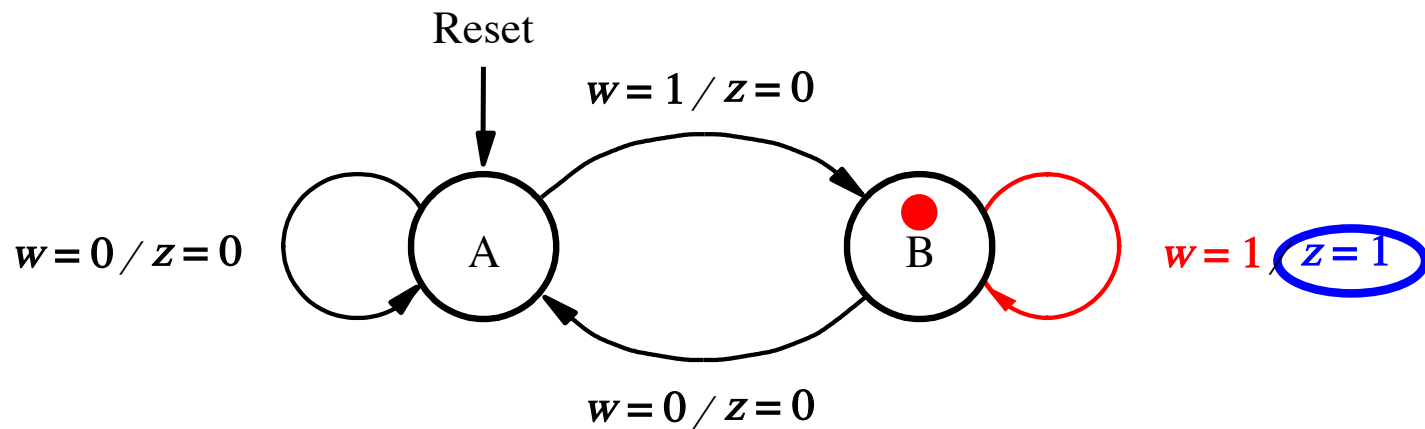
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



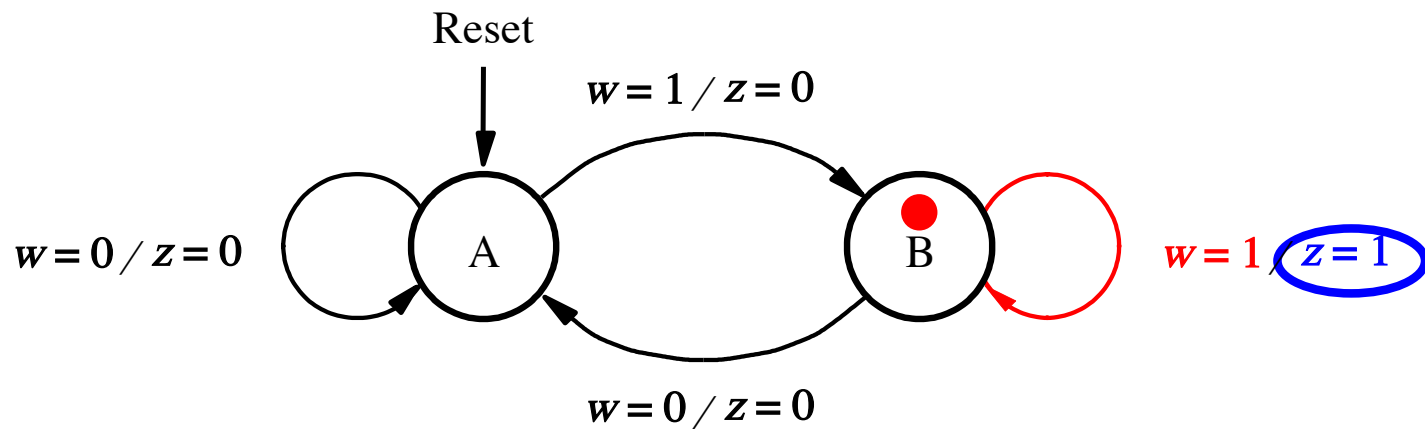
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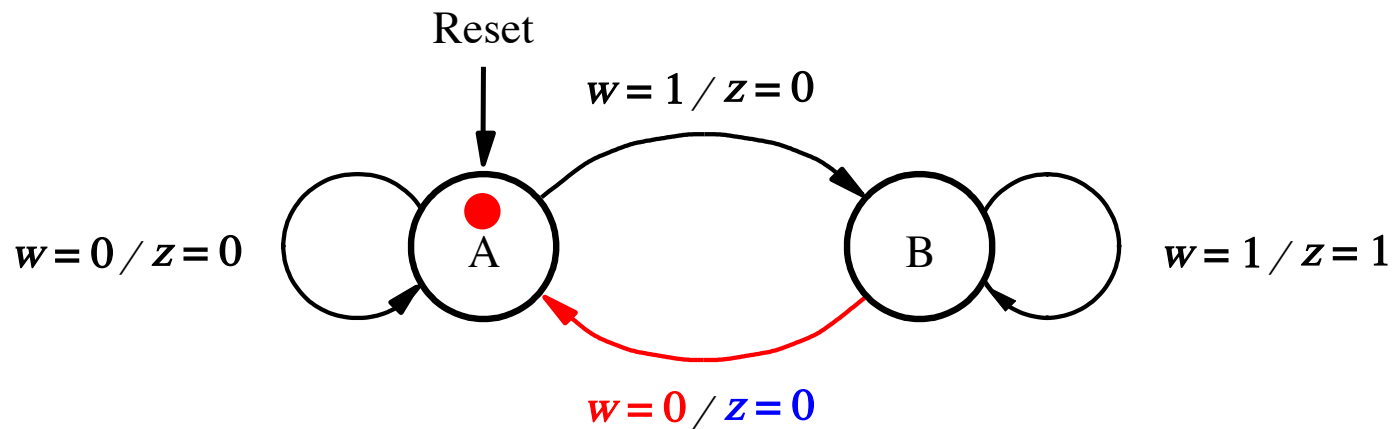
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Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0



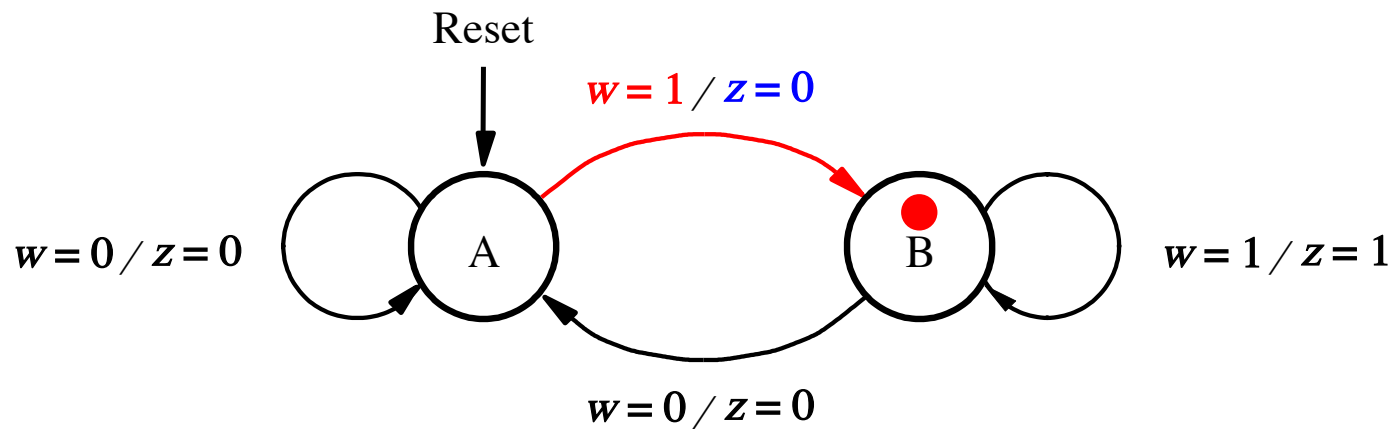
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Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
output z :	0	0	0	0	1	0	0	1	1	0	0

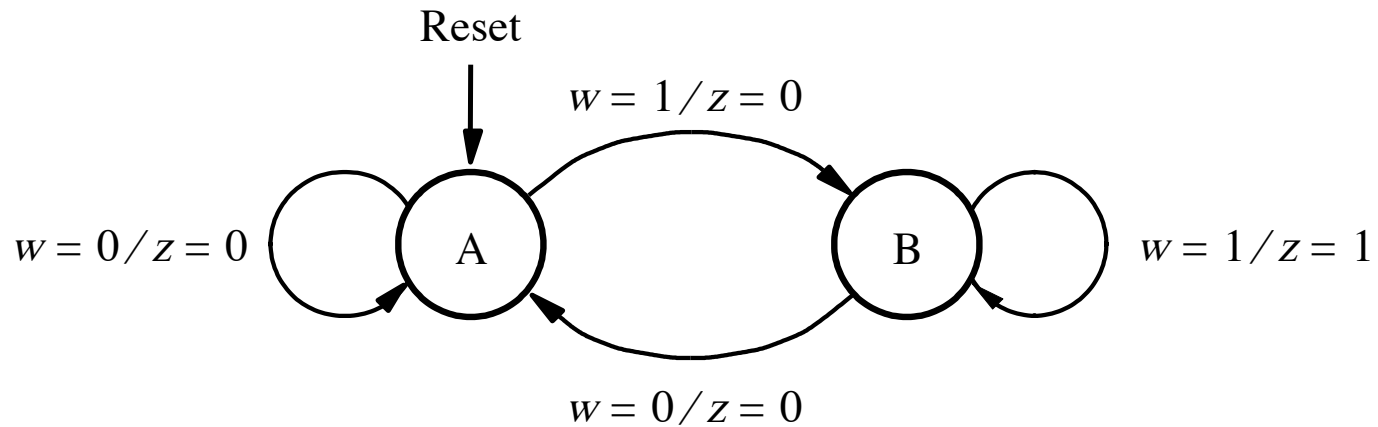


Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w :	0	1	0	1	1	0	1	1	1	0	1
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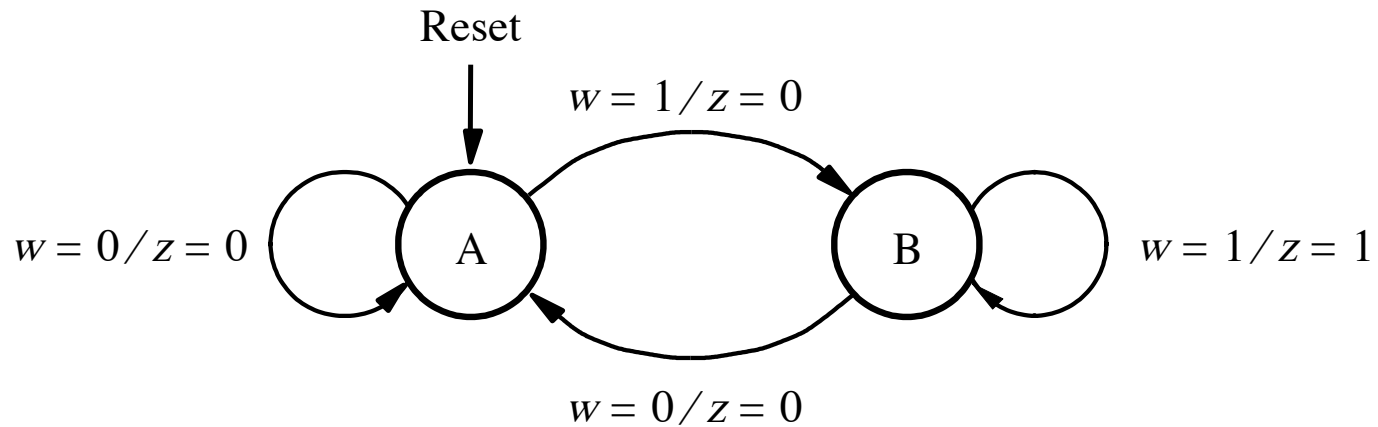


Now Let's Do the State Table for this FSM



Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A				
B				

Now Let's Do the State Table for this FSM



Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

The State Table for this FSM

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

Let's Do the State-assigned Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

Present state	Next state		Output	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
y	Y	Y	z	z
A 0				
B 1				

Let's Do the State-assigned Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

The State-assigned Table

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

The State-assigned Table

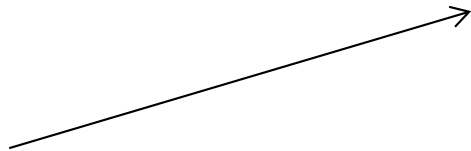
	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

$$Y = D = w \quad z = wy$$

The State-assigned Table

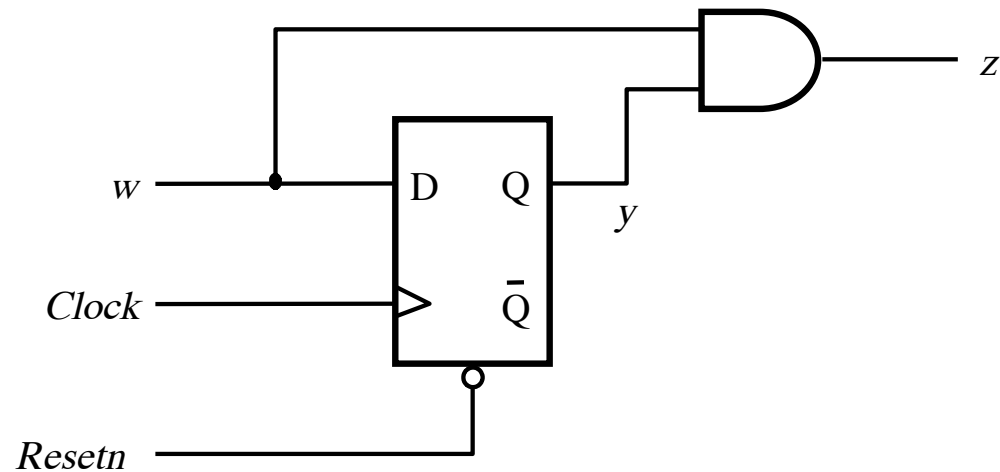
	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

$$Y = D = w \quad z = wy$$



This assumes D flip-flop

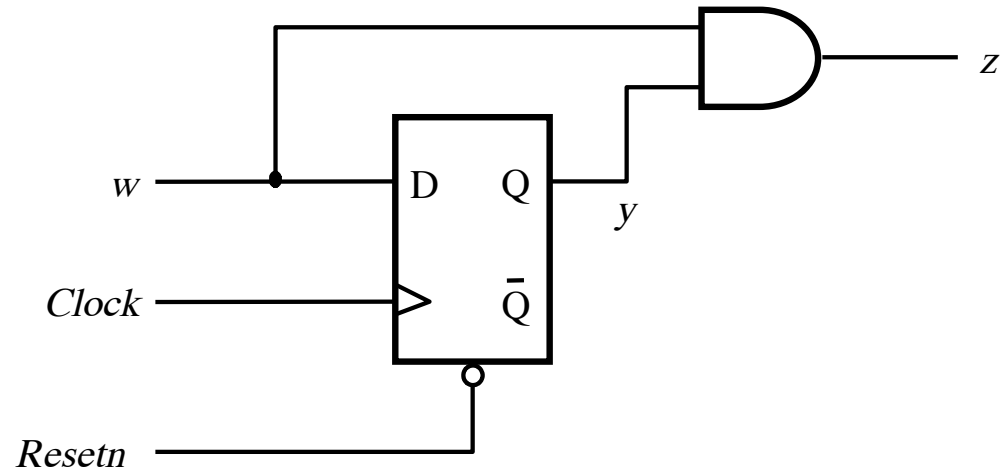
Circuit Implementation of the FSM



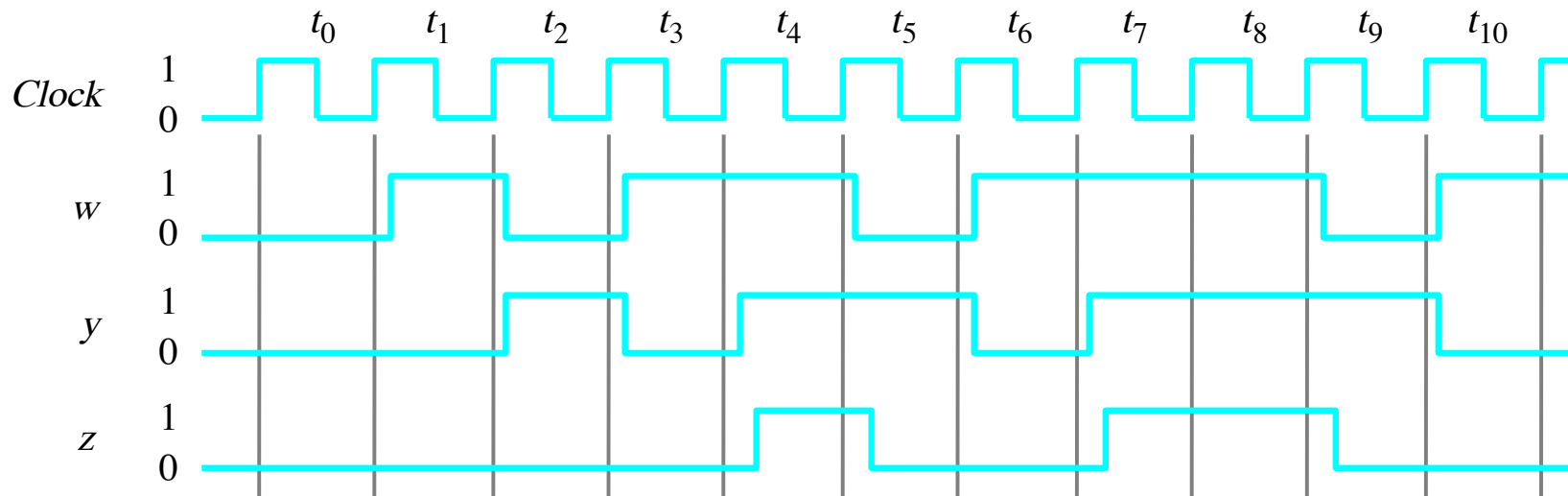
$$Y = D = w$$

$$z = wy$$

Circuit & Timing Diagram



(a) Circuit

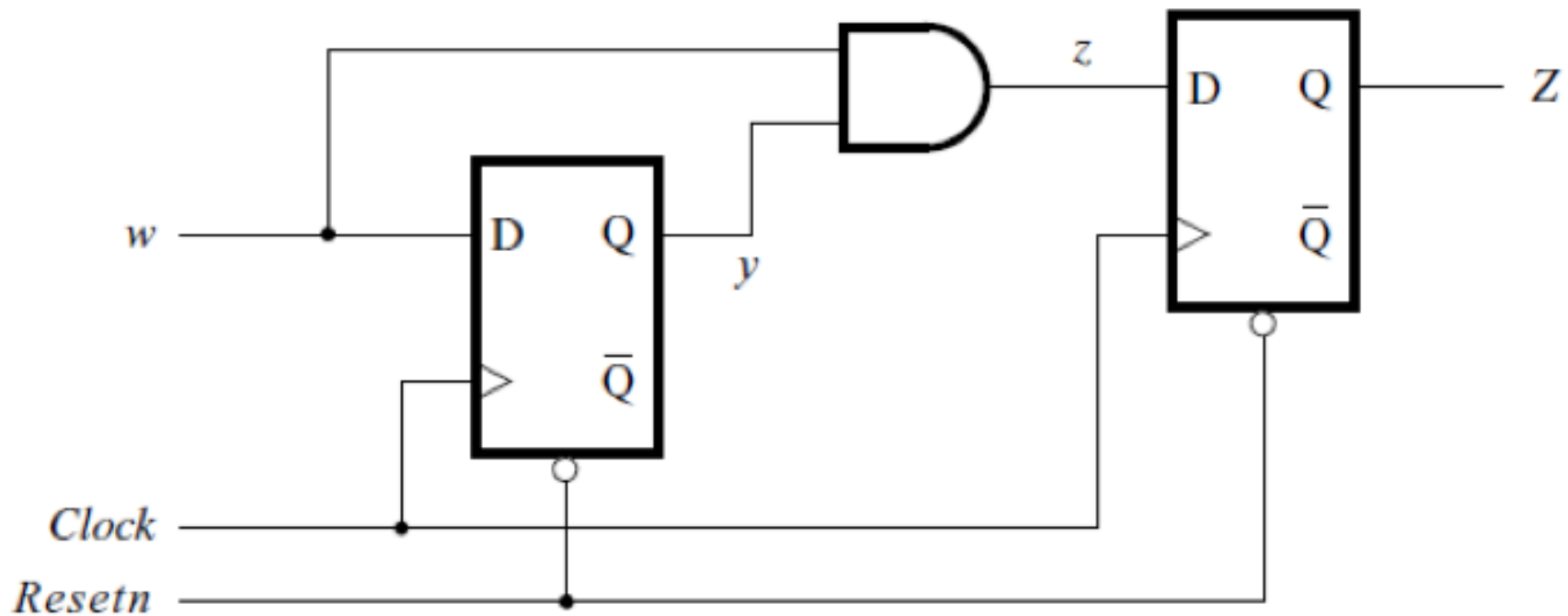


(b) Timing diagram

[Figure 6.26 from the textbook]

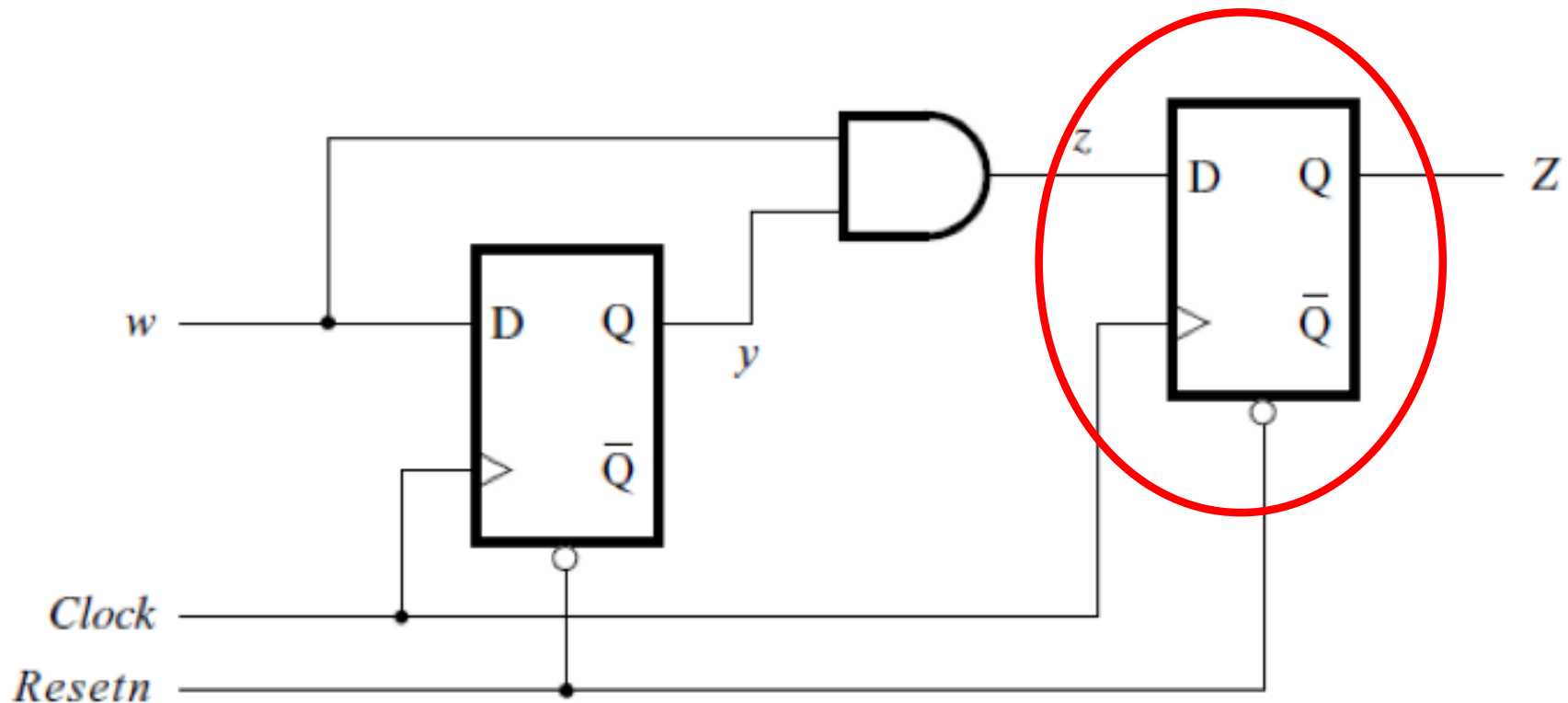
What if we wanted the output signal to be delayed by 1 clock cycle?

Circuit Implementation of the Modified FSM



[Figure 6.27a from the textbook]

Circuit Implementation of the Modified FSM



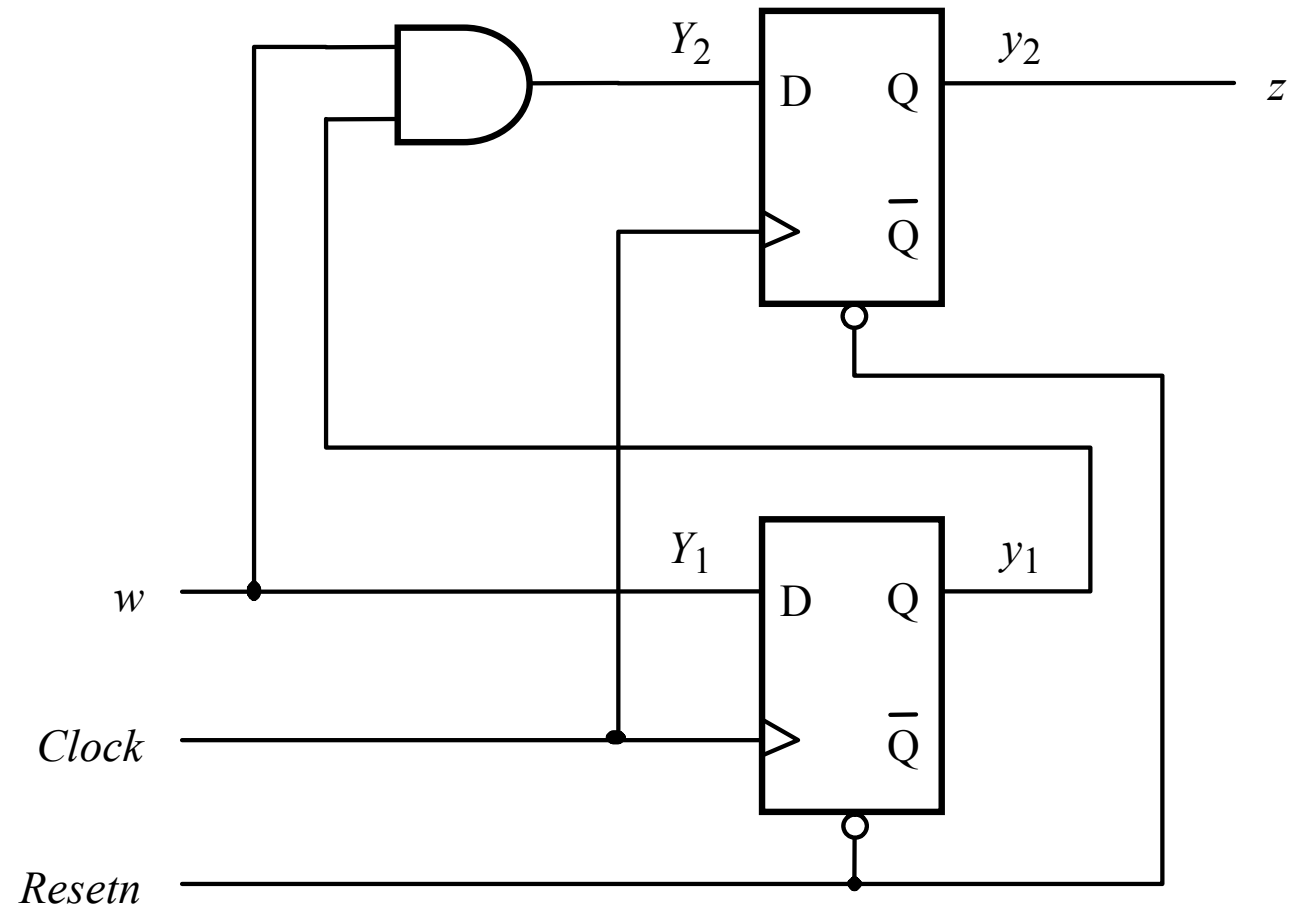
This flip-flop delays the output signal by one clock cycle

We Have Seen This Diagram Before

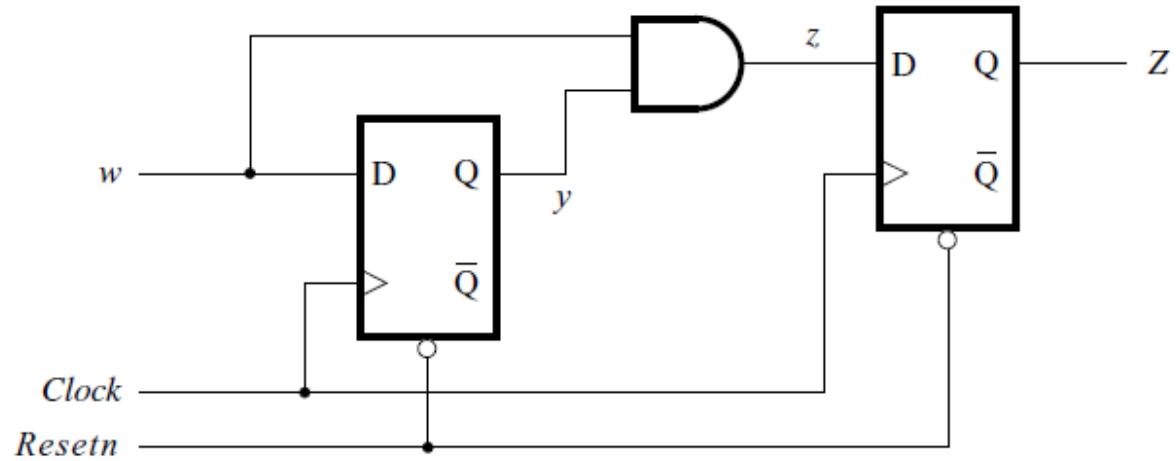
$$Y_1(w, y_2, y_1) = w$$

$$Y_2(w, y_2, y_1) = wy_1$$

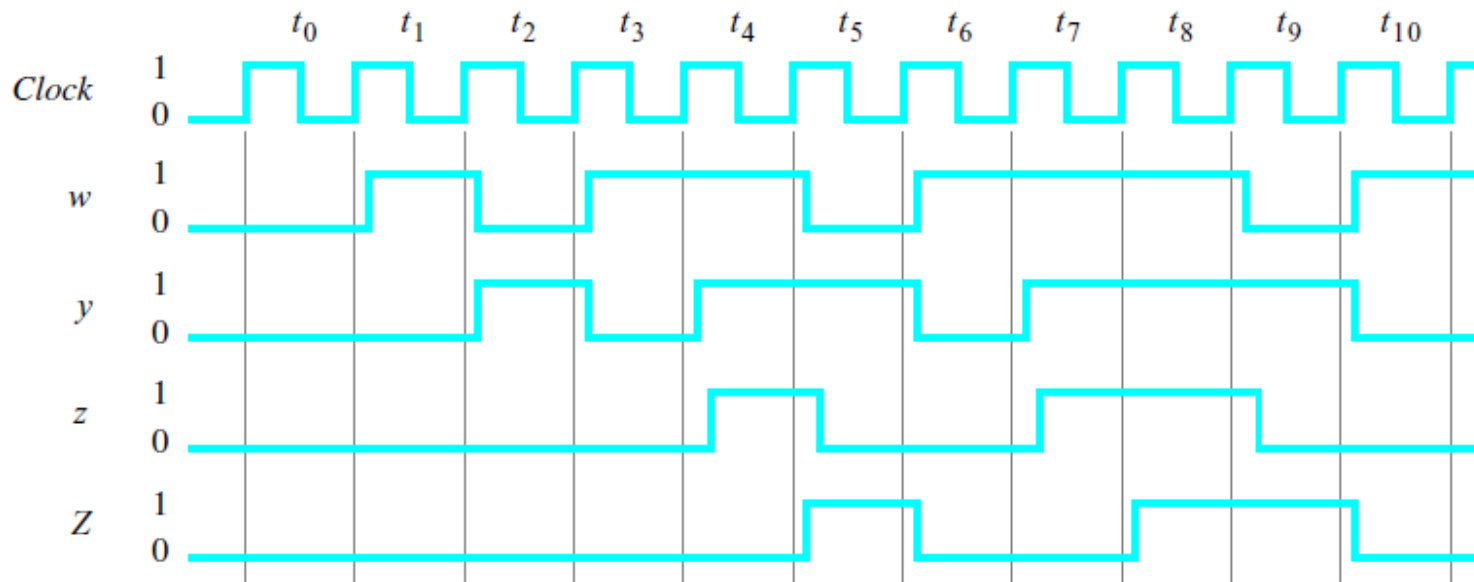
$$z(y_2, y_1) = y_2$$



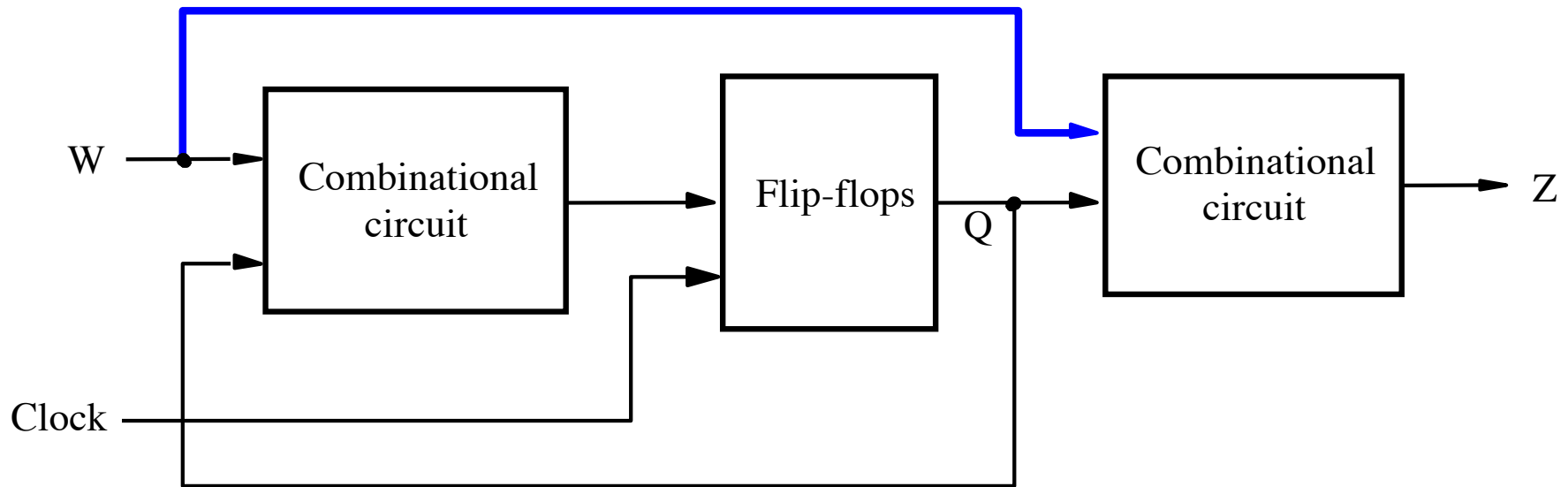
Circuit & Timing Diagram



(a) Circuit

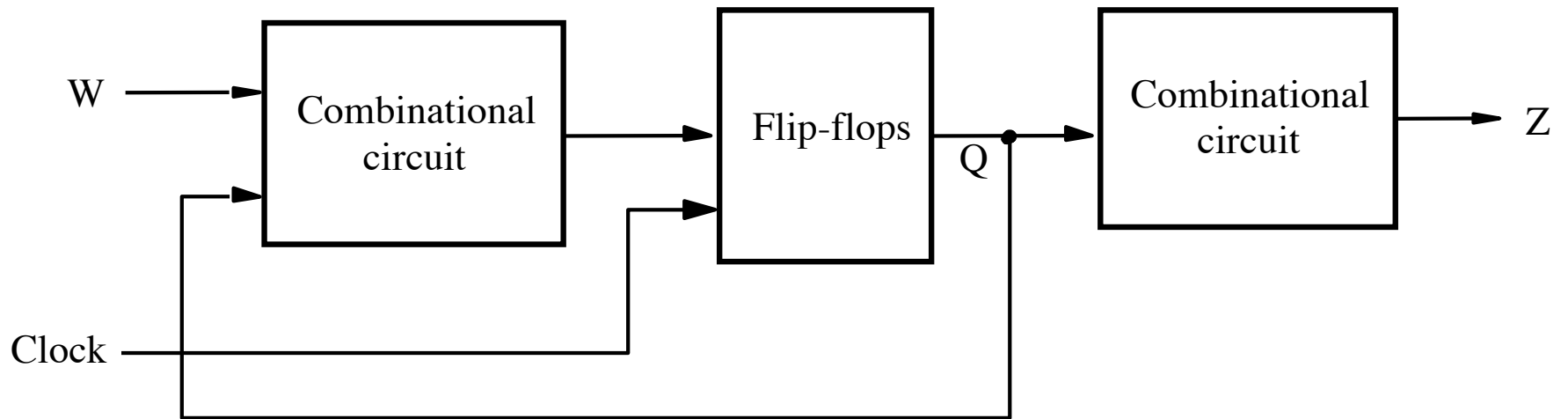


The general form of a synchronous sequential circuit

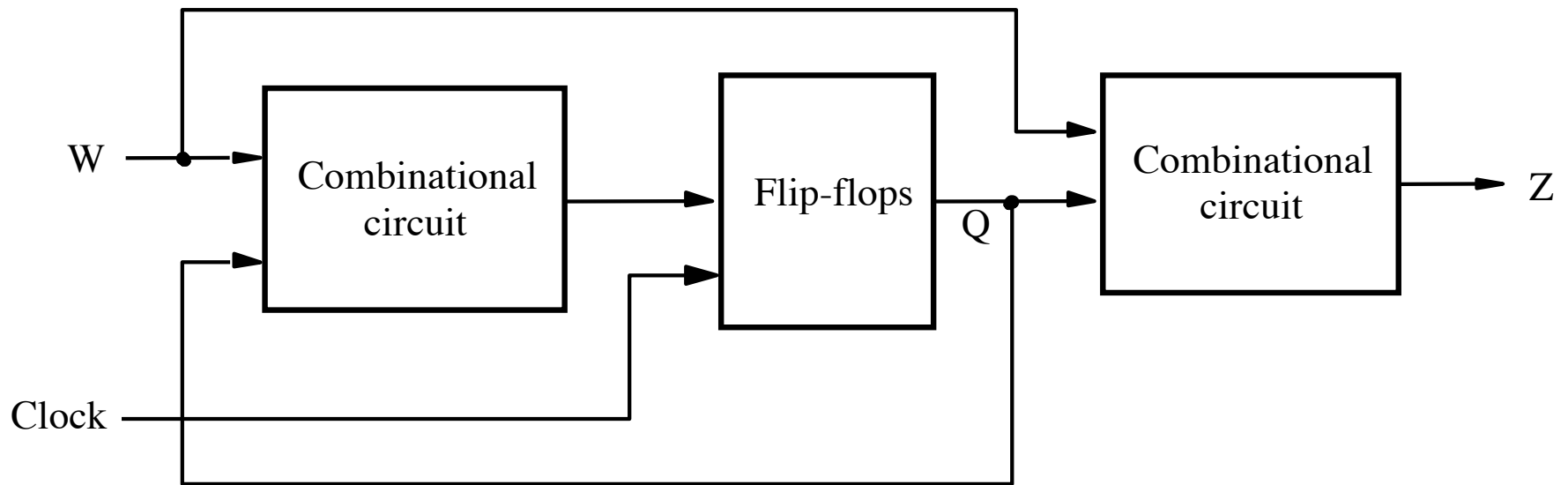


[Figure 6.1 from the textbook]

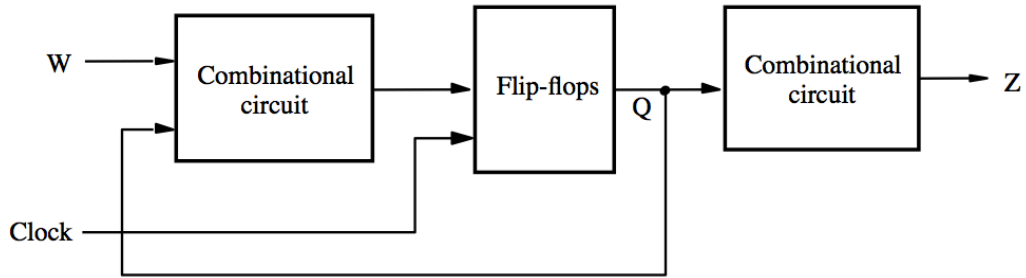
Moore Type



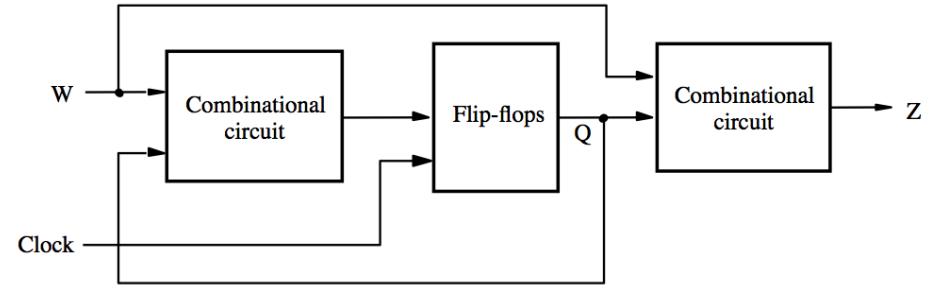
Mealy Type



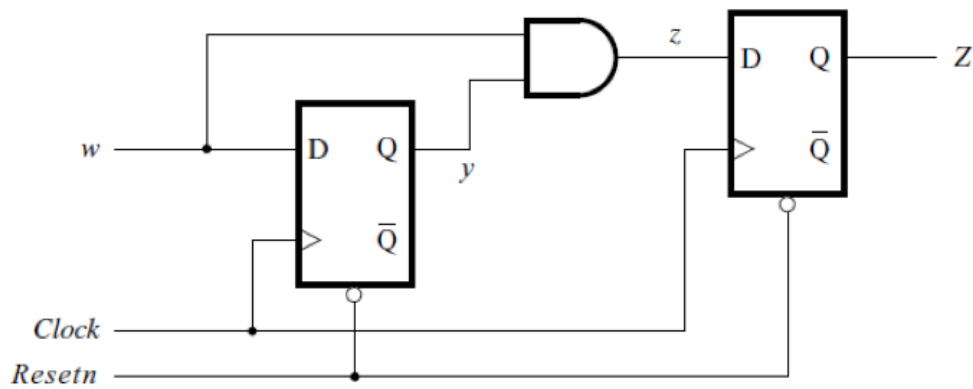
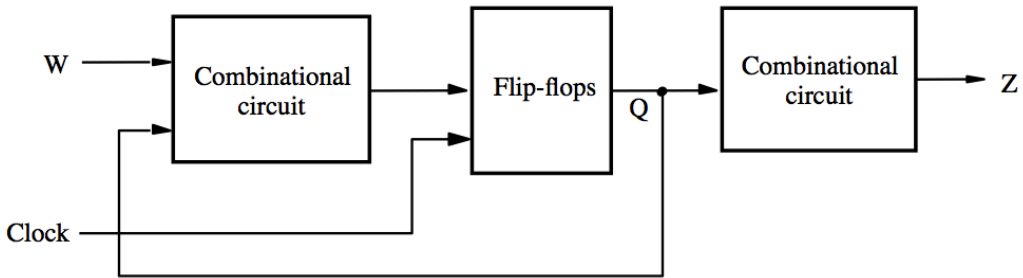
Moore



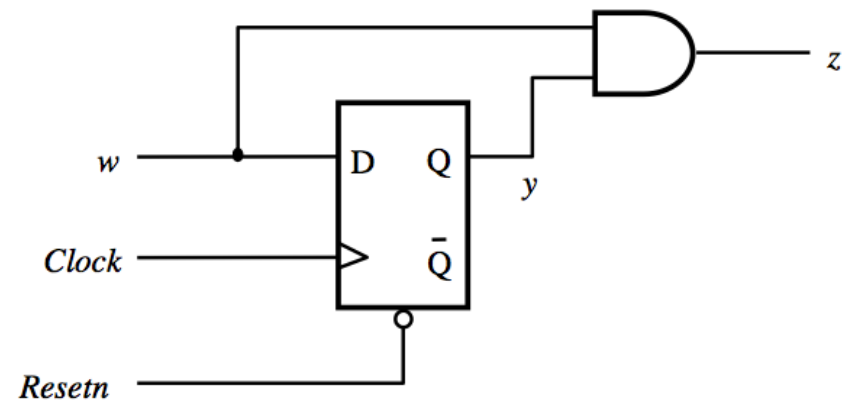
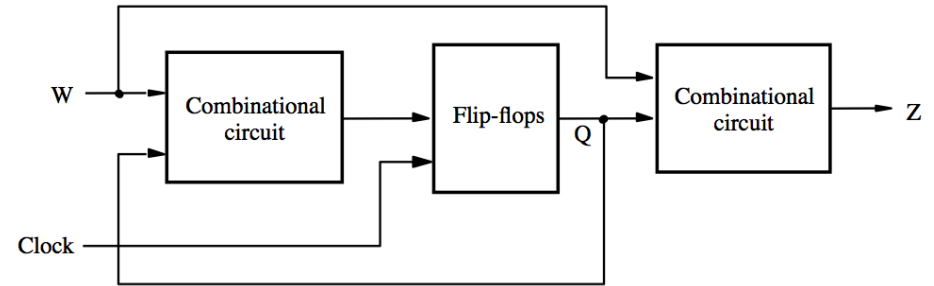
Mealy



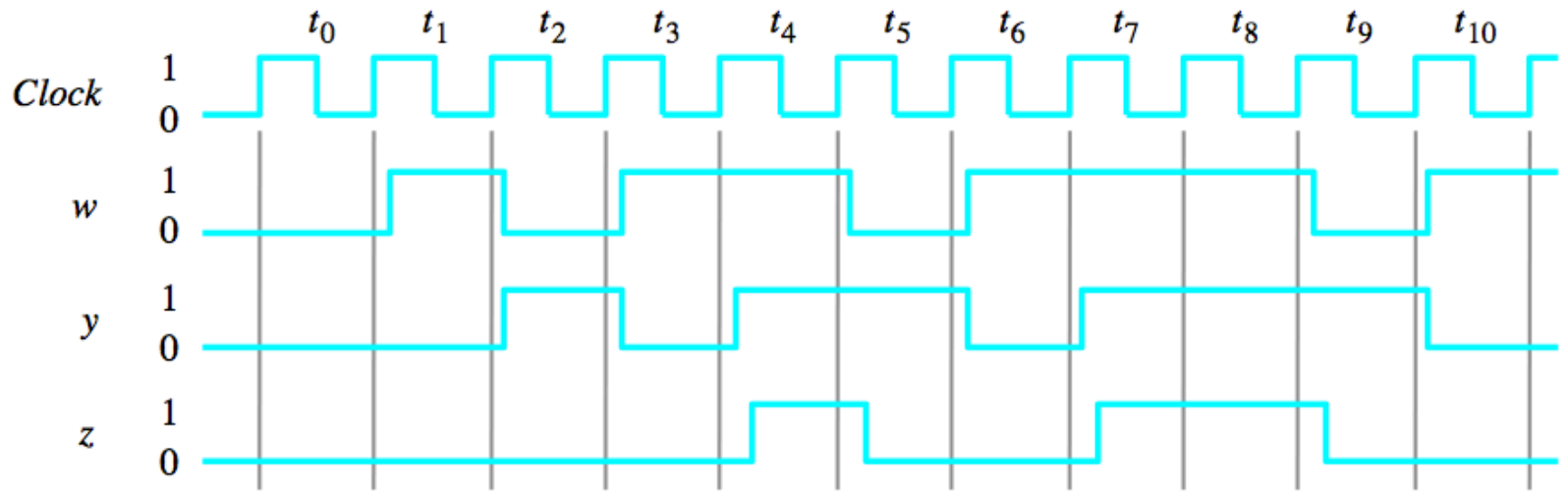
Moore



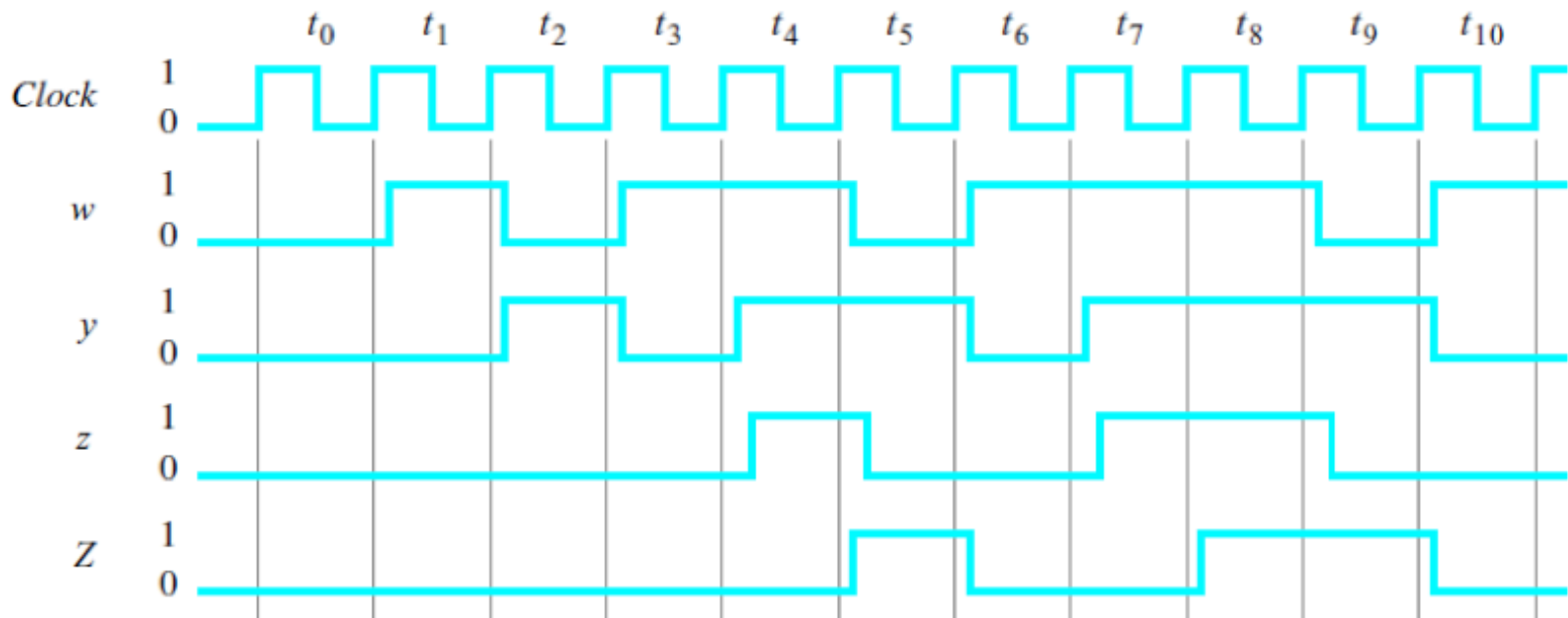
Mealy



Mealy

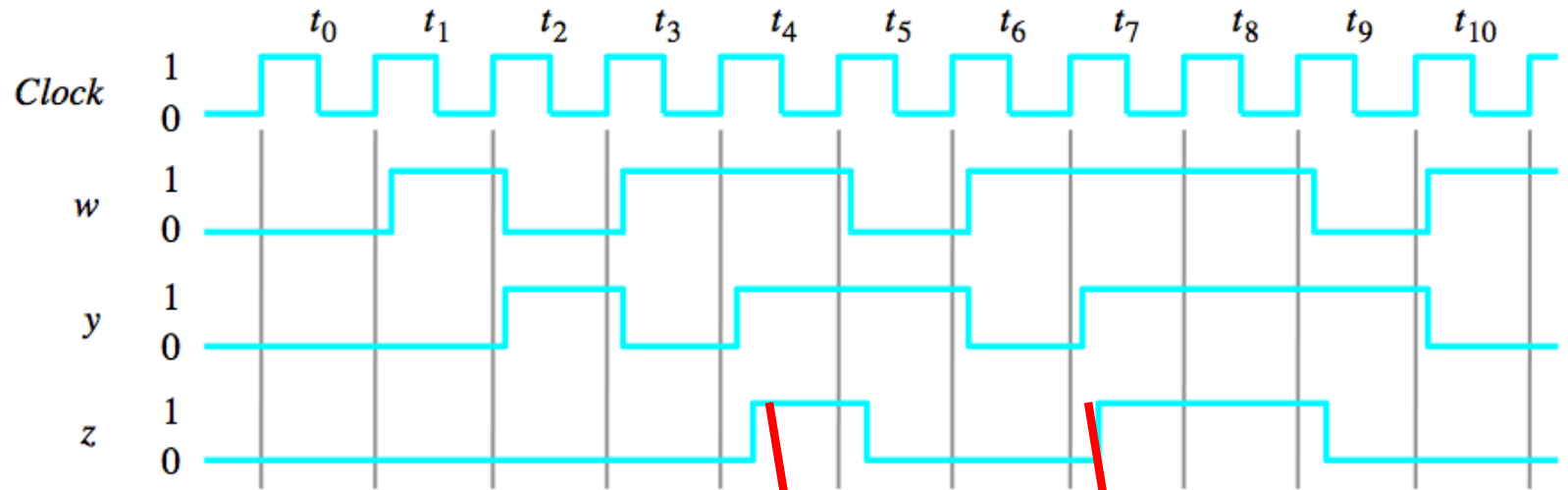


Moore

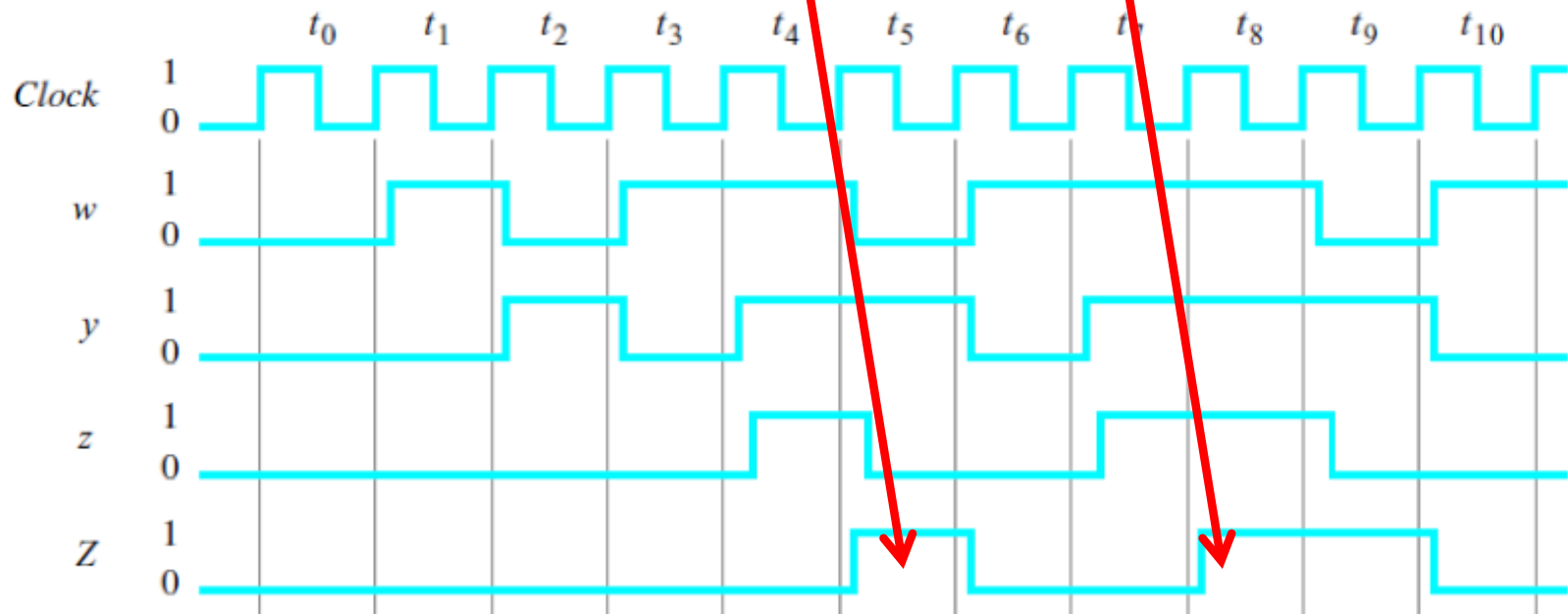


Notice that the output of the Moore machine is delayed by one clock cycle

Mealy



Moore



Questions?

THE END