

# **CprE 281: Digital Logic**

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http://www.ece.iastate.edu/~alexs/classes/

## **State Minimization**

CprE 281: Digital Logic Iowa State University, Ames, IA Copyright © Alexander Stoytchev

## **Administrative Stuff**

- Final Project
- Posted on the class web page (Labs section)
- Pick one of the problems and solve it.
- Your grade will not depend on which project you pick
- By next Wednesday you need to select your project and send an e-mail to your lab TAs

## Sample E-mail

Hello TAs,

I decided to pick problem number x for my final project in CprE 281.

Thanks,

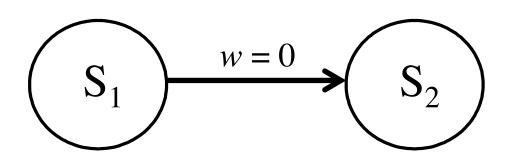
[your name, your lab section]

## **Equivalence of states**

"Two states  $S_i$  and  $S_j$  are said to be equivalent if and only if for every possible input sequence, the same output sequence will be produced regardless of whether  $S_i$  or  $S_j$  is the initial state."

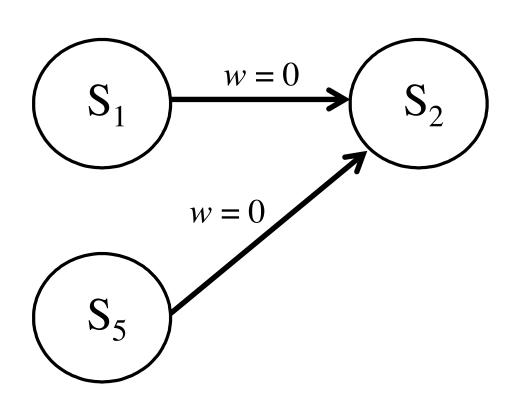
## **Partition Minimization Procedure**

#### Assuming that we have only one input signal w



S<sub>2</sub> is a 0-successor of S<sub>1</sub>

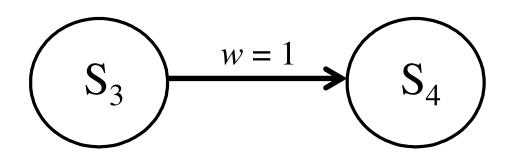
#### Assuming that we have only one input signal w



 $S_2$  is a 0-successor of  $S_1$ 

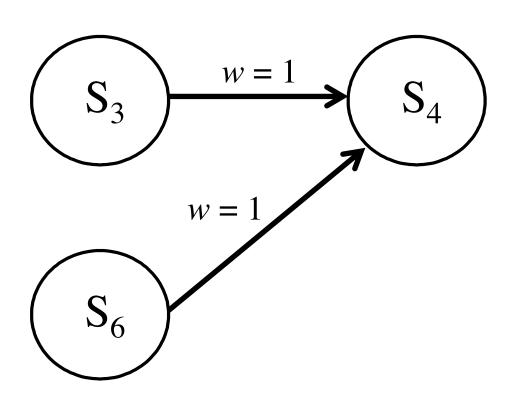
S<sub>2</sub> is a 0-successor of S<sub>5</sub>

Assuming that we have only one input signal w



 $S_4$  is a 1-successor of  $S_3$ 

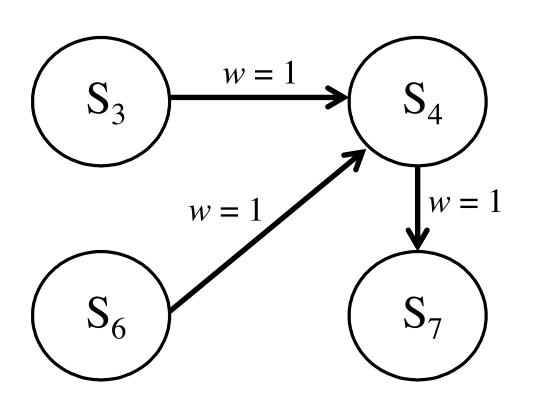
#### Assuming that we have only one input signal w



 $S_4$  is a 1-successor of  $S_3$ 

S<sub>4</sub> is a 1-successor of S<sub>6</sub>

#### Assuming that we have only one input signal w



 $S_4$  is a 1-successor of  $S_3$ 

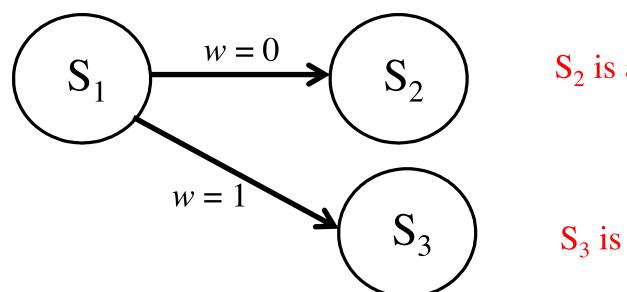
S<sub>4</sub> is a 1-successor of S<sub>6</sub>

 $S_7$  is a 1-successor of  $S_4$ 

Assuming that we have only one input signal w, then k can only be equal to 0 or 1.

Assuming that we have only one input signal w, then k can only be equal to 0 or 1.

In other words, this is the familiar 0-successor or 1-successor case.

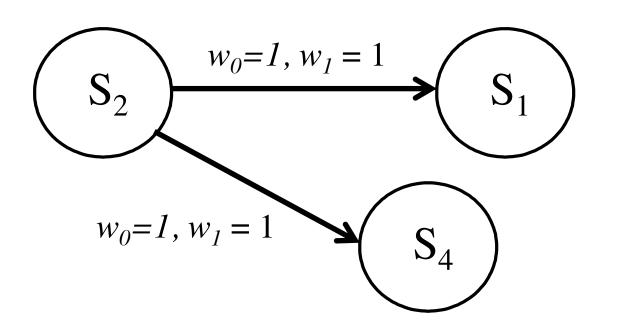


S<sub>2</sub> is a 0-successor of S<sub>1</sub>

 $S_3$  is a 1-successor of  $S_1$ 

If we have two input signals, e.g.,  $w_0$  and  $w_1$ , then k can only be equal to 0,1, 2, or 3.

If we have two input signals, e.g.,  $w_0$  and  $w_1$ , then k can only be equal to 0,1, 2, or 3.



 $S_1$  is a 3-successor of  $S_2$ 

 $S_4$  is a 3-successor of  $S_2$ 

## **Equivalence of states**

"If states  $S_i$  and  $S_j$  are equivalent, then their corresponding k-successors (for all k) are also equivalent."

#### **Partition**

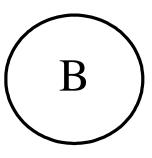
"A partition consists of one or more blocks, where each block comprises a subset of states that may be equivalent, but the states in a given block are definitely not equivalent to the states in other blocks."

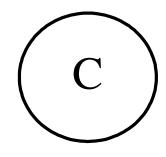
## State Table for This Example

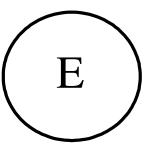
Present	Next	Output	
state	w = 0	w = 1	Z
A	В	С	1
В	D	F	1
C	F	E	0
D	В	G	1
E	F	C	0
F	Е	D	0
G	F	G	0

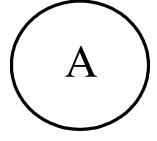
# State Diagram (just the states)

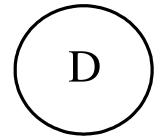
Present	Next state		Output
state	w = 0	w = 1	z
A	В	C	1
В	D	F	1
C	F	E	0
D	В	G	1
Е	F	C	0
F	E	D	0
G	F	G	0

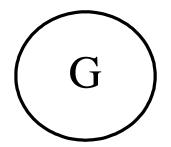


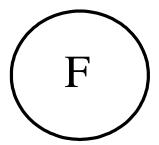








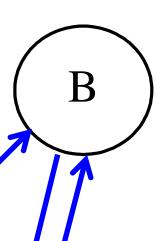


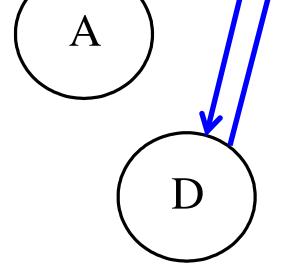


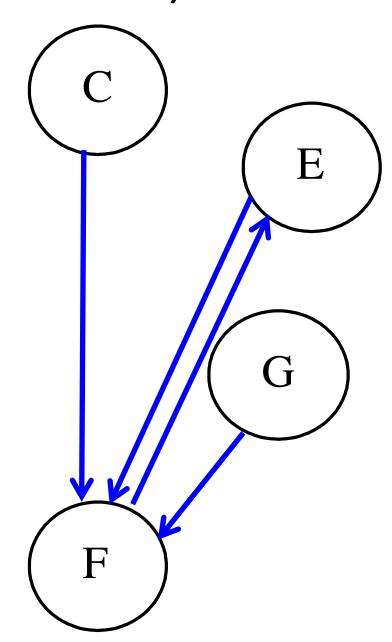
## **State Diagram**

(transitions when w=0)

Present	Nex	Output	
state	w = 0	w = 1	z
A	В	С	1
В	D	F	1
C	F	Е	0
D	В	G	1
E	F	C	0
F	Е	D	0
G	F	G	0

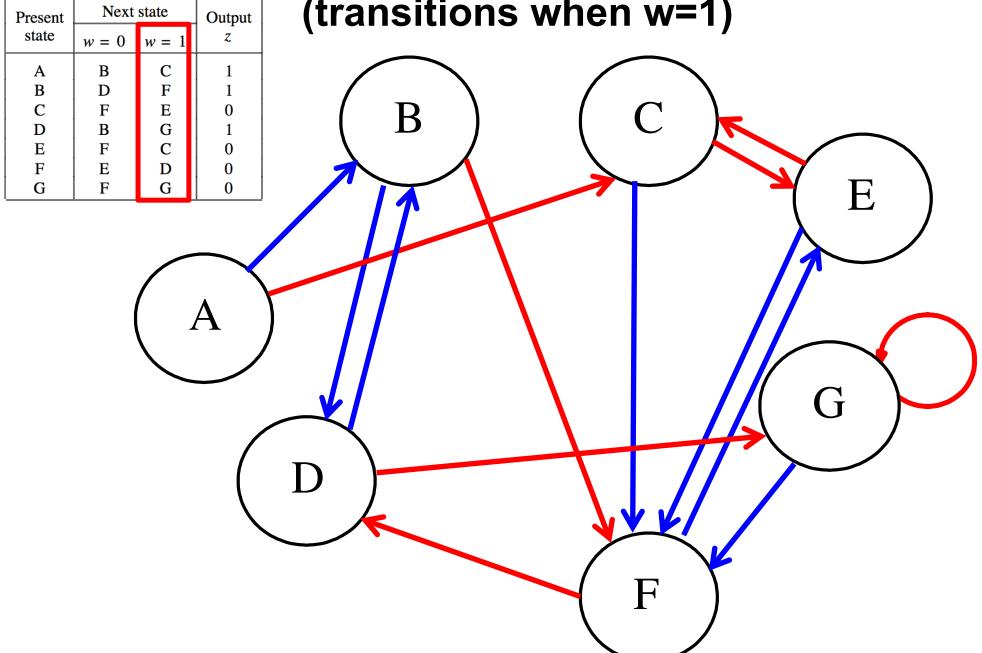






## **State Diagram**

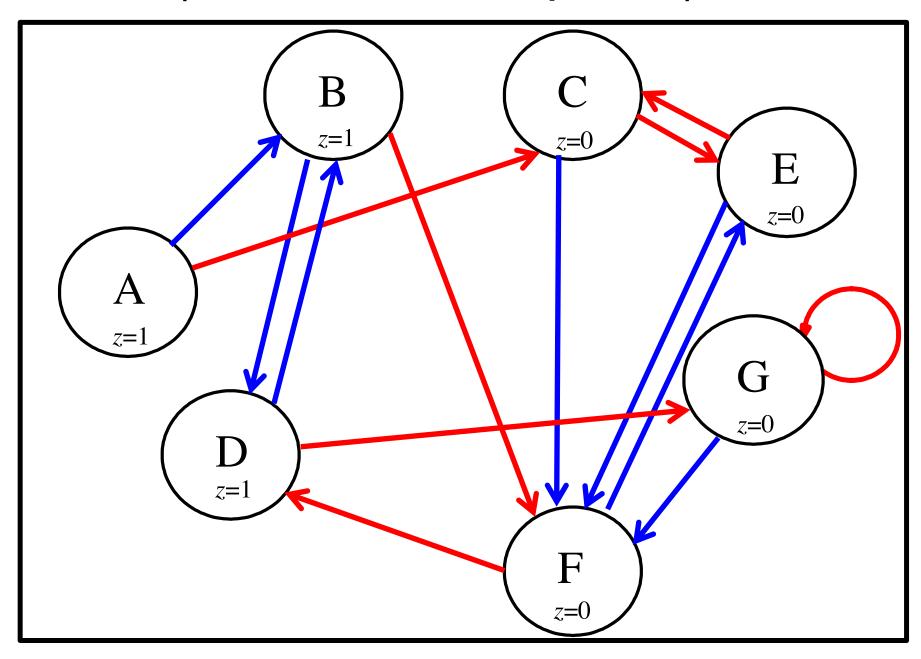
(transitions when w=1)



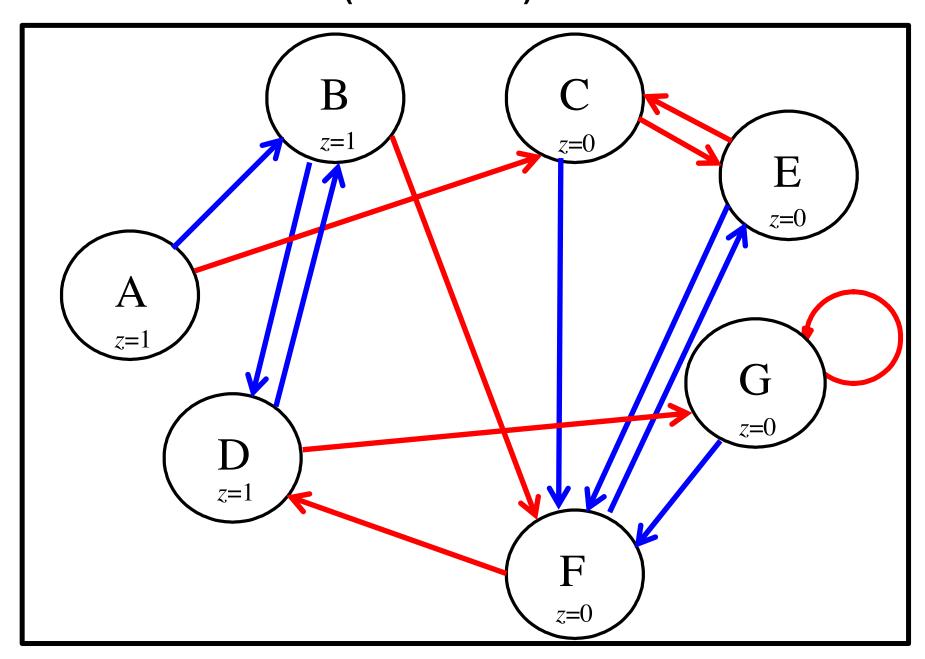
## **Outputs**

Present	Next	state	Output	
state	w = 0	w = 1	z	
Α	В	С	1	
B	D	F	1	
C	F	F E G	0	$\begin{pmatrix} \mathbf{B} \\ z=1 \end{pmatrix} \qquad \begin{pmatrix} \mathbf{C} \\ z=0 \end{pmatrix}$
D	В	G	1	$\begin{array}{c} B \\ z=1 \end{array}$
E	F	C	0	
F	E	D	0	z=1
G	F	G	0	E $z=0$
				z=0
			1	
	1	(	٨	
		\	A =1/	
			1	
			;=1	
				C
				z=0
				D $z=1$
				$\zeta=1$
				$\mathbf{F}$
				$\begin{pmatrix} \mathbf{F} \\ z=0 \end{pmatrix}$
				$\mathbf{z}=0$

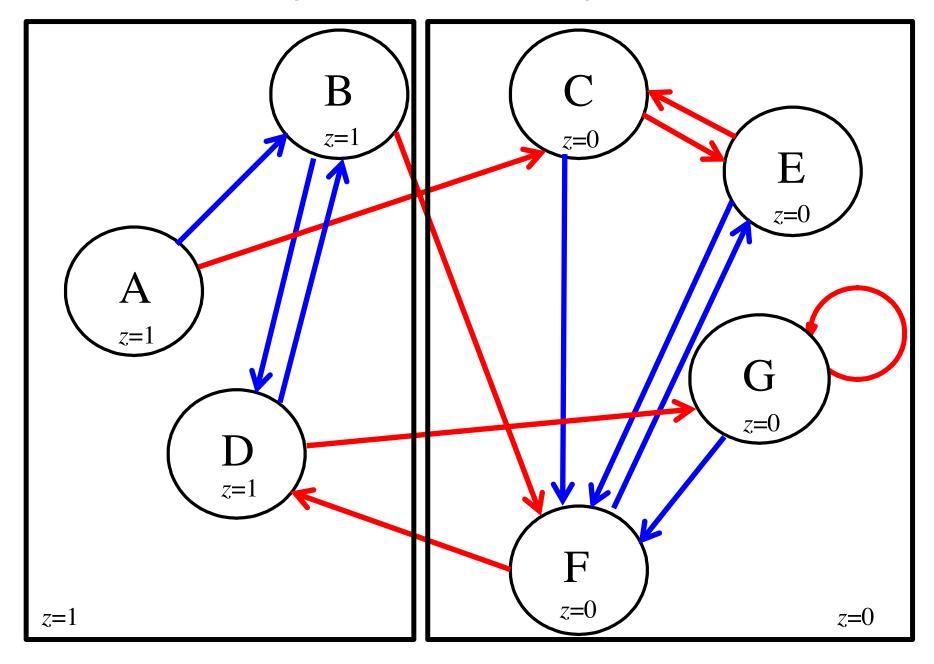
(All states in the same partition)



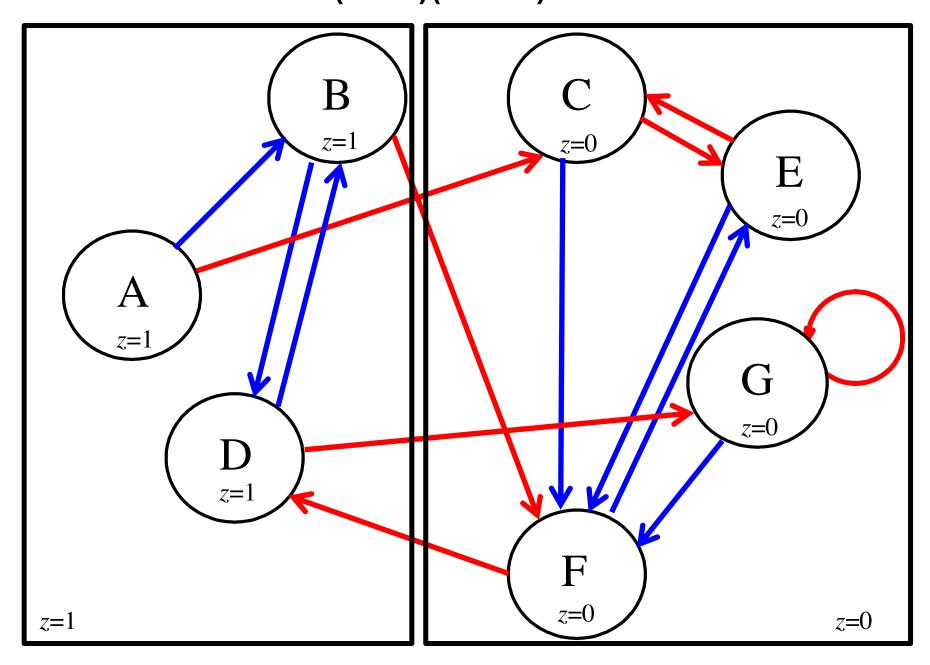
## Partition #1 (ABCDEFG)



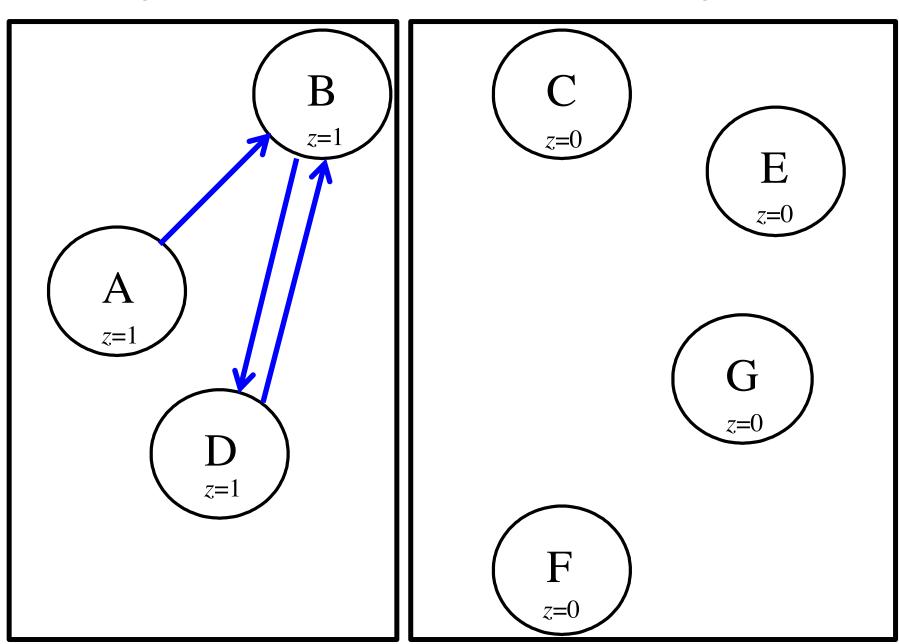
(based on outputs)



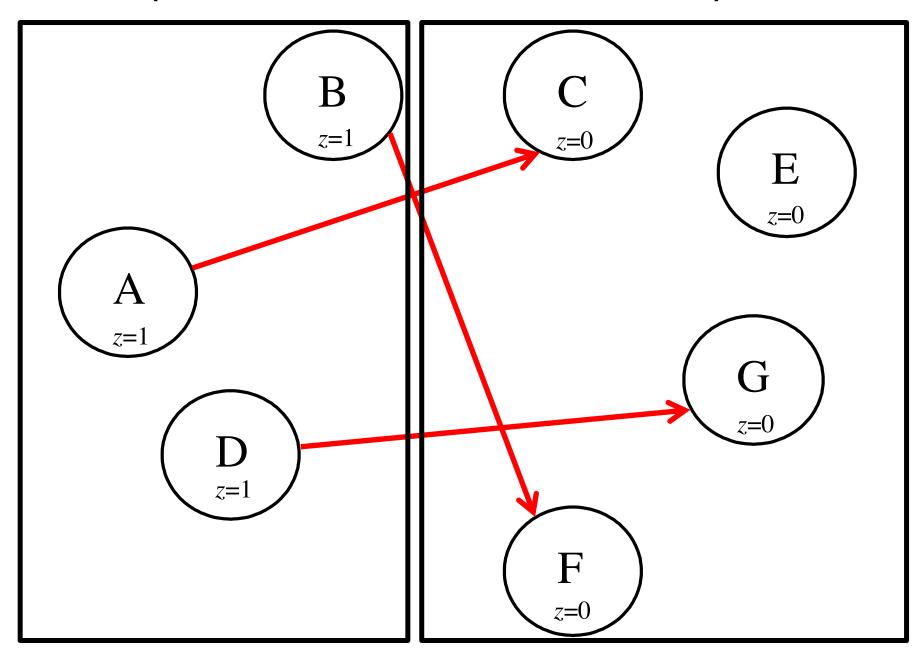
## Partition #2 (ABD)(CEFG)



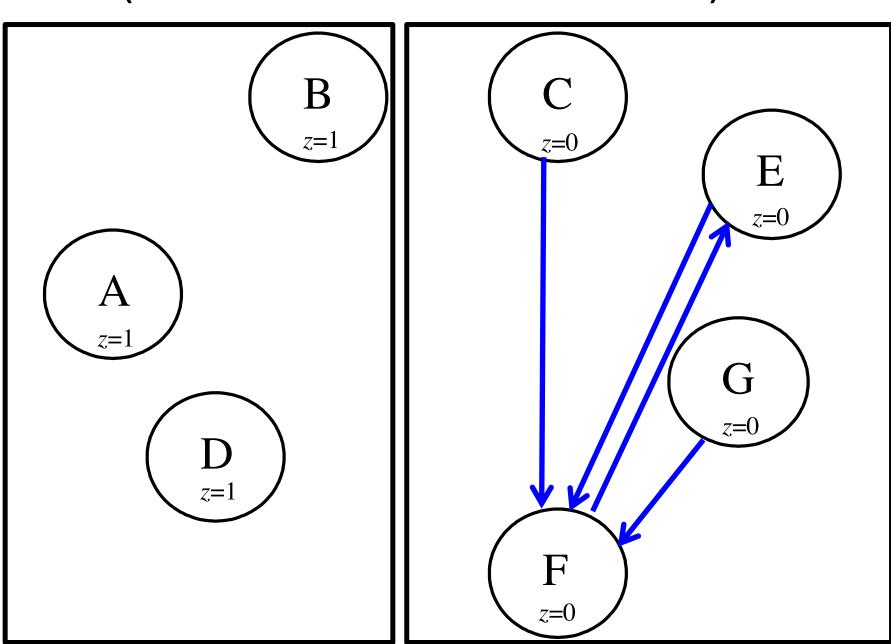
(Examine the 0-successors of ABD)



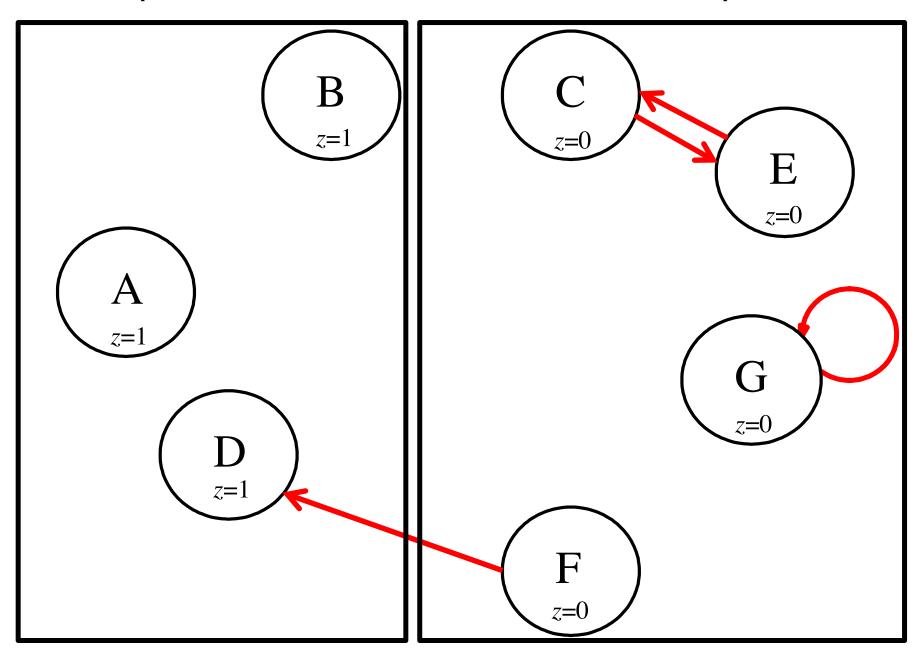
(Examine the 1-successors of ABD)



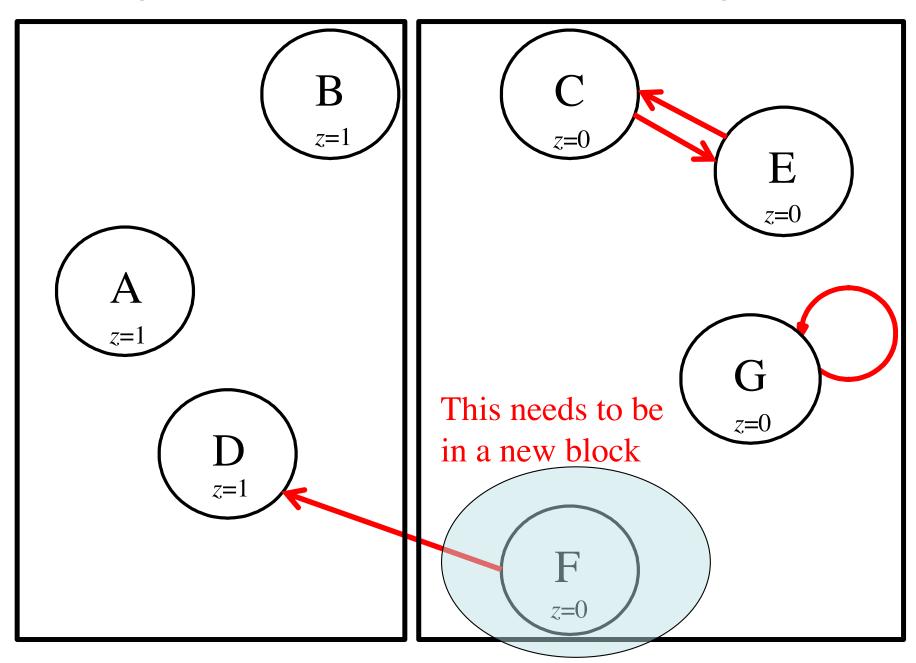
(Examine the 0-successors of CEFG)



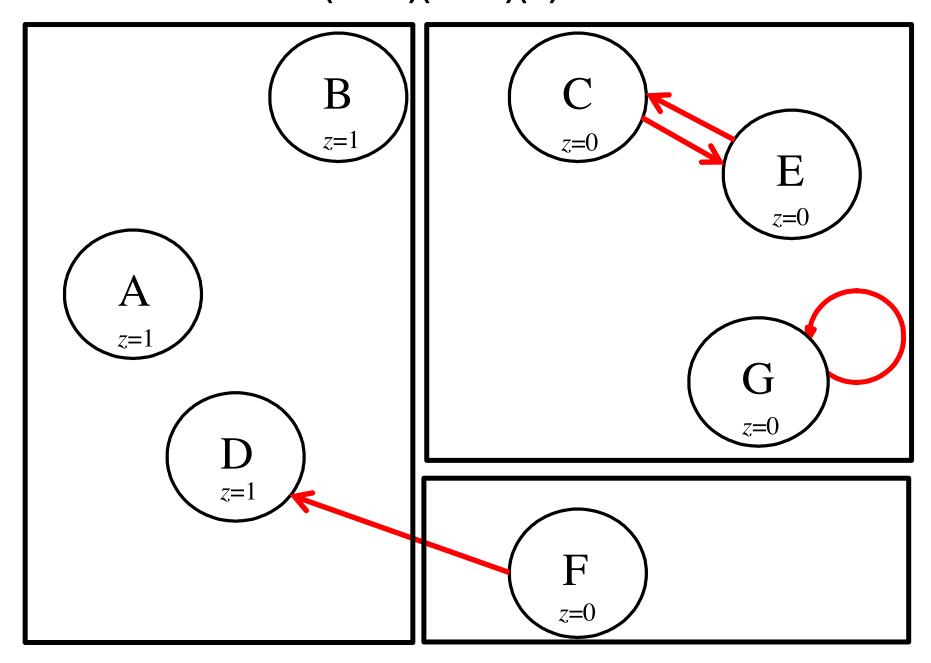
(Examine the 1-successors of CEFG)



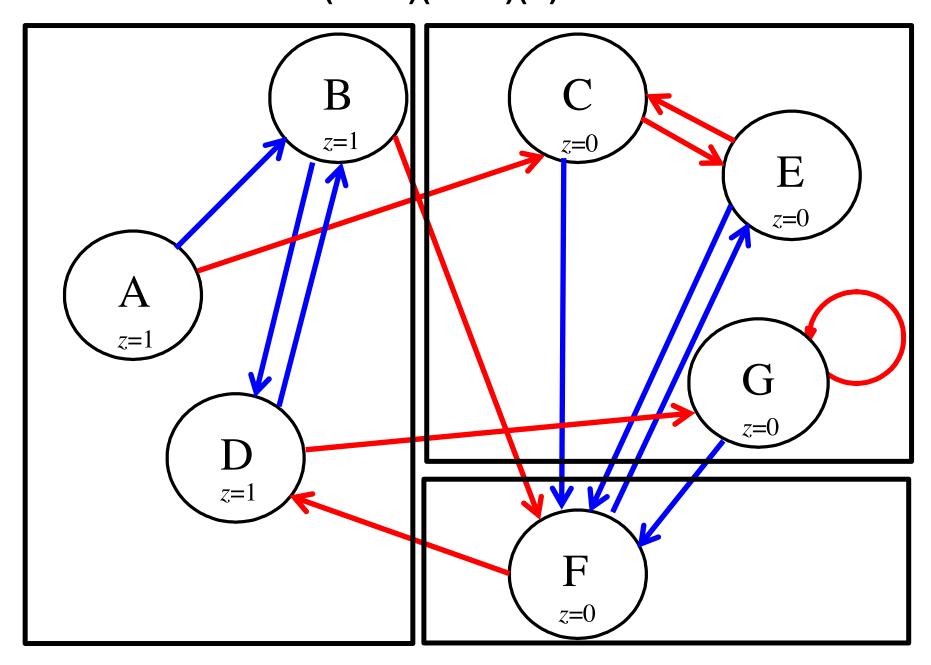
(Examine the 1-successors of CEFG)



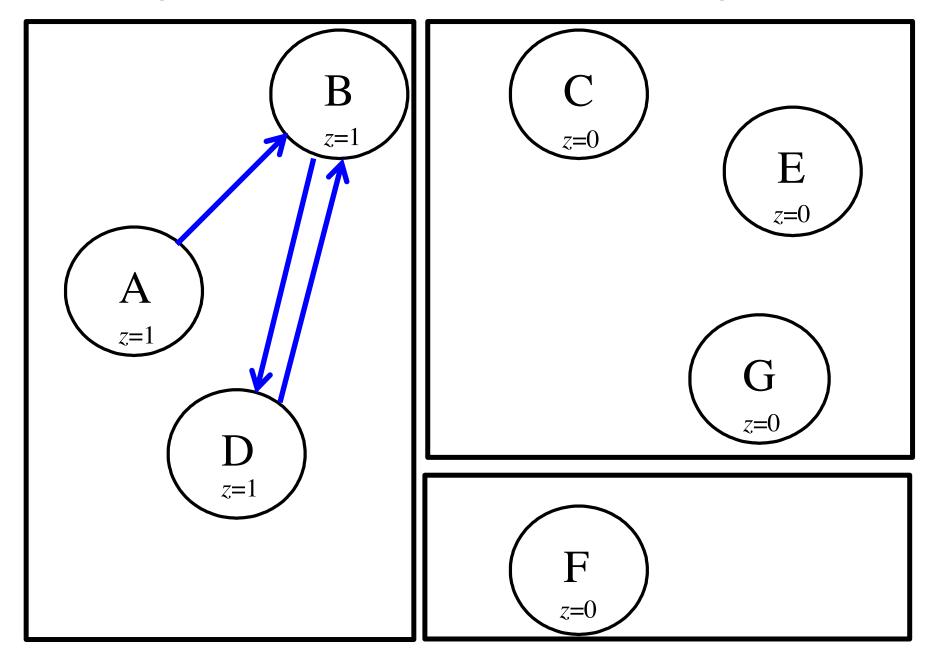
## Partition #3 (ABD)(CEG)(F)



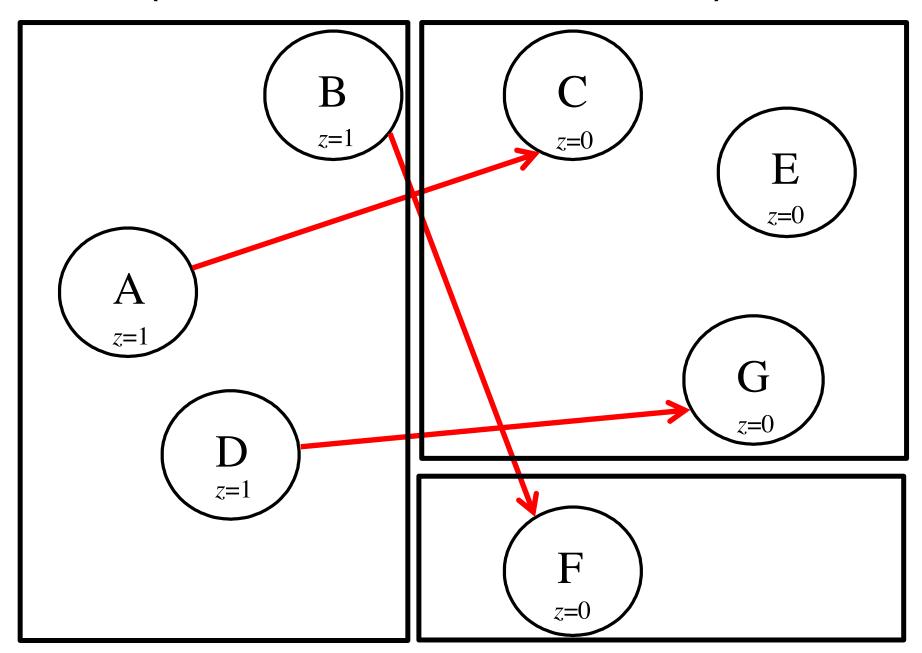
## Partition #3 (ABD)(CEG)(F)



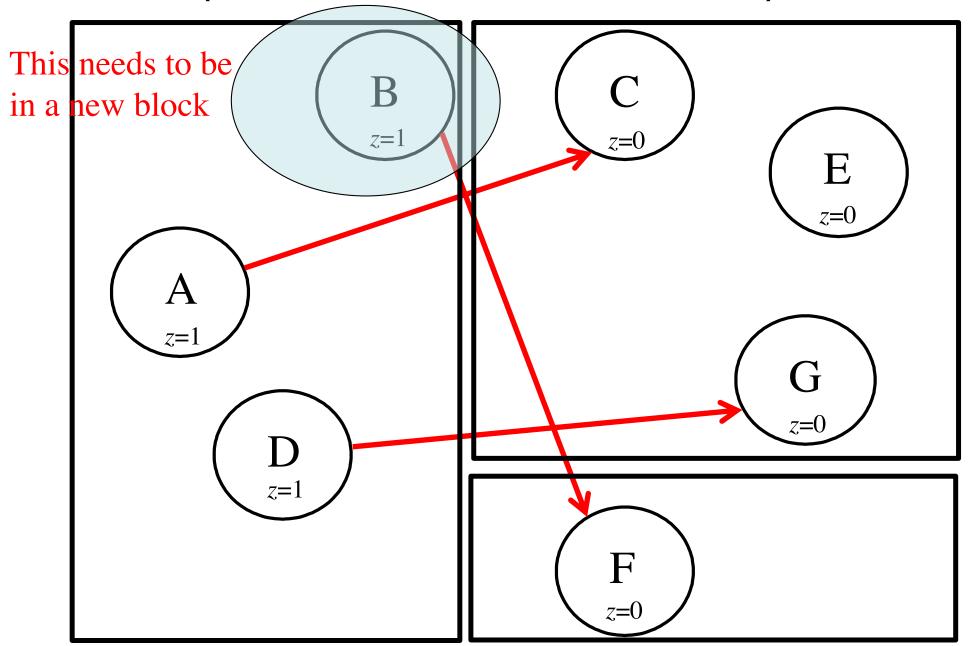
(Examine the 0-successors of ABD)



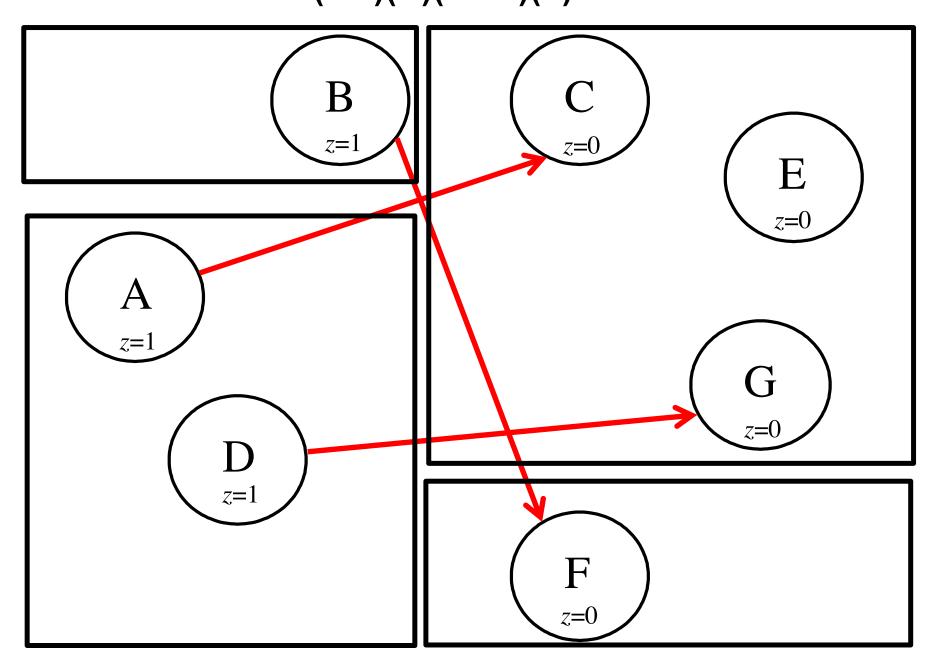
(Examine the 1-successors of ABD)



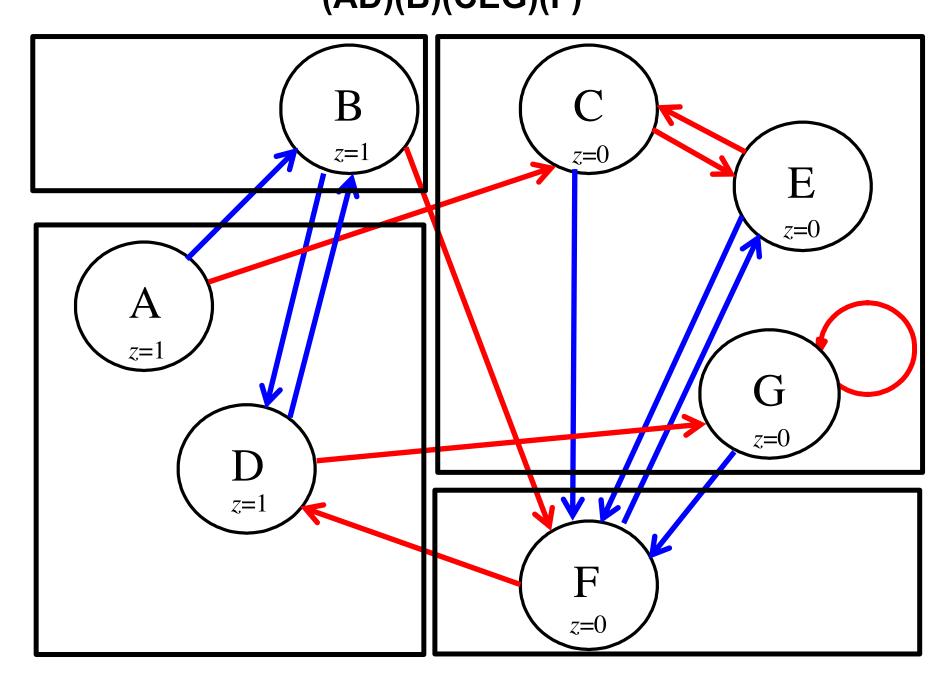
(Examine the 1-successors of ABD)



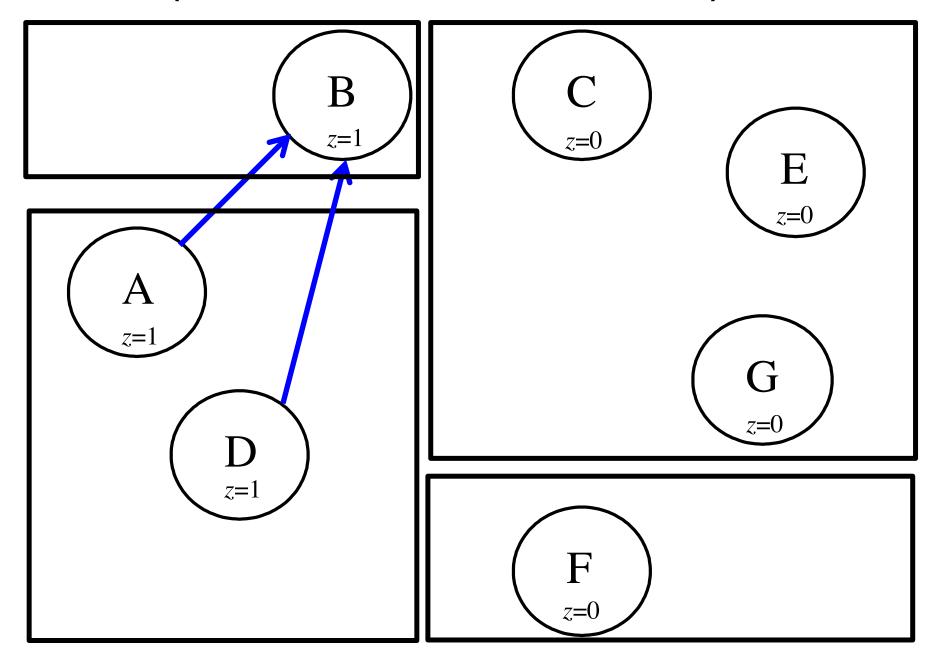
## Partition #4 (AD)(B)(CEG)(F)



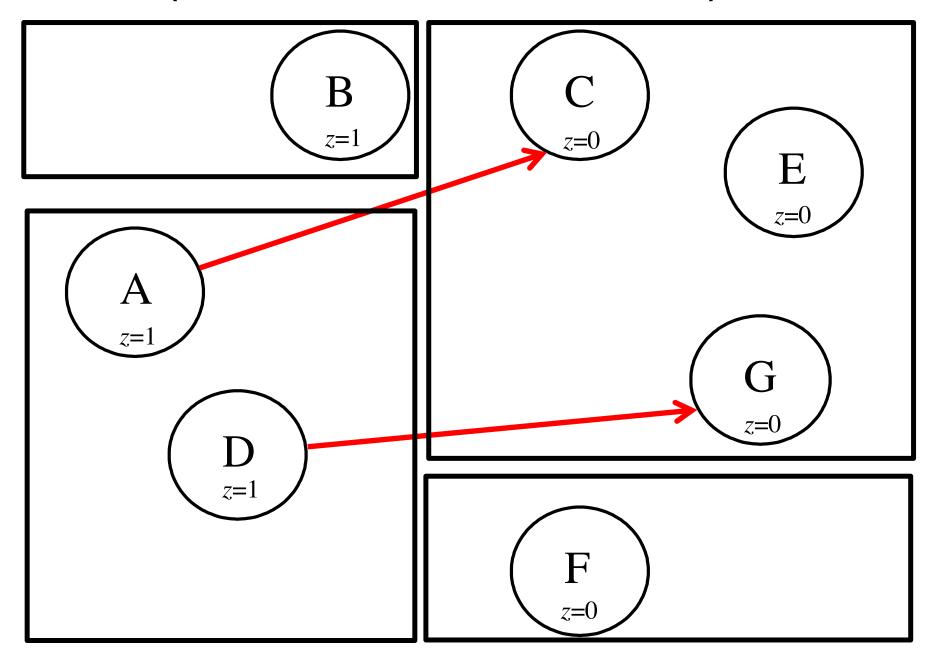
## Partition #4 (AD)(B)(CEG)(F)



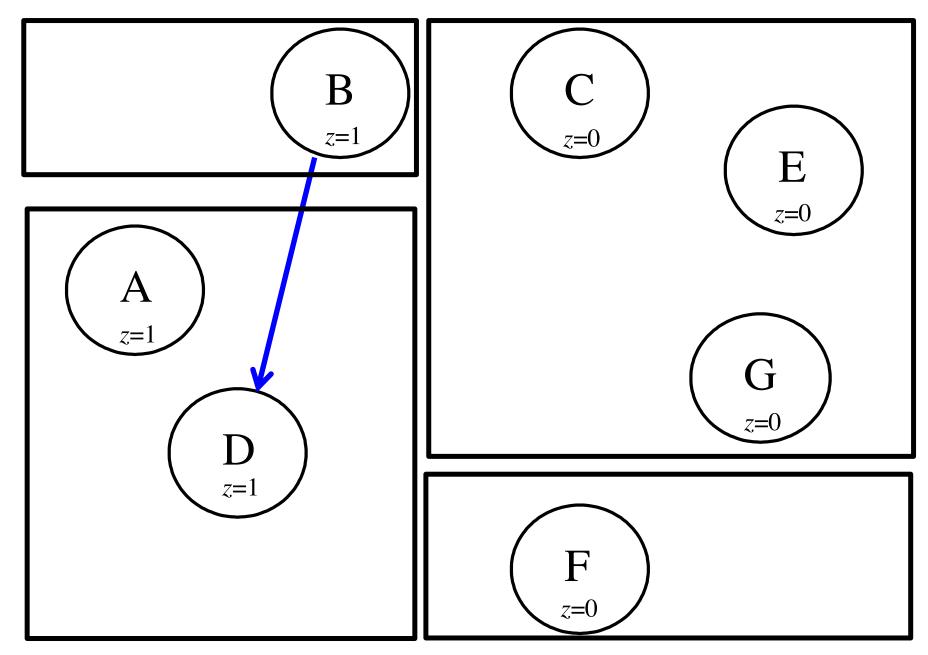
(Examine the 0-successors of AD)



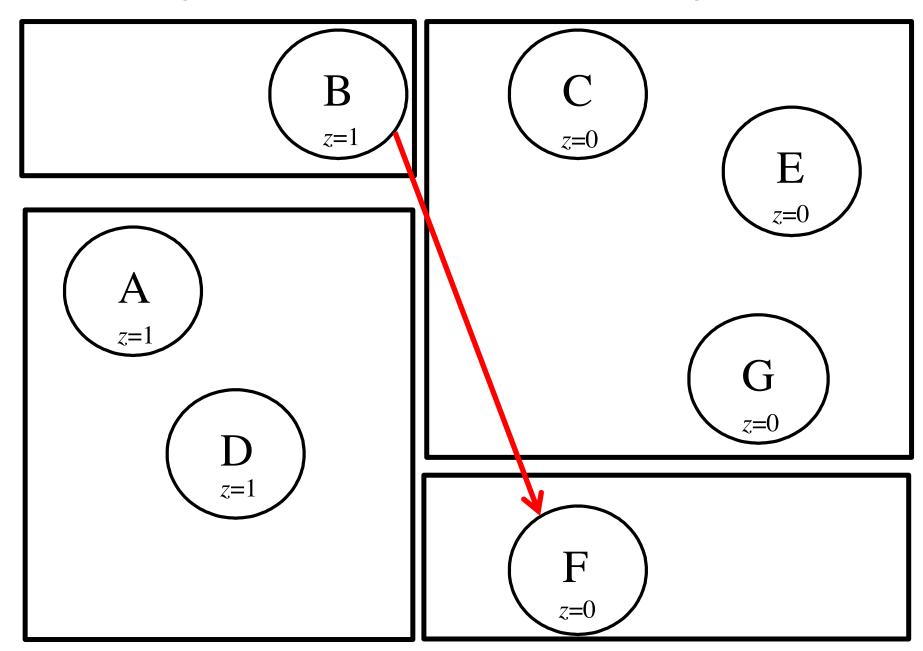
(Examine the 1-successors of AD)



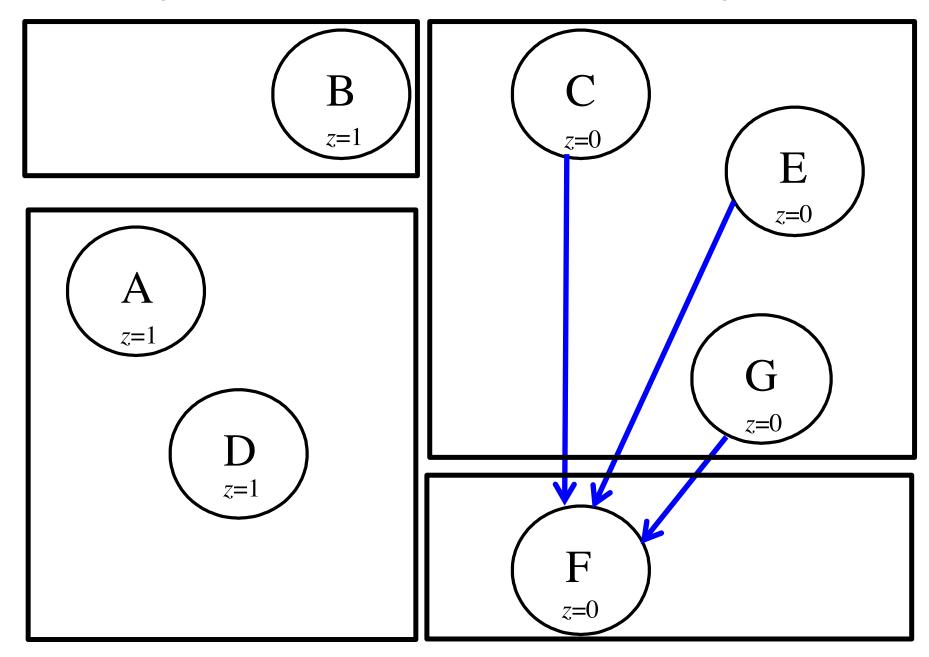
(Examine the 0-successors of B)



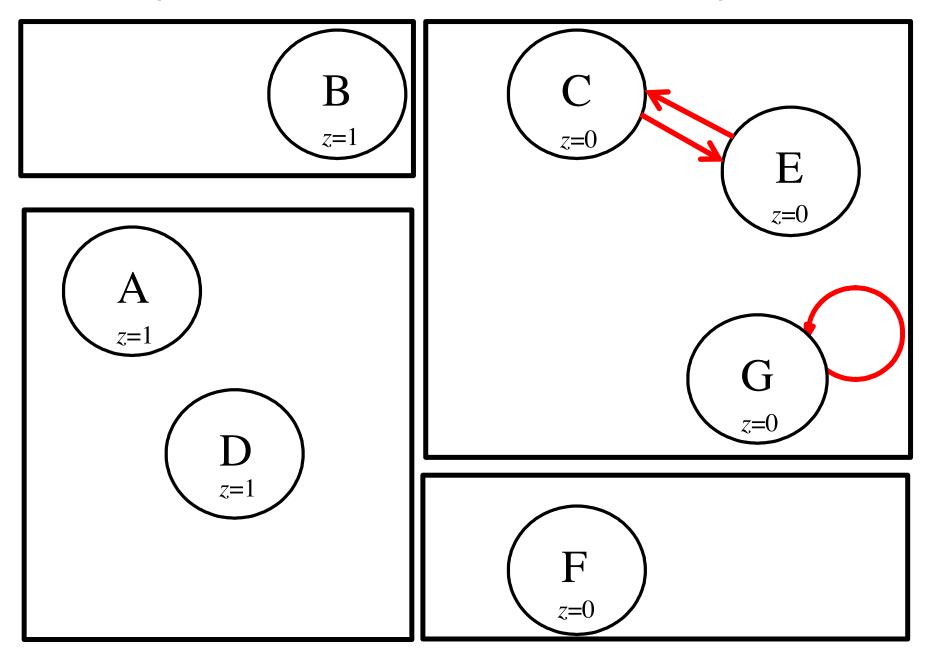
(Examine the 1-successors of B)



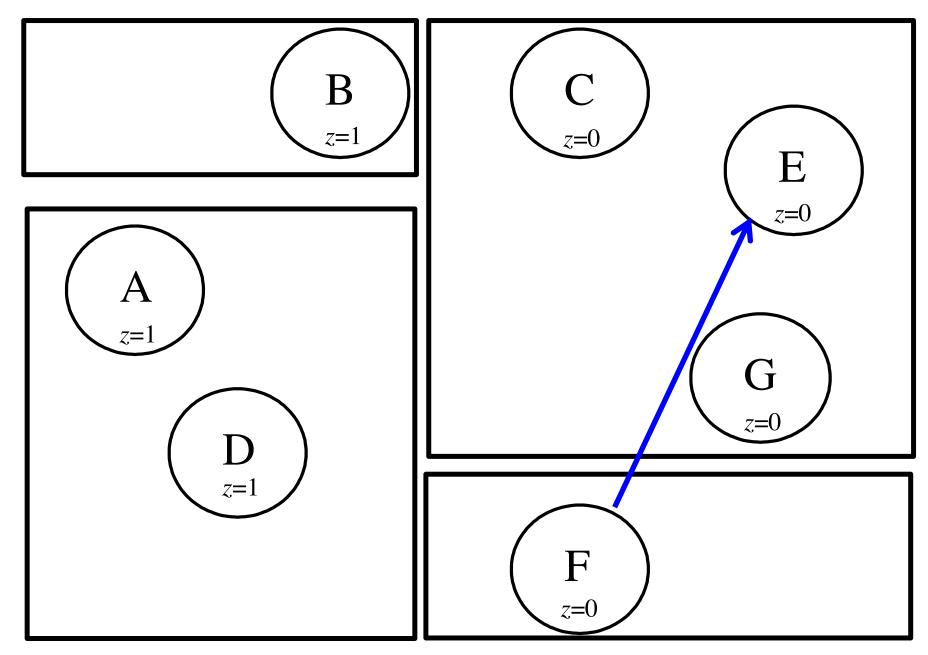
(Examine the 0-successors of CEG)



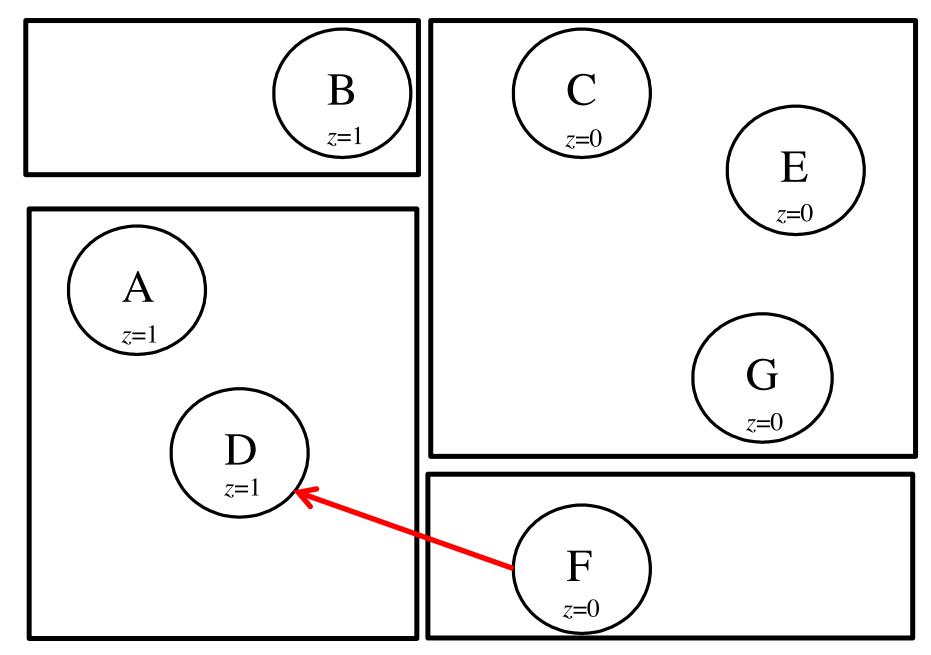
(Examine the 1-successors of CEG)



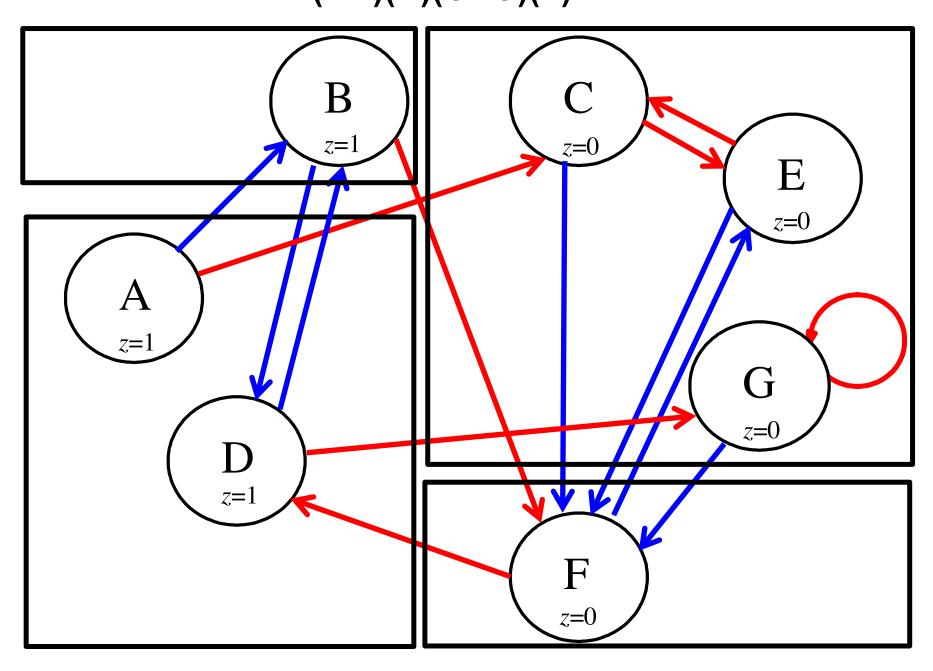
(Examine the 0-successors of F)



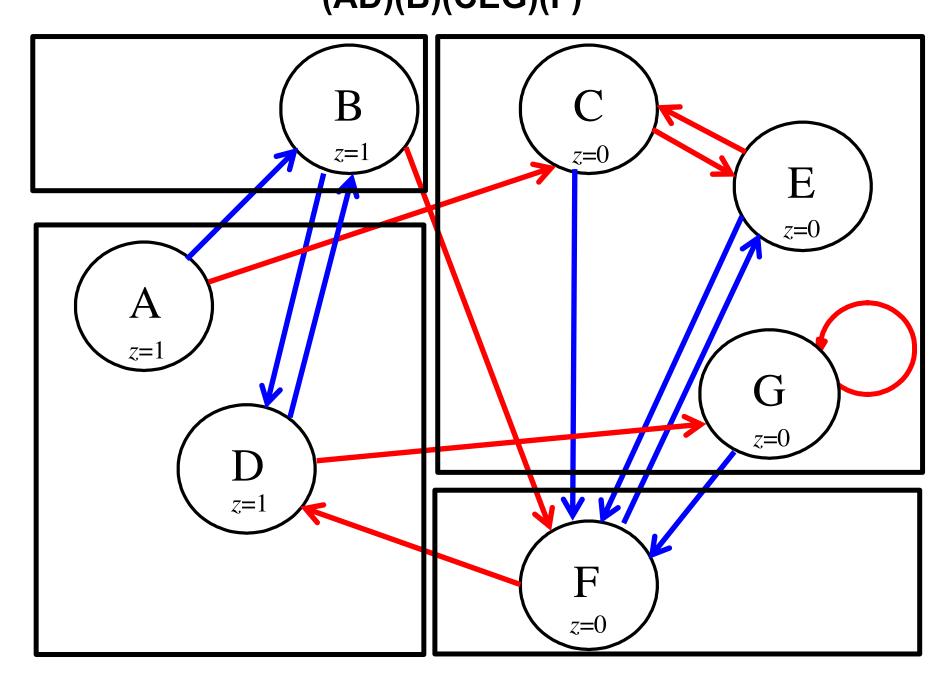
(Examine the 1-successors of F)



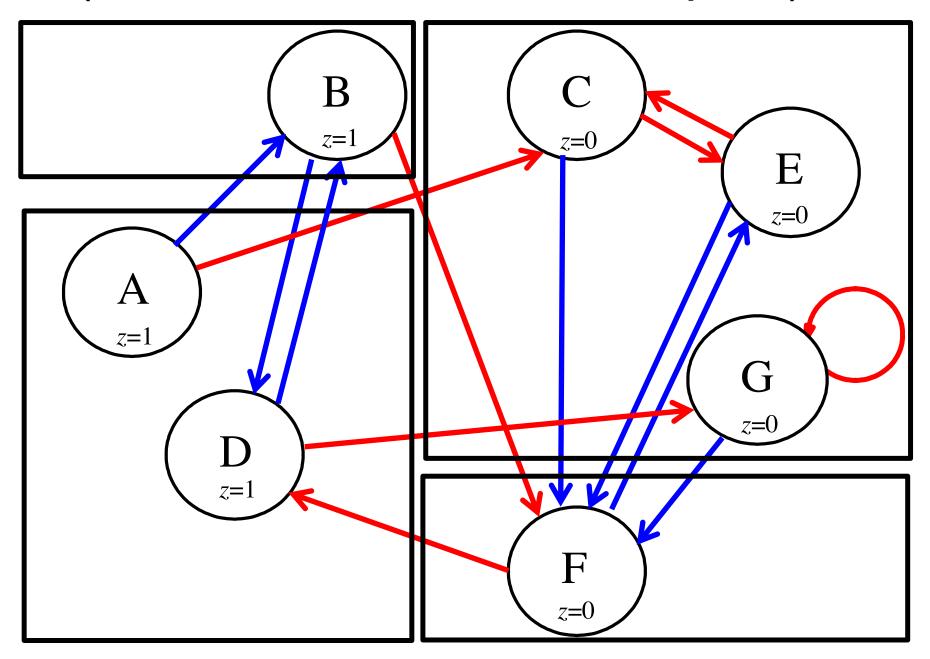
## Partition #5 (AD)(B)(CEG)(F)



## Partition #4 (AD)(B)(CEG)(F)



(This is the same as #4 so we can stop here)



#### Minimized state table

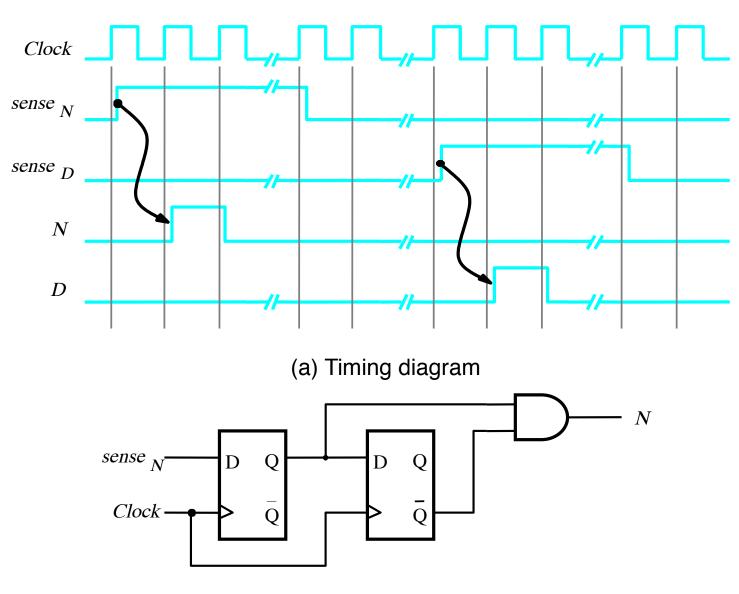
Present	Next	Output	
state	w = 0	w = 1	Z
A	В	С	1
В	A	F	1
C	F	C	0
F	C	A	0

## **Vending Machine Example**

### **Vending Machine Example**

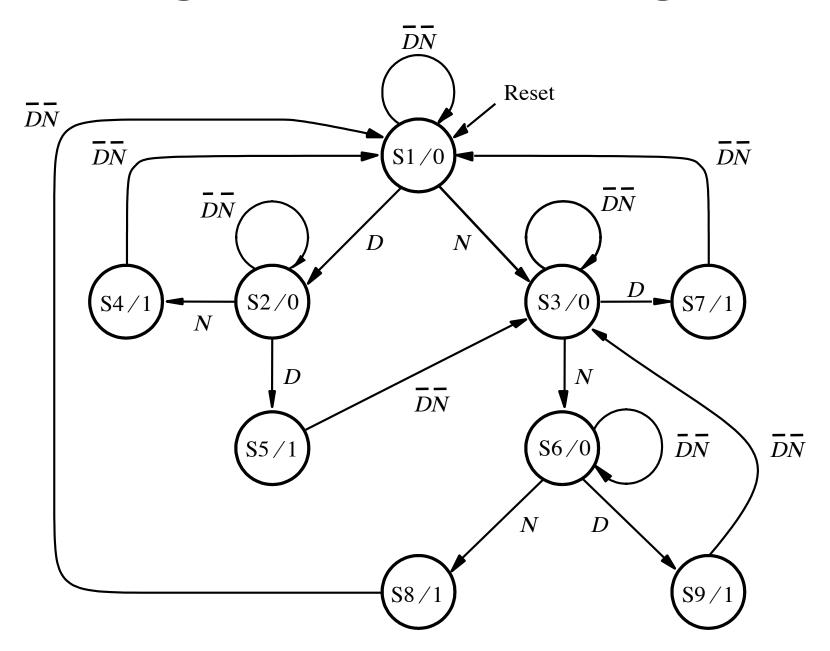
- The machine accepts nickels and dimes
- It takes 15 cents for a piece of candy to be released from the machine
- If 20 cents is deposited, the machine will not return the change, but it will credit the buyer with 5 cents and wait for the buyer to make a second purchase.

### Signals for the vending machine

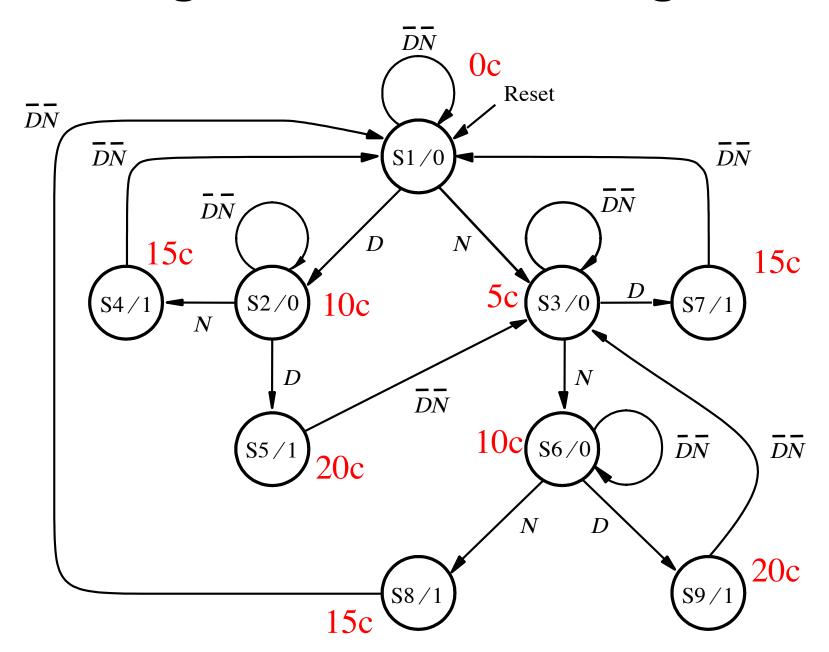


(b) Circuit that generates N

## State Diagram for the vending machine



## State Diagram for the vending machine



## State Table for the vending machine

Present	esent Next state					
state	DN =00	01	10	11	Z	
<b>S</b> 1	<b>S</b> 1	<b>S</b> 3	<b>S</b> 2	1	О	
S2	S2	<b>S</b> 4	<b>S</b> 5	_	0	
S3	<b>S</b> 3	<b>S</b> 6	<b>S</b> 7	_	0	
S4	<b>S</b> 1	_	_	_	1	
S5	<b>S</b> 3	_	_	_	1	
<b>S</b> 6	<b>S</b> 6	<b>S</b> 8	<b>S</b> 9	_	0	
S7	<b>S</b> 1	_	_	_	1	
<b>S</b> 8	<b>S</b> 1	_	_	_	1	
S9	S3	_	_	_	1	

Incompletely specified state table

Present		Next state			
state	00	01	10	11	z
S1	S1	S3	S2	_	0
S3	S3	<b>S</b> 6	<b>S</b> 7	_	0
S2	S2	<b>S</b> 4	S5	-	0
S6	S6	S8	S9	-	0
S4	S1	-	-	-	1
S7	S1	_	-	-	1
S8	S1	-	-	-	1
S5	S3	-	_	_	1
S9	S3	-	-	_	1

P1=(S1,S2,S3,S4,S5,S6,S7,S8,S9)

Present		Next	state		Output
state	00	01	10	11	z
S1	S1	S3	S2	-	0
S3	S3	<b>S</b> 6	<b>S7</b>	-	0
S2	S2	<b>S4</b>	<b>S</b> 5	-	0
S6	S6	S8	S9	-	0
<b>S4</b>	S1	_	-	-	1
<b>S7</b>	S1	_	-	-	1
S8	S1	_	-	-	1
S5	S3	-	-	-	1
S9	S3	-	-	-	1

P1=(S1,S2,S3,S4,S5,S6,S7,S8,S9) P2=(S1,S2,S3,S6) (S4,S5,S7,S8,S9)

Present		Next state				
state	00	01	10	11	z	
S1	S1	S3	S2	-	0	
S3	S3	<b>S</b> 6	<b>S7</b>	-	0	
S2	S2	<b>S4</b>	<b>S</b> 5	-	0	
<b>S6</b>	<b>S</b> 6	S8	S9	-	0	
S4	S1	_	-	-	1	
<b>S7</b>	S1	_	-	-	1	
S8	S1	_	-	-	1	
S5	S3	_	-	-	1	
S9	S3	-	-	-	1	

```
P1=(S1,S2,S3,S4,S5,S6,S7,S8,S9)
P2=(S1,S2,S3,S6) (S4,S5,S7,S8,S9)
P3=(S1) (S3) (S2,S6) (S4,S5,S7,S8,S9)
```

Present		Next state			
state	00	01	10	11	z
S1	S1	S3	S2	_	0
<b>S</b> 3	<b>S</b> 3	<b>S</b> 6	<b>S</b> 7	-	0
S2	S2	<b>S</b> 4	<b>S5</b>	-	0
S6	<b>S</b> 6	S8	<b>S</b> 9	-	0
S4	S1	-	-	-	1 1
<b>S7</b>	S1	-	-	-	1
<b>S8</b>	S1	-	-	-	1 1
<b>S5</b>	S3	-	-	-	1
<b>S</b> 9	<b>S</b> 3	-	_	-	1

```
P1=(S1,S2,S3,S4,S5,S6,S7,S8,S9)
P2=(S1,S2,S3,S6) (S4,S5,S7,S8,S9)
P3=(S1) (S3) (S2,S6) (S4,S5,S7,S8,S9)
P4=(S1) (S3) (S2,S6) (S4,S7,S8) (S5,S9)
```

Present		Next state				
state	00	01	10	11	z	
S1	S1	S3	S2	-	0	
S3	S3	<b>S6</b>	<b>S7</b>	-	0	
S2	S2	<b>S4</b>	<b>S5</b>	-	0	
<b>S</b> 6	<b>S</b> 6	S8	<b>S</b> 9	-	0	
<b>S4</b>	S1	-	-	-	1	
<b>S7</b>	S1	_	-	-	1	
S8	S1	-	-	-	1	
<b>S5</b>	S3	_	-	-	1	
<b>S</b> 9	S3	-	-	-	1	

```
P1=(S1,S2,S3,S4,S5,S6,S7,S8,S9)

P2=(S1,S2,S3,S6) (S4,S5,S7,S8,S9)

P3=(S1) (S3) (S2,S6) (S4,S5,S7,S8,S9)

P4=(S1) (S3) (S2,S6) (S4,S7,S8) (S5,S9)

P5=(S1) (S3) (S2,S6) (S4,S7,S8) (S5,S9)
```

Present		Output			
state	00	01	10	11	Z
S1	S1	<b>S</b> 3	S2	-	0
S3	<b>S</b> 3	<b>S</b> 6	<b>S</b> 7	-	0
S2	S2	S4	<b>S</b> 5	-	0
<b>S</b> 6	<b>S</b> 6	S8	<b>S</b> 9	-	0
S4	S1	-	_	-	1
<b>S7</b>	S1	-	-	-	1
S8	S1	-	-	-	1
<b>S5</b>	<b>S</b> 3	-	-	-	1
<b>S</b> 9	S3	-	-	-	1

```
P1=(S1,S2,S3,S4,S5,S6,S7,S8,S9)

P2=(S1,S2,S3,S6) (S4,S5,S7,S8,S9)

P3=(S1) (S3) (S2,S6) (S4,S5,S7,S8,S9)

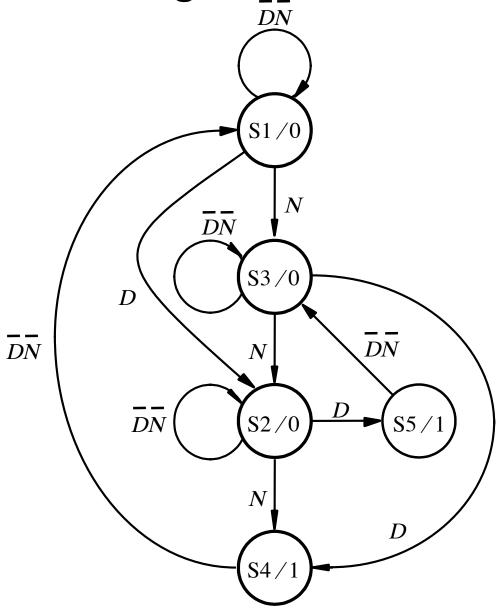
P4=(S1) (S3) (S2,S6) (S4,S7,S8) (S5,S9)

P5=(S1) (S3) (S2,S6) (S4,S7,S8) (S5,S9)
```

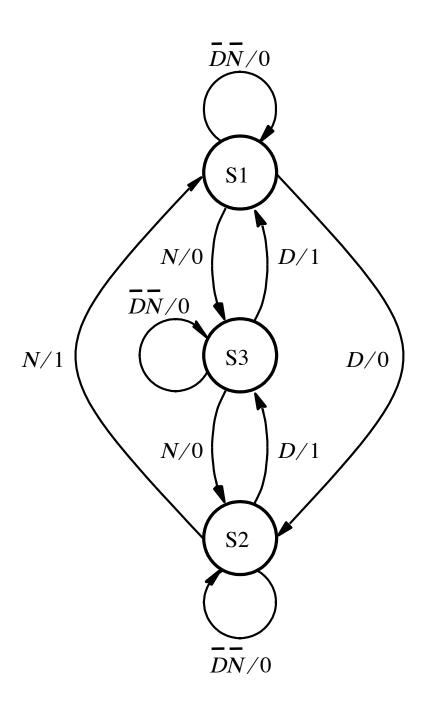
#### Minimized State Table for the vending machine

Present	Nε	Output			
state	DN =00	01	10	11	Z
S1	<b>S</b> 1	<b>S</b> 3	<b>S</b> 2	_	0
S2	<b>S</b> 2	<b>S</b> 4	<b>S5</b>	_	0
<b>S</b> 3	<b>S</b> 3	<b>S</b> 2	<b>S</b> 4	_	0
<b>S</b> 4	<b>S</b> 1	_	_	_	1
S5	<b>S</b> 3	_	_	_	1

#### Minimized State Diagram for the vending machine



#### Mealy-type FSM for the vending machine



# Another Example of Incompletely specified state table

Present	Next state		Outp	out z
state	w = 0	w = 1	w = 0	w = 1
A	В	C	0	0
В	D	_	0	_
C	F	E	0	1
D	В	G	0	0
E	F	C	0	1
F	Е	D	0	1
G	F	_	0	_

## **Questions?**

### THE END