Cpr E 281 HW05
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Karnaugh Maps
Assigned: Week 5
Due Date: Oct. 1, 2018

P1 (12 points): You want to develop a circuit that implements the truth table shown below.

Q_3	Q_2	Q_1	Q_0	Z
0	0	0	0	D
0	0	0	1	1
0	0	1	0	D
0	0	1	1	0
0	1	0	0	D
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1

Q_3	Q_2	Q_1	Q_0	Z
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	D
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	D

A: Implement circuit Z as Z_1 using any number of NOT gates, but no more than three AND gates and only one OR gate may be used.
B: Implement circuit Z as Z_2 using only NOT gates and NAND gates.
C: Let the logic gate transistor cost (GTC) be as follows: NOT gates have GTC of 2, while NAND/NOR gates have GTC of 2x (x being the number of gate inputs to the NAND/NOR gate). Show that the total GTC of the circuit for Z_2 is 24.
D: Show that the GTC for an AND/OR gate is 2(x+1).
E: Show that the total GTC of the circuit for Z_1 is 32.

P2 (9 points): Convert the following expressions into simplified SOP expressions.
I: $f_1(A,B,C,D) = \sum m(0,1,4,7,13,15) + \mathcal{D}(3,5,12)$
II: $f_2(W,X,Y,Z) = \sum m(0,2,8,14) + \mathcal{D}(1,3,4,6,9,10,12)$
III: $f_3(x_3,x_2,x_1,x_0) = m_3 + m_9 + m_{10} + m_{15} + \mathcal{D}(4,7,8,11,13,14)$

P3 (9 points): Convert the following expressions into simplified POS expressions.
I: $g_1(A,B,C,D) = M_7 M_{13} + \mathcal{D}(0,1,2,3,4,6,8,9,10,11,12,14)$
II: $g_2(W,X,Y,Z) = \prod M(3,4,13) + \mathcal{D}(2,5,6,8,10,14)$
III: $g_3(x_3,x_2,x_1,x_0) = \prod M(1,4,5,6,9,11,15) + \mathcal{D}(0,2,3)$

P4 (15 points): We want to design a circuit that accepts a four-bit number X and produces an output that meets the following specifications:
* the circuit outputs n=0 if X is 0, 1, 2, or 6.
* the circuit outputs n=1 for other values of X
* we can assume that X is a number in the range of 0 to 9. For example, we do not have to process numbers such as 10 (1010_2) or 15 (1111_2) that are larger than nine.

A: Draw the truth table for this function n.
B: You are unsure whether the SOP expression or the POS expression will be more efficient. Derive the simplest SOP expression n_{SOP} and the POS expression n_{POS}.
C: Show that n_{SOP} and n_{POS} have the same cost. Note that the cost is the number of gates plus the number of gate inputs.
D: Is it true that $n_{SOP} = n_{POS}$?

P5 (15 points): A given circuit receives a four-bit number B (b_3, b_2, b_1, b_0) and produce two outputs: output T will be 1 if B is a multiple of 2 or a multiple of 3, whereas output C will be 1 if B is a composite number (4, 6, 8, 9, etc.) Recall that a composite number is a positive integer that has at least one multiple other than 1 and itself, and that 0 is not a positive integer!
I: Draw the truth table for C and T.
II: Show that C and T can be implemented using 5 OR gates and 2 AND gates. Assume that the complemented inputs are available; that is, you do not need NOT gates to produce $\bar{b}_3, \bar{b}_2, \bar{b}_1, \bar{b}_0$ since these are also usable as external inputs to your circuit.

P6 (20 points): Show that the functions $g_1(w,x,y,z) = \prod M(1,2,3,4,5,6,9,13)$ and $g_2(w,x,y,z) = \sum m(2,3,4,6,7,10,11)$ can be implemented using only 11 gates. You can only use NOT gates, AND gates, and OR gates in your solution. Note that NOT gates should also be counted in the number of gates used here to implement g_1 and g_2.

P7 (12 points): Given a ripple carry adder with 6-bit unsigned input A, 6-bit unsigned input B, and a carry in bit C_{in}, state the value of the sum output and the value of the carry out bit C_{out}. For each problem, also indicate if the addition causes the result to overflow (first, identify how you can determine if an unsigned addition led to an overflow).
I: A = 000111_2, B = 010101_2, C_{in} = 0.
II: A = 111111_2, B = 101101_2, C_{in} = 0.
III: A = 001010_2, B = 101010_2, C_{in} = 1.

P8 (8 points): Convert the number -18 into 6-bit binary with the following representations:
A: Sign and Magnitude representation.
B: 1's Complement representation.
C: 2's Complement representation.