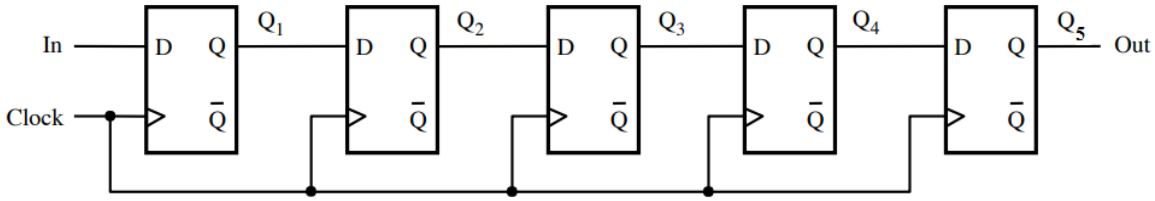
Cpr E 281 HW09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

# Registers and Counters
## Assigned: Week 10
## Due Date: Nov. 5, 2018

**P1 (10 points):** Complete the following table for the shift register shown. Assume that each horizontal line is a single pulse of the clock.




| Time | In | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ |
|---|---|---|---|---|---|---|
| t=0 | 1 | 0 | 1 | 1 | 0 | 1 |
| t=1 | 1 | | | | | |
| t=2 | 0 | | | | | |
| t=3 | 0 | | | | | |
| t=4 | 1 | | | | | |
| t=5 | 0 | | | | | |
| t=6 | 0 | 0 | 1 | 0 | 0 | 1 |

**P2 (16 points):** Design a four-bit register with both shift and parallel load features. The inputs of the register include a 2-bit input bus J as $J_1J_0$, a 4-bit input bus X as $X_3X_2X_1X_0$, and a clock signal. The register will have a 4-bit output bus Q that represents the value stored in the register. You are allowed to use any number and size of the following: DFFs, MUXes, decoders, encoders, AND gates, OR gates, and NOT gates (Notice that you do not need all of them). The operation of the registers are defined below:

If J=0, then the output Q remains unchanged. $Q_3^{new} = Q_3^{old}, Q_2^{new} = Q_2^{old}, Q_1^{new} = Q_1^{old}, Q_0^{new} = Q_0^{old}$
If J=1, then the output Q is shifted to the left $Q_3^{new} = Q_2^{old}, Q_2^{new} = Q_1^{old}, Q_1^{new} = Q_0^{old}, Q_0^{new} = X_0$
If J=2, then the output Q is shifted to the right. $Q_3^{new} = X_0, Q_2^{new} = Q_3^{old}, Q_1^{new} = Q_2^{old}, Q_0^{new} = Q_1^{old}$
If J=3, then the output Q will take on the values in X. $Q_3^{new} = X_3, Q_2^{new} = X_2, Q_1^{new} = X_1, Q_0^{new} = X_0$

**P3 (14 points):** In the circuit below, Y=0 and C=0. In addition, for all of the memory components shown below, Z=Q=0. At the beginning of our simulation, the value of Y is then set to 1.

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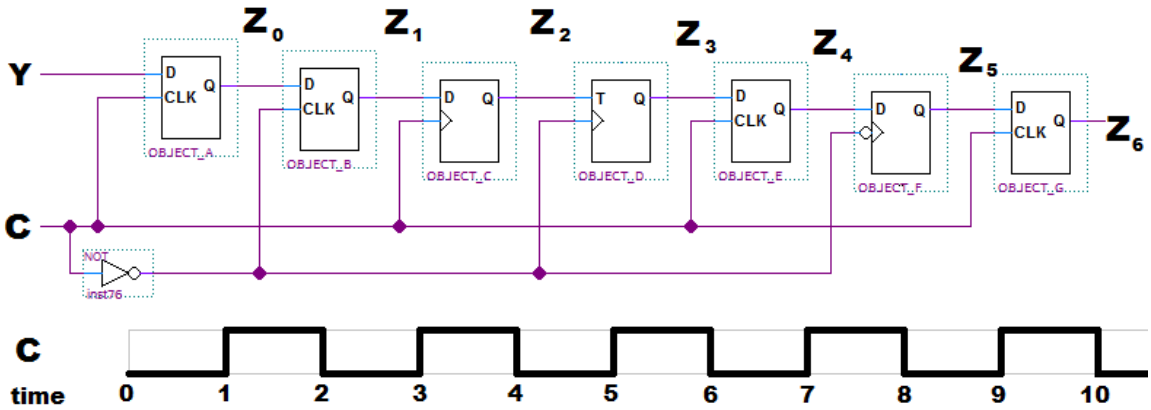
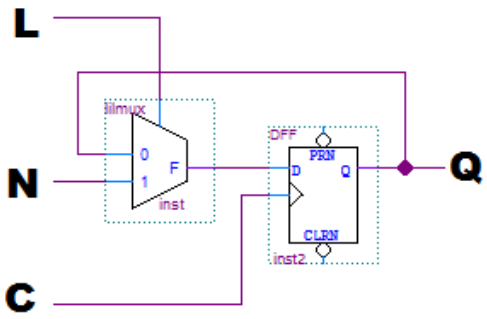
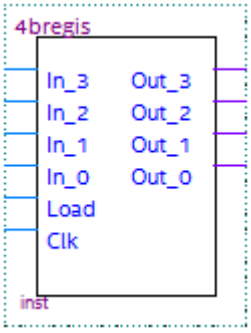



Fill out the table below by identifying the components in the above picture and stating at what time each component's output becomes 1. The time can be determined by looking at the timing diagram for C and checking the number values underneath for the time. The output of OBJECT_C has already been filled in for you. Identify the components as their symbol appears inside of their object rectangle and not based on the value of C.

| Object Name | Object Type | Time until Q=1 |
|---|---|---|
| OBJECT_A | | |
| OBJECT_B | | |
| OBJECT_C | **Positive-Edge-Triggered DFF** | **3** |
| OBJECT_D | | |
| OBJECT_E | | |
| OBJECT_F | | |
| OBJECT_G | | |

**P4 (8 points):** Shown below: on the left is a one-bit parallel-access register (register). Show how one-bit registers can be used to construct the register shown on the right. This register will have a 4-bit input IN ($IN_3$, $IN_2$, $IN_1$, $IN_0$) that contains the data to be stored in the register, a 4-bit output OUT ($OUT_3$, $OUT_2$, $OUT_1$, $OUT_0$) which continuously outputs the value in the register, a clock signal CLK, and a 1-bit input LOAD that determines if the register will update its held data. Use a symbol for the one-bit parallel access register to simplify the drawing.

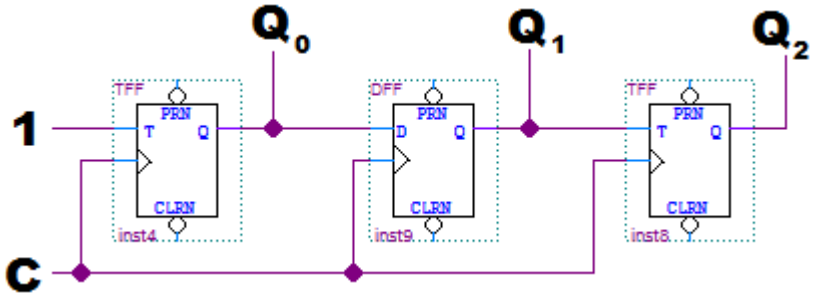



**P5 (12 points):** A given register file can support storing values in its 32 registers. Each register is designed to hold numbers ranging from -25 to +25 (in 2's complement) with no additional bits beyond those necessary to hold numbers in this range. Answer the following questions:
A: What is the **width** of the LD_DATA bus? (Note that **width** is the number of bits)
B: What is the width of each register?
C: What is the width of the RA bus?
D: What is the width of the WA bus?
E: How many DFFs exist in this register file?
F: What type of decoder is used in this register file?

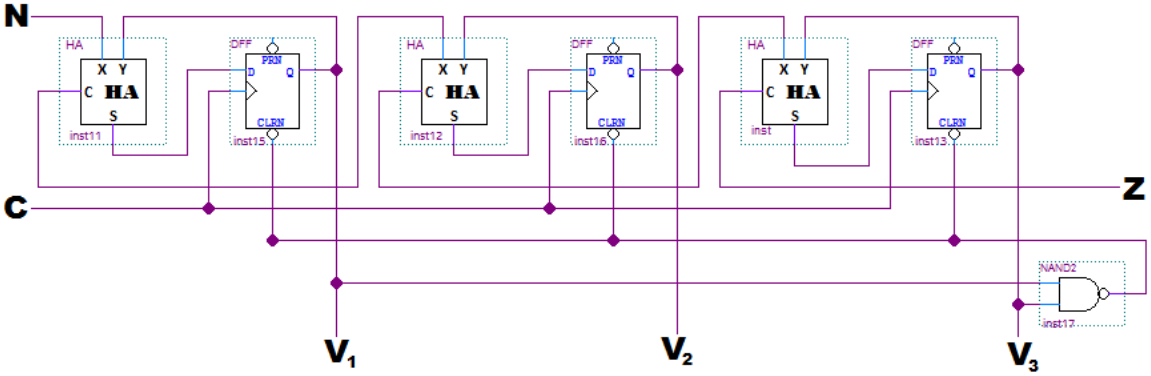
**P6 (8 points):** Upon examination of a register file, you notice only that the output is controlled by a 12-bit 16-1 MUX, but were unable to observe the rest of the circuitry of the register file.
A: What type of decoder is used in this file?
B: How many 1-bit 2-1 MUXes are needed to replicate the operation of the 12-bit 16-1 MUX?

**P7 (10 points):** The circuit below looks like a counter. The clock signal C is connected to a 24Hz clock signal.




A: What is the counting sequence of this circuit? Assume that the output Q is initially 000.
B: What is the steady-state frequency of the output signal from $Q_2$?

**P8 (10 points):** The circuit below was designed with three DFFs, three Half-Adders, and one two-input NAND gate. The clock signal to this circuit has a period of 256 µs (Hint: $f = \frac{1}{T}$).




A: What is the **modulus** of this counter; that is, how many distinct values will be output by this counter before it resets? Do not include values that are not present for the entire clock cycle.
B: What will be the period of the output signal Z?
C: What will be the period of the output signal $V_1$?

**P9 (12 points):** Using only a number of modulo-20 counters as shown below, design a circuit that will take a 4.8kHz signal F and produce a 6Hz signal G. When N=1, the counter will count up. When N=0, the counter will hold its current value.