

P1 (15 points): Design a modulo-7 down counter using TFFs. Include a RESET signal that will reset the counter to 6. Use a state assignment that causes the output to be equivalent to the state value.

A: Use K-maps to show that the expressions for the TFF inputs are as follows: $T_2 = w\bar{Y}_1\bar{Y}_0$, $T_1 = w\bar{Y}_0$, $T_0 = w(Y_2 + Y_1 + Y_0)$.

B: Draw the circuit diagram for the modulo-7 down counter using three TFFs, three 2-1 MUXes, one AND gate and one OR gate. Use W as the select line input.

P2 (15 points): You are given a 3-bit shift register with clock input C and an input N which contains the bit to be shifted into the register on the next negative clock cycle. The shift register also has an input J that functions as follows: if J=0, then the shift register holds its value constant for this clock cycle, but if J=1, the shift register will shift to the right.

A: Draw the circuit diagram for this shift register. Preset and Clear connections should remain unused.

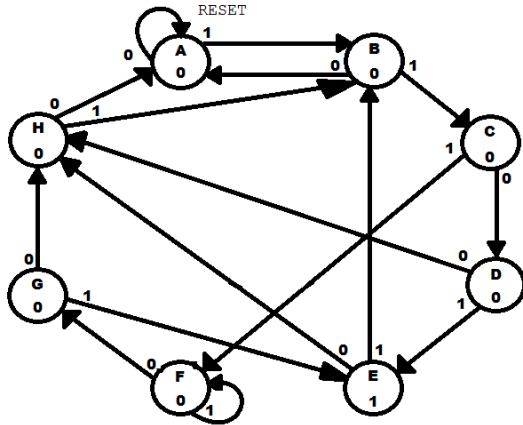
B: Let us make a Mealy FSM that can fill this shift register with the value 101 as follows. The FSM will have an input W such that, when W=1, the FSM will first fill the shift register with 101 and then maintain 101 as the output until W=0; when W=0, the shift register will fill with 0s. Note that the shift register does not have to fill with 0s in one step; the only requirement here is that, while W=0, the shift register will eventually fill with zeros. Draw the state diagram for this FSM.

P3 (10 points): Let us make a Moore FSM that determines if a number is divisible by three.

A: Draw the state diagram for a Moore FSM that receives an input W and produces an output Z=1 only if the accumulated value V is a multiple of 3. When W is input, the new value is as follows: $V_{new} = 2V + W$. The FSM should have only three states, where each state corresponds to the value of $V \bmod 3$.

B: Use your state diagram to determine if the 36-bit number 101100101111001011101101011011001010 is a multiple of 3.

P4 (10 points): Reduce the state diagram below to use only five states.



P5 (15 points): Consider the multiplication of $Y = 3X$. We want to create a FSM that will produce the bits of Y given X from least-significant bit to most-significant bit.

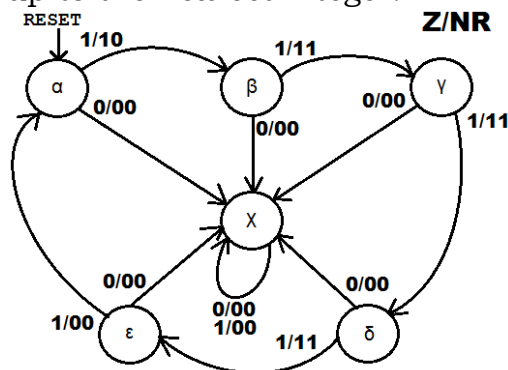
A: First, design a circuit that will multiply a four-bit X by 3 to produce Y . You can use only Full Adders to implement this circuit. Note that this circuit should not be implemented as an FSM yet.

B: Modify the Mealy FSM serial adder circuit (figure 6.43 from the book) to design a circuit that sequentially calculates $Y = 3X$. The value of X is now stored in a shift register and each bit will be input serially into the circuit via an input x . Your circuit should contain only one Full Adder and only two DFFs. The output y is now only one-bit that will produce the full value of Y one-bit at a time.

P6 (20 points): You have a modulo-256 down counter (**operand counter**) with 8-bit output and one-bit input N (the **operand counter** counts down for each clock cycle where N=1). Assume that this **operand counter** is initially holding an unknown value V. You also have a second modulo-256 up counter (**result counter**) to store an 8-bit mathematical result W (the **result counter** counts up for each clock cycle where R=1). Design the following:

I: Design a circuit that outputs Z=1 if the **operand counter** is nonzero.

II: The following FSM state diagram receives input Z and outputs N/R (which decrements the down counter) and R (which increments the up counter). When the down counter reaches zero, algebraically describe the value of the up counter W in terms of the initial value of the down counter V. Also, denote if the answer will be rounded down or rounded up to the nearest integer.

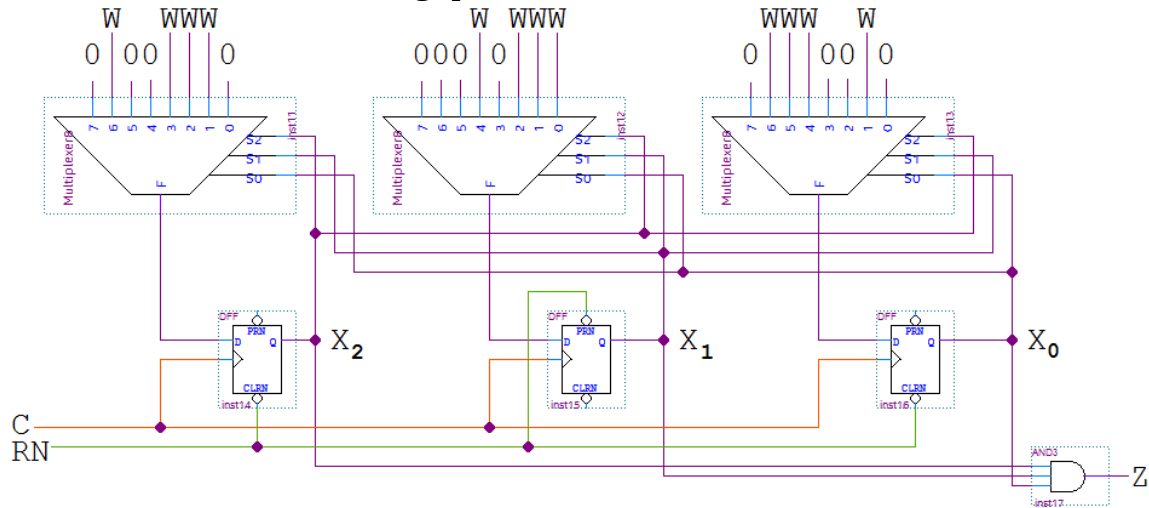


III: Design a FSM state diagram that fills the **result counter** with the value $W = \left\lfloor \frac{V}{5} \right\rfloor$ (the result of division rounded down to the nearest integer) using the one-bit input Z, output R (R is the input which enables the up counter), and output N (N is the input which enables the down counter). You only need to draw the state diagram; the destination for each FSM connection should be specified as above. When the result counter contains the correct value, the result counter should remain unchanged for any future clock cycles.

IV: Repeat part II, but produce the result $W = \left\lceil \frac{3V}{5} \right\rceil$ (here, the quotient is rounded up to the nearest integer).

V: Repeat part II, but produce the result $W = \left\lceil \frac{5V}{3} \right\rceil$ (round up).

P7 (15 points): The following circuit uses 3 8-to-1 MUXes to implement a FSM. Answer the following questions about this circuit:



A: Based on the number of DFFs in this circuit, what is the maximum number of states that this circuit may have?

B: Draw a state table for the circuit.

C: Which two values of X (the state value in $X_2X_1X_0$) are unreachable after the circuit is reset?

D: Draw a state diagram for this FSM. Note: state diagrams should not contain states that cannot be reached from the reset state. Don't forget to include the reset state, since there is a reset in the circuit.

E: Is this a Moore FSM or a Mealy FSM?

F: Let $W=1$ and $RN=1$. If the clock C is connected to a 7.2kHz signal, what will be the frequency of the output Z?