Name and Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**PRELAB:**

**Q1.** Read section 3.0 and fill in the truth table below for *lab2step1*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Circuit Diagram:

TA Initials: \_\_\_\_\_\_\_\_\_

**Q2.** Read section 4.0 and fill in the truth table below for *lab2step2*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Circuit Diagram:

TA Initials: \_\_\_\_\_\_\_\_\_

**LAB:**

**3.0** Hardware results demonstrate a correct circuit. TA Initials: \_\_\_\_\_\_\_\_\_

**4.0** Hardware results demonstrate a correct circuit. TA Initials: \_\_\_\_\_\_\_\_\_