

Name and Std No.: _____ Lab Section: _____

Date: _____

PRELAB:

Refer to Chapter 5 in your textbook and the lab instructions to complete your pre-lab. Please read all the material and complete the circuit diagrams before you come to the lab.

Q1. Draw the circuit diagram for the SR Latch using NOR Gates for **Section 2.0** in the space below.

Q2. Draw the circuit diagram for the \overline{SR} Latch using NAND Gates for **Section 2.0** in the space below.

Q3. Draw the circuit diagram for the D Latch using NAND Gates and a NOT gate for **Section 3.0** in the space below.

Q4. Draw the circuit diagram for the Master-Slave D Flip-Flop for **Section 4.0** using the D latches you built in the previous step in the space below. The flip-flop should be triggered by the negative edge of the clock.

Q5. Draw the circuit diagram for the Positive-Edge-Triggered D Flip-Flop using NAND gates for **Section 4.0** in the space below.

LAB:

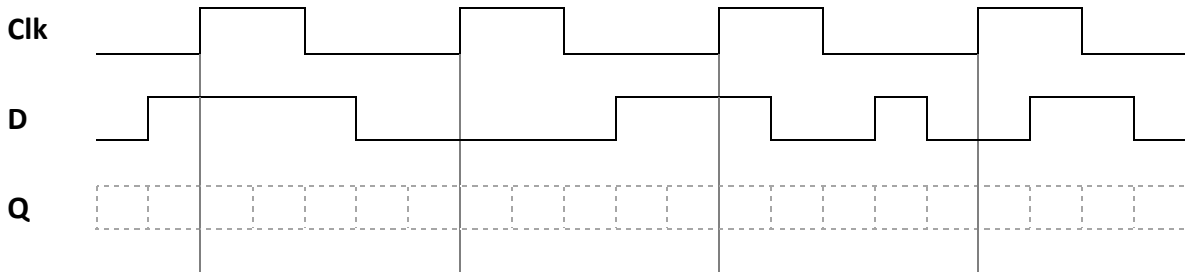
2.0 Complete the characteristic table for both versions of the SR latch. Do both versions function properly as a latch?

SR NOR Latch		
S	R	Action
0	0	<i>Keep State</i>
0	1	$Q =$
1	0	$Q =$
1	1	<i>Restricted Combination</i>

\overline{SR} NAND Latch		
S	R	Action
0	0	
0	1	$Q =$
1	0	$Q =$
1	1	

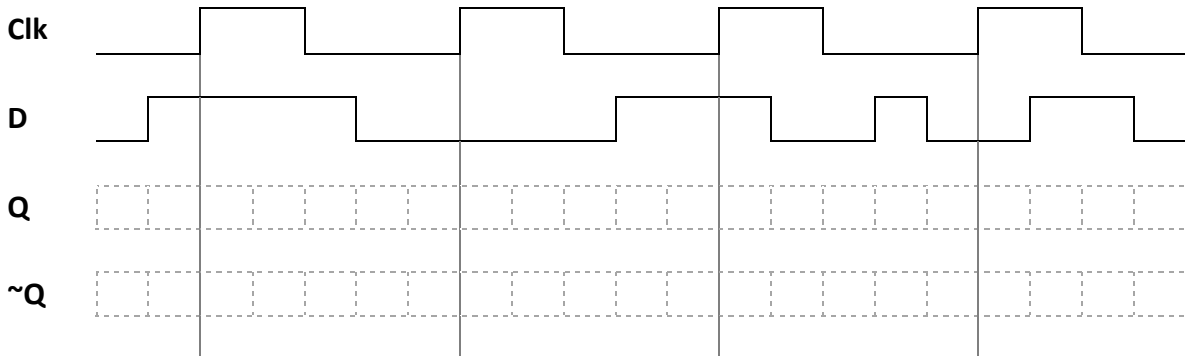
Hardware results demonstrate a good circuit. TA Initials: **NOR**_____ **NAND**_____

3.0 Complete the timing diagram below for your Gated D Latch. What is the difference between this gated latch and the previous basic latches?



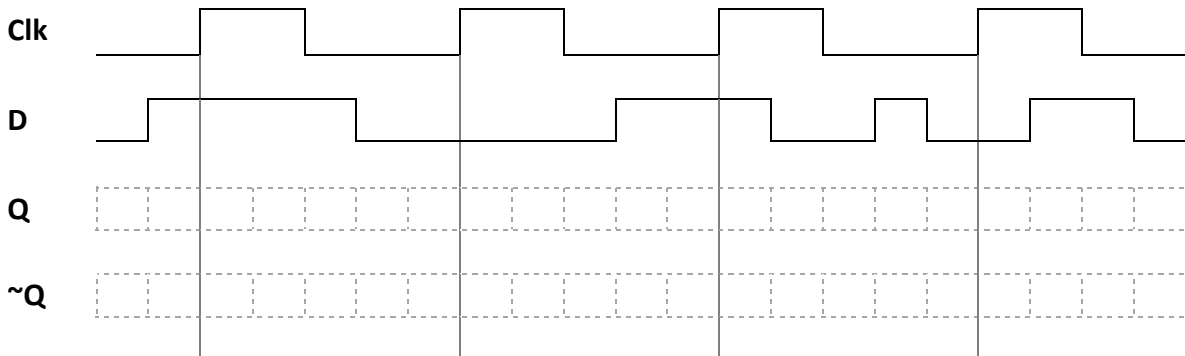
Hardware results demonstrate a good circuit. TA Initials: _____

4.0 Complete the timing diagram below for your Negative-Edge-Triggered D Flip-Flop.



Hardware results demonstrate a good circuit. TA Initials: _____

Complete the timing diagram below for your Positive-Edge-Triggered D Flip-Flop.



Hardware results demonstrate a good circuit. TA Initials: _____