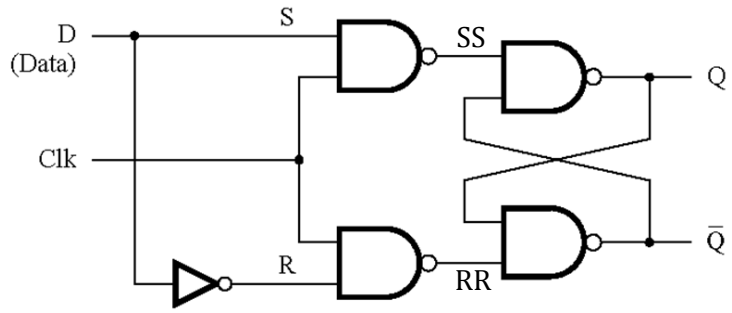
Cpr E 281 RC08
WEEK 11
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Recitation Material for Week 11
Tasks to do in the recitation section
Assigned Date: Tenth Week

T1. Answer any general questions about the materials covered in the second midterm exam.
T2. Answer any general questions about Lab 08.
T3. Solve the following problems.

1. Consider a T flip flop. Let Clk be a periodical signal (switches from 1 to 0 or from 0 to 1) every 1 micro second. Let T=1. Describe the waveform of the output Q.
2. Draw waveforms for signals D, Clk, S, R, SS, RR, Q and Q' for the gated D-latch circuit below (same as Fig. 5.7(a) in textbook) for 16 time steps. Assume Q=0 and Q'=1 initially. Assume D = 0 from time steps 0 to 6 and then D=1. Clk is 0 from time steps 0 to 7 and then Clk = 1. Assume each gate has a delay of one time step.



3. A TD flip flop has two inputs, C and I. When C=0, the TD FF acts as a D FF, where D=I. When C=1, the TD FF acts as a T FF, where T=I. Design a TD FF using one JK flip flop and several other simple gates like AND, OR, NOT, and XOR. Please make your design as minimal as possible.
4. The universal flip-flop has two operation select lines S2 and S1, and two inputs I2 and I1. It can work as the SR, D, JK or T flip-flops depending on the values of S2 and S1, and the inputs I2 and I1 act as the flip-flop inputs as given below. For example, according to the table below, when S2 = 0 and S1 = 1, the flip-flop works as a D flip-flop. I1 is equal to D if I2 = 0, while I1 is equal to D if I2 = 1. Convert a JK flip-flop to a universal flip-flop using two 2-to-1 multiplexers at the input of J and K terminals and S1 as their select. Identify inputs of the muxes.

S2	S1	Operation	I2	I1
0	0	SR flip-flop	S	R
0	1	D flip-flop	0	D
0	1	D flip-flop	1	D'
1	0	JK flip-flop	J	K
1	1	T flip-flop	0	T
1	1	T flip-flop	1	T'