Cpr E 281 RC09
WEEK 12
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

# Recitation Material for Week 12
# Tasks to do in the recitation section
# Assigned Date: Eleventh Week

T1. Review HW09 problems and solve any problems that the students point out they had difficulties with.
T2. Answer any general questions about HW10 and Lab 10.
T3. Solve the following problems.

1. Using D flip flops, and multiplexers, design a 5-bit shift register that has a control input, *S*, and a data input, *Input*:
   - If *S=0* when a clock edge arrives, the register shifts right by one bit, and the *Input* is stored in the leftmost flip flop.
   - If *S=1* when a clock edge arrives, the register shifts right by two bits, and the *Input* is stored in the second flip flop from the left, while a zero is stored in the leftmost flip flop.

   Your design should be as minimal as possible.

2. A D flip-flop with synchronous clear and preset has two extra inputs clear *C* and preset *P* besides D and Clock. Setting *C*=0 will force Q to 0 at the next clock edge while setting *C*=1 will not affect the state of the flip-flop. Setting *P*=0 will force Q to 1 at the next clock edge while setting *P*=1 will not affect the state of the flip-flop. *C* and *P* should not be set to 0 at the same time. (Please refer to Sec. 5.4.3 of textbook.)
   (a) Implement a 3-bit synchronous up-counter with enable using D flip-flops with synchronous clear and preset and a minimal amount of logic.
   (b) Modify the counter in part (a) to implement the counting sequence 000, 001, 010, 011, 100, 101, 000, .... by setting the *C* and *P* inputs appropriately.
   (c) Modify the counter in part (a) to implement the counting sequence 000, 001, 010, 011, 101, 000, .... by setting the *C* and *P* inputs appropriately.

3. In Question #2 above, a 3-bit synchronous up-counter with enable is constructed using D flip-flops with synchronous clear and preset. The counter is then modified to generate some special counting sequences.
   (a) Suppose the clear (C) and preset (P) inputs of the D flip-flops are asynchronous (rather than synchronous). Assume the values of the flip-flops are changed in an extremely short time after either C or P is set to 0. Show how to generate the counting sequence 000, 001, 010, 011, 100, 101, 000, .... by setting the C and P inputs appropriately. *Hint:* The idea is that when a count of 110 is detected, all flip-flops should be cleared asynchronously. In here, we assume that it is not a problem for the count to be 110 for a very short period of time.
   (b) In practice, the counter implemented in part (a) has a problem if flip-flops have different speeds. Please describe what the problem is.

4. Design a 6-bit ring counter using a 3-bit synchronous up counter with synchronous clear and a 3-to-8 decoder with enable, and a minimal number of gates.