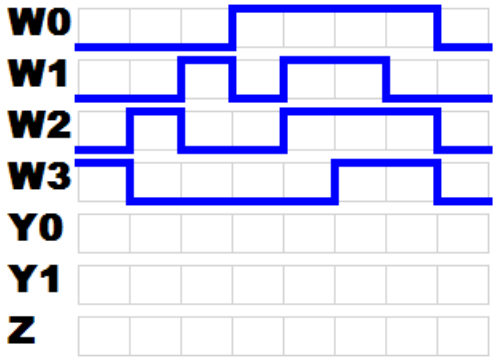
Cpr E 281 HW08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

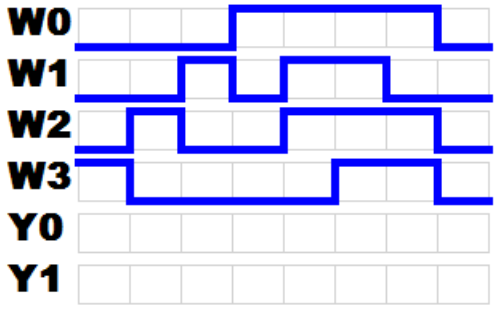
Representation and Arithmetic
Assigned: Week 9
Due Date: Oct. 28, 2019

P1 (15 points): Given a 3-bit input A, 1-bit input P, 1-bit input Q, a 6-bit adder, some 2-to-1 MUXes, some NOT gates, and some XOR gates:
A: Design a circuit that produces a 6-bit integer B such that B=3+A if P=0 and produces B=5-A if P=1.
B: Design a circuit that produces a 6-bit integer C such that C=3A if P=0 and produces C=5A+1 if P=1.
C: Design a circuit that outputs 6-bit integer D such that D=B if Q=0 and D=C if Q=1.

P2 (20 points): Fill in the timing diagrams below:
A: For a 4-to-2 priority encoder.

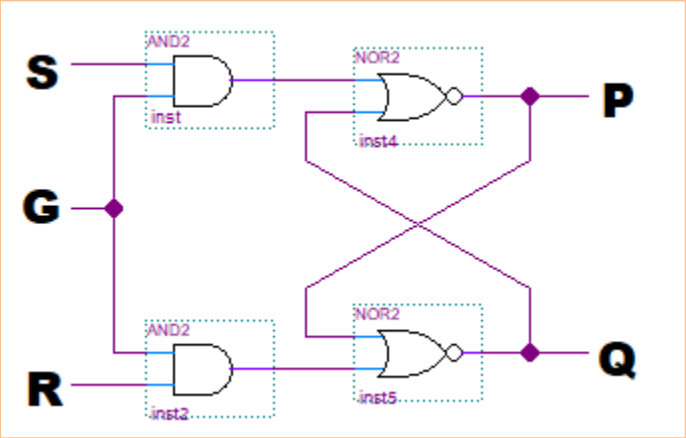


B: For a 4-to-2 binary encoder.



C: Which encoder's inputs are contrary to its input assumptions? Why?

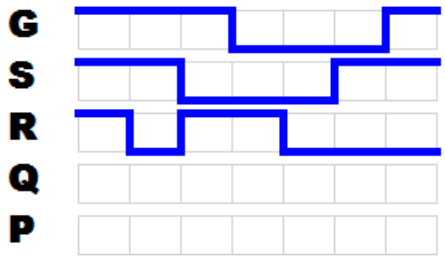
P3 (10 points): Consider the SR Latch shown below.



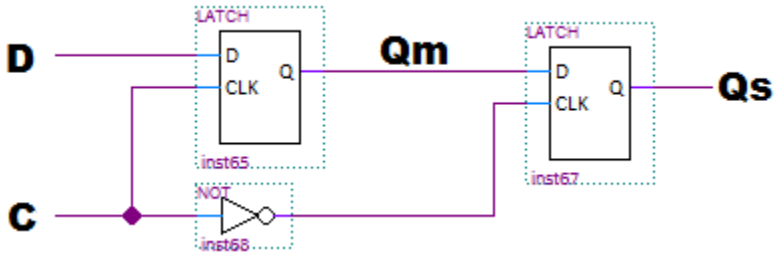
A: Complete the characteristic table.

G	S	R	Q	P
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

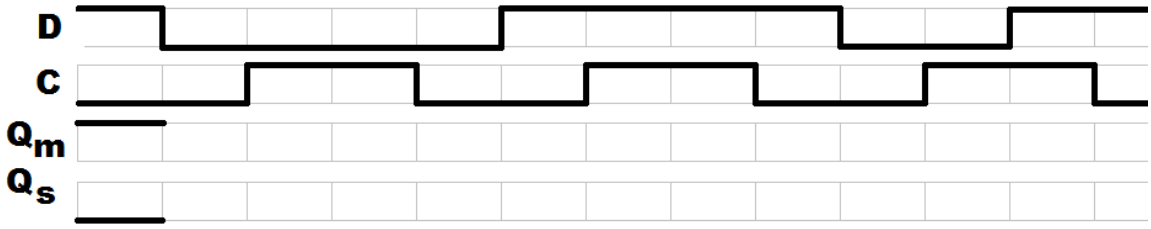
B: Complete the timing diagram shown below for outputs Q and P.



P4 (10 points): Answer the following questions based on the circuit shown below.



A: The latch that appears (twice) in the above circuit is a D Latch. Show the characteristic table for a D Latch.
B: Fill in the timing diagram for the values shown above.



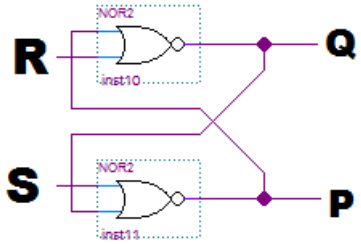
P5 (10 points): Show how a D Flip-Flop (DFF) can be made using a T Flip-Flop (TFF). Your circuit must contain all of the functionality of a DFF (PRESET and CLEAR implementations are not necessary), but must use only one TFF and one 2-1 MUX.

P6 (15 points): We want to create an LM-latch with the characteristic table shown below:

L	M	Q	P
0	0	0	1
0	1	No change	No change
1	0	No change	No change
1	1	1	0

A: Show the characteristic table for the SR Latch shown below.

S	R	Q	P
0	0		
0	1		
1	0		
1	1		



B: For each input combination to the LM-latch characteristic table shown above, write the values of S and R that will produce the output combinations. Then derive expressions for S and R in terms of L and M.
C: Draw the completed circuit for the LM-latch with the characteristic table based on the expressions derived in part B.

P7 (20 points): Answer the following questions about the Negative-Edge-Triggered Master-Slave DFF with PRESET_N and CLEAR_N connections, as shown in Figure 5.12 from the book. Suppose that D=1 and CLK=0. Answer the following questions about Q.
A: Ignoring PRESET_N and CLEAR_N (assume that they are not connected), what effect does pulsing the clock have on Q in this circuit?
B: What effect does pulsing PRESET_N have on this circuit?
C: What effect does pulsing CLEAR_N have on this circuit?
D: What will be the value of Q if PRESET_N=0 and CLEAR_N=1?
E: What will be the value of Q if PRESET_N=0 and CLEAR_N=0?
F: What will be the value of Q if the clock is pulsed while PRESET_N=0?
G: What will be the value of Q if the clock is pulsed while CLEAR_N=0?
H: What will be the value of Q if the clock is pulsed while CLEAR_N=1 and PRESET_N=1?