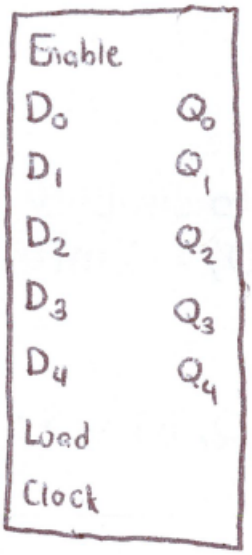
Cpr E 281 HW10
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

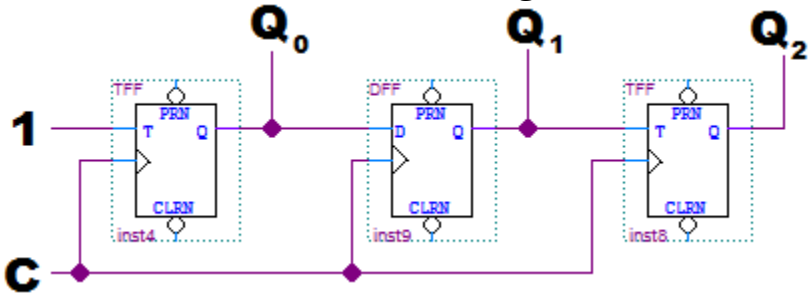
Counters and Sequential Circuits
Assigned: Week 12
Due Date: Nov. 11, 2019

P1 (15 points): Shown below is a 5-bit synchronous sequential counter with synchronous load. With Enable connected to VCC and Load connected to GND, assume that the Clock signal is connected to a 720kHz clock.



A: What are the frequencies of the outputs Q_0, Q_2, and Q_4?
B: Suppose that we instead used a 5-bit ring counter. What are the frequencies of the outputs Q_0, Q_2, and Q_4?
C: Suppose that we instead used a 5-bit Johnson counter. What are the frequencies of the outputs Q_0, Q_2, and Q_4?

P2 (10 points): The circuit below looks like a counter. The clock signal C is connected to a 24Hz clock signal.



A: What is the counting sequence of this circuit? Assume that the output Q is initially 000.
B: What is the steady-state frequency of the output signal from Q_2?

P3 (20 points): We want to design a circuit with input W and an output Z, where Z will equal 1 if, for the last three clock cycles, W has been 1.
A: Draw a state diagram for a Moore Finite State Machine (FSM) that

implements this circuit in four states, specified as follows:

B: Complete a state table for the above state diagram with the state assignments as shown below for state variables D_1 and D_0.

	W=0	W=1	Z
S-0 : 00			
S-I : 01			
S-II : 10			
S-III : 11			

C: Use K-maps to show that the output and next-state variables can be expressed as:

$$D_1^{new} = (w)(D_1 + D_0)$$
$$D_0^{new} = (w)(D_1 + \bar{D}_0)$$
$$z = D_1 D_0$$

D: Let's consider if the states were encoded as:

S-0 = 00, S-I = 01, S-II = 11, S-III = 10

Use K-maps to show that the output and next-state variables with this new encoding can be expressed as:

$$D_1^{new} = (w)(D_1 + D_0)$$
$$D_0^{new} = w\bar{D}_1$$
$$z = D_1 \bar{D}_0$$

E: Draw the circuit for this FSM (developed in part D) using only DFFs, AND gates, and one OR gate (Do not use any NOT gates).

P4 (15 points): Draw the state diagram for a Moore FSM that has a 1-bit input P and a 1-bit output Q. P will be either 1 or 0 on any particular clock cycle. Q=0 if P has been 1 for an even number of clock cycles; Q=1 if P has been 1 for an odd number of clock cycles.
A: Draw the state diagram for this Moore FSM.
B: Draw the state table for this FSM.
C: Draw a state assigned table for this FSM. The state should be the same as the output: Q.
D: Draw the truth table for this FSM's next-state variable.
E: Derive the expression for the next state variable and the output Q.
F: Draw the circuit for this FSM. If done properly, the circuit you create will implement a component that you have seen before. What component have you implemented?

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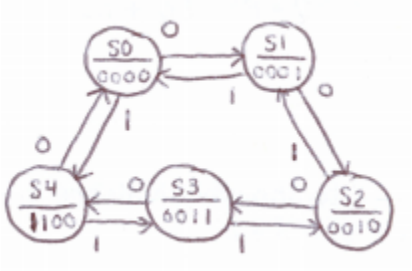
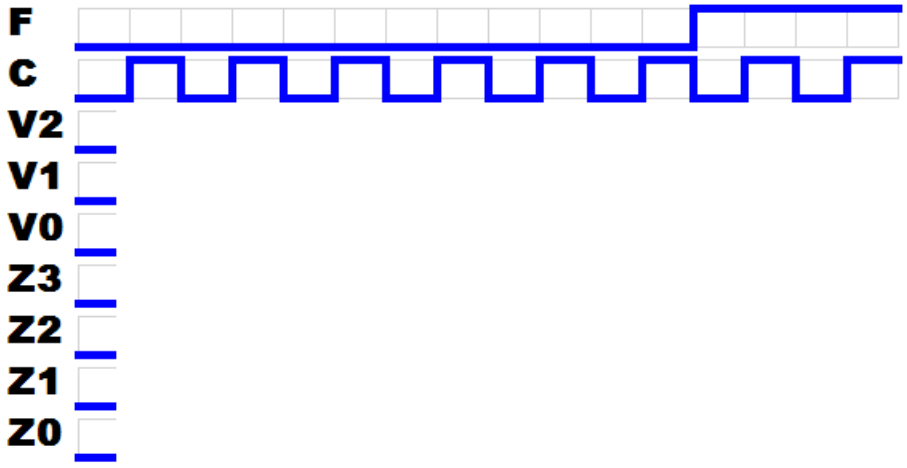
P5 (25 points): Given the FSM State Diagram below, observe that 0 moves clockwise through the diagram and that 1 moves counterclockwise. With this in mind, answer the following questions:



A: Complete the following state diagram with one-bit input F and four-bit input Z (z_3 z_2 z_1 z_0). Assume the state variables are V2, V1, and V0. Assume the state assignments are as follows: S0 = 000, S1 = 001, S2 = 010, S3 = 011, and S4 = 100. In the diagram below, the state and output all start at the value 0. The circuit is implemented with positive-edge-triggered flip-flops.



B: Is this a Mealy FSM or a Moore FSM?
C: What are the expressions for the four output bits for Z (z_3 z_2 z_1 z_0)?
D: Draw a state-assigned table for this FSM.
E: If the clock signal to this circuit is a 720kHz signal, what is the frequency of the output signal z_3 if F is kept at a constant 1?

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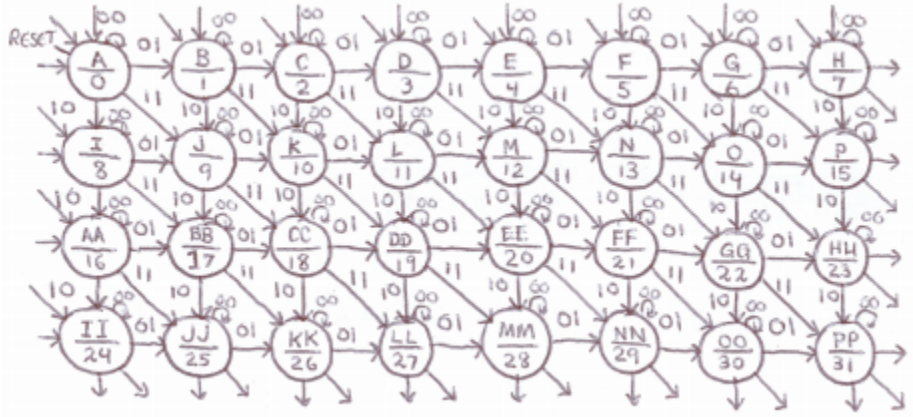
P6 (15 points): Shown below is a FSM with 32 states. The two inputs are X and Y, in this order (that is, from state A, X=0 and Y=1 leads to state B). Note that the arrows which extend off of the sides wrap around to the top to complete the pattern (that is, from state MM, input 10 goes to state E, and input 11 goes to state F). Input 01 always goes to the state on the right, 10 to the state beneath, and 11 downwards and to the right. The five output bits are, in order from most to least significant for the output integers: z_1 z_0 w_2 w_1 w_0. Answer the following questions:



A: What is the minimum number of state variables that can be used to implement this FSM?
B: What is the minimum number of TFFs that can be used to implement this FSM?
C: How many total state transitions exist in this FSM?
D: Suppose that input X were always connected to ground. Draw the new state diagram (hint: the reset state is always reachable). How many states and state transitions would be removed (note: a state transition is removed if its beginning state or its end state are removed)?
E: Suppose instead that input Y were always connected to ground. Draw the new state diagram. How many states and state transitions would be removed?
F: What two circuits implemented separately would implement this 32-state FSM? Why? (Hint: What FSM did the 32-state FSM reduce to in step D?)