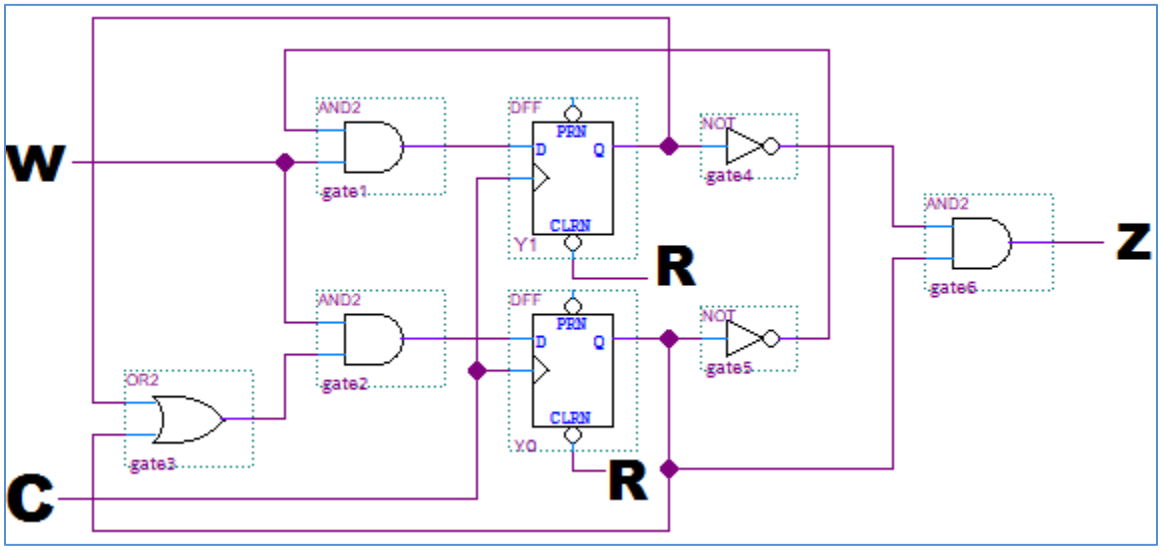
Cpr E 281 HW11
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned: Week 12
Due Date: Nov. 18, 2019

P1 (20 points): Create a Moore FSM for a circuit that outputs z=1 if input w=1 for the last three clock cycles. The states should be as follows: SA=00, SB=10, SC=11, and SD=01 are the states encountered in order from reset to completion of the three clock cycles.
A: Draw a state diagram for this FSM.
B: Create a state-assigned table for this FSM.
C: Use a K-map to show that the following circuit implements this FSM. Note the expressions should be in POS form, in accordance with the circuit below.



D: Let us instead create an FSM for a circuit with three inputs (x_2, x_1, and x_0) and outputs z=1 if at least two of the three inputs of x are one. The states should be set in the same order that they were in P1. Draw a state diagram for this FSM.

P2 (10 points): Design a Moore FSM that has one-bit input A and one-bit output B, where B=1 if the last six bits of A are 110100 (from earliest to latest). Draw the state diagram for this FSM.

P3 (10 points): Design a Mealy FSM that has one-bit input A and one-bit output B, where B=1 if the last six bits of A are 101001 (from earliest to latest). Draw the state diagram for this FSM.

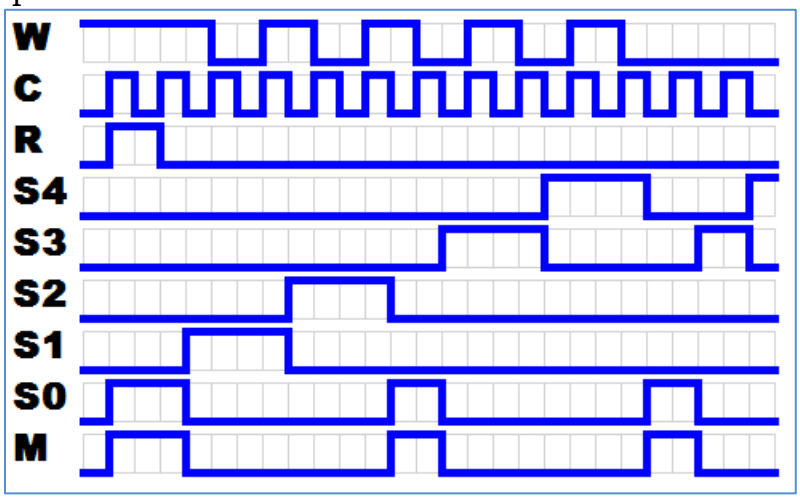
P4 (10 points): Design a Mealy FSM with the following specifications:

- There is a two-bit input X (x_1 x_0)
- There is a one-bit output Z
- Each cycle, the input X is added to the value in memory. Let us refer to this sum as V.

- The output Z=1 if V is greater than 5 but less than 10.

Draw the state table for this Mealy FSM.

P5 (20 points): A FSM has five states, five state variables, one-bit input W, one-bit reset R, and one-bit output M. The FSM has an output that corresponds with the timing diagram shown below. Answer the following questions.



A: The five states encountered in this timing diagram, in order, are A, B, C, D, and then E. What are the state encodings for these states?
B: Draw a state diagram for this FSM.
C: Draw a state-assigned table for this FSM.
D: This circuit is implemented using five DFFs. Derive expressions for the next state variables and the output M.
E: In addition to the five DFFs needed to implement this FSM, if no other gates are used, how many 2-to-1 MUXes are necessary to implement this circuit?
F: Explain why this particular circuit has the same number of states as it does state variables and why this isn't necessarily true of other circuits?

P6 (15 points): The FSM state diagram below has two inputs x_1 and x_0. In addition, it has two DFFs, three 4-to-1 MUXes, a single XOR gate, a single AND gate, and a single output bit Z. Answer the following questions about this FSM.

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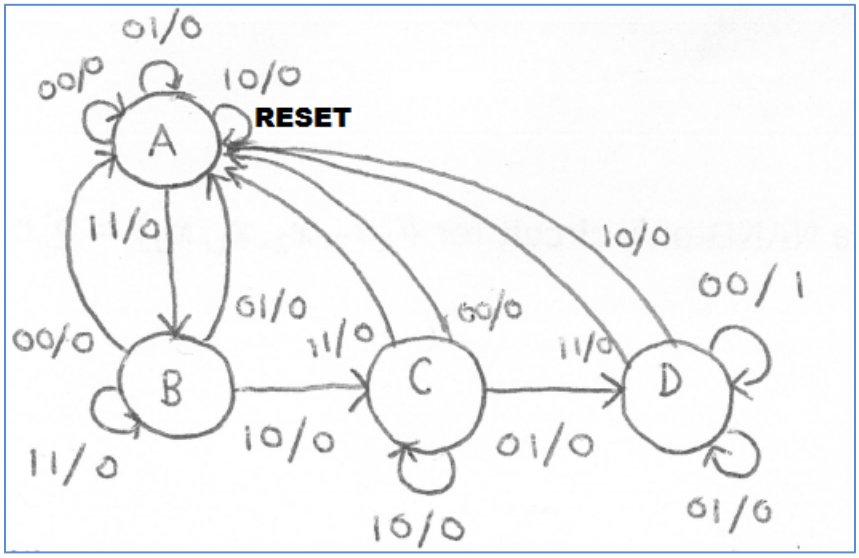
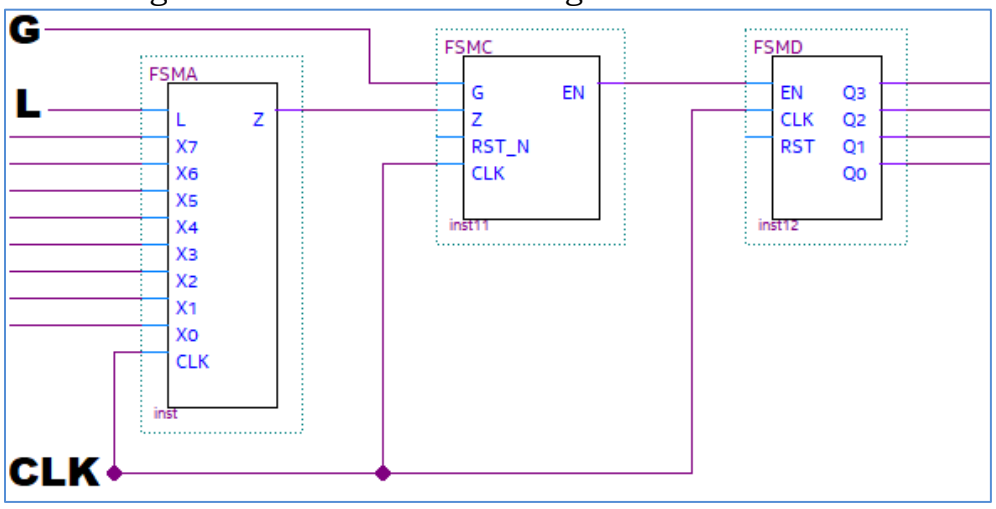


A: Is this a Moore FSM or a Mealy FSM?
B: The state encodings are A=00, B=01, C=10, and D=11. Write a state-assigned table for this state diagram.
C: Use K-maps to show that the expressions for the next-state variables and the output are as follows:

$$Y_1^{new} = \bar{x}_1 y_1 y_0 + \bar{x}_1 x_0 y_1 + x_1 \bar{x}_0 \bar{y}_1 y_0 + x_1 \bar{x}_0 y_1 \bar{y}_0$$
$$Y_0^{new} = \bar{x}_1 y_1 y_0 + \bar{x}_1 x_0 y_1 + x_1 x_0 \bar{y}_1$$
$$Z = \bar{x}_1 \bar{x}_0 y_1 y_0$$

D: Draw a circuit which implements this FSM as mentioned above: two DFFs, three 4-to-1 MUXes, one AND gate, and one XOR gate. Use the two-bit input X for the select lines.

P7 (15 points): This problem concerns the circuit diagram shown below, containing three FSMs connected together.



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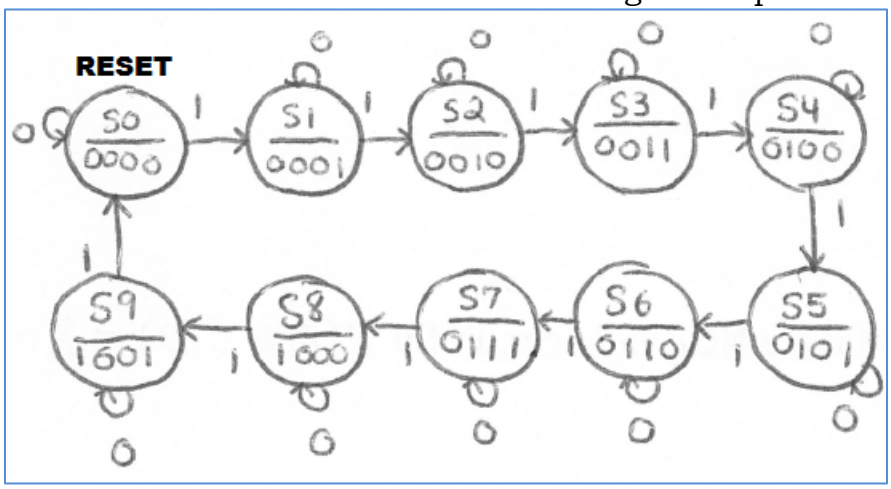
A: Design a circuit that has nine-bit input (L X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0) and one-bit output Z such that if L=0, the value in X is stored into memory (hereafter referred to as Y) on the clock signal and, if L=1, the value in memory (Y) is shifted right. The output Z is the least significant bit of the value Y in memory. It is not necessary to create an FSM to implement this circuit as it is a circuit that you have seen before. What circuit meets the above criteria (describe the width and input/output method)?
B: As this circuit is an FSM, how many states would it have?
C: Next, design a Moore FSM with two inputs (G and Z) and one output EN. If G=0 at any point on this FSM, the circuit always returns to the beginning and outputs 0. If G=1, then the circuit looks at Z from this circuit as an input and outputs EN=1 until the second 1 is observed on the input Z, at which point the circuit will always output EN=0 until G is set to zero and the cycle continues again. Draw the state diagram for this FSM. Note: G is not an asynchronous reset and should also be included within the state diagram.
D: The output of the previous FSM (EN) will be used as an input to the following state diagram with input EN and four-bit output F. What type of circuit does this Moore FSM state diagram implement?



E: If the user inputs the value X = 11101000 to the first FSM (by setting L=0 and G=0 and then advancing the clock one cycle), sets L=1 and G=1, and then starts the counter, what will be the final value of F?