CprE 281: Digital Logic
Midterm 1: Friday Nov. 1, 2019

Name: _____ **ID Number:**_____

Lab Section: **Mon 12-3 (#13)** **Tue 11-2 (#16)** **Wed 8-11 (#8)** **Thur 11-2 (#14)** **Fri 11-2 (#7)**
(circle one) **Tue 2-5 (#11)** **Wed 11-2 (#18)** **Thur 11-2 (#17)**
Tue 2-5 (#20) **Thur 2-5 (#10)**
Thur 5-8 (#9)

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name, lab section, and student ID number. TRUE / FALSE

(b) Removing a NOT gate from a D Flip-Flop makes it positive-edge triggered. TRUE / FALSE

(c) A 4-to-1 multiplexer can be built with 7 basic logic gates (AND, NOT, OR). TRUE / FALSE

(d) An XNOR gate can be constructed using only one 2-to-1 multiplexer. TRUE / FALSE

(e) The parallel input lines of an 8-bit register are one-hot encoded. TRUE / FALSE

(f) Shannon mapped Boolean logic to switches in his PhD dissertation. TRUE / FALSE

(g) Big Endian is used more often today than Little Endian. TRUE / FALSE

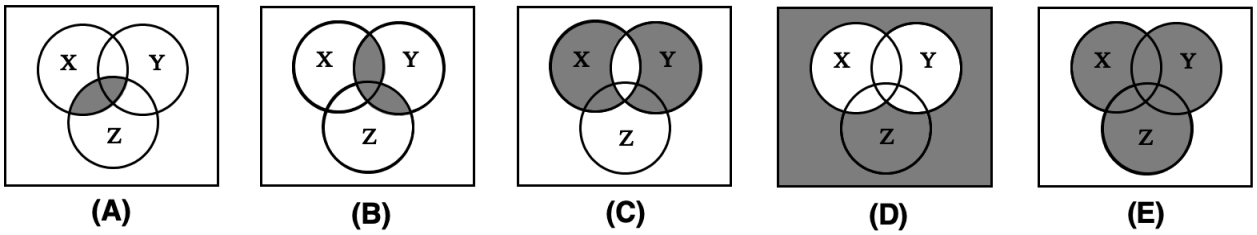
(h) In 1's complement notation it is possible to have both +0 and -0. TRUE / FALSE

(i) In 32-bit IEEE 754 format it is possible to have both +0.0 and -0.0. TRUE / FALSE

(j) Chewbacca's home planet is called Endor. TRUE / FALSE

2. Venn Diagrams (5 x 1p each = 5p)

Write the <u>Boolean expression</u> that corresponds to each Venn diagram below each figure.



3. Minimization with K-maps (3 x 5p each = 15p)

a) Draw the truth table for $f(a,b,c,d)=\Pi M(0, 2, 3, 7, 14) + D(8,15)$. **(5p)**

b) Use a K-map to derive the minimum-cost SOP expression for this function. **(5p)**

c) Use a K-map to derive the minimum-cost POS expression for this function. **(5p)**

4. Basic Circuits (3 x 5p each = 15p).
In all sub-problems, draw the complete wiring diagram using logic gates (no high-level graphical symbols are allowed in this problem). Clearly label all inputs and outputs.

(a) Gated D Latch (with NAND gates for the latch).

(b) 4-to-1 multiplexer.

(c) XOR gate, implemented using only AND, OR, and NOT gates.

5. Number Conversions (3p + 4p + 4p + 4p = 15p)

(a) Convert 163_{10} to binary.

(b) Convert the following 32-bit float number (in IEEE 754 format) to decimal.

1 1 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

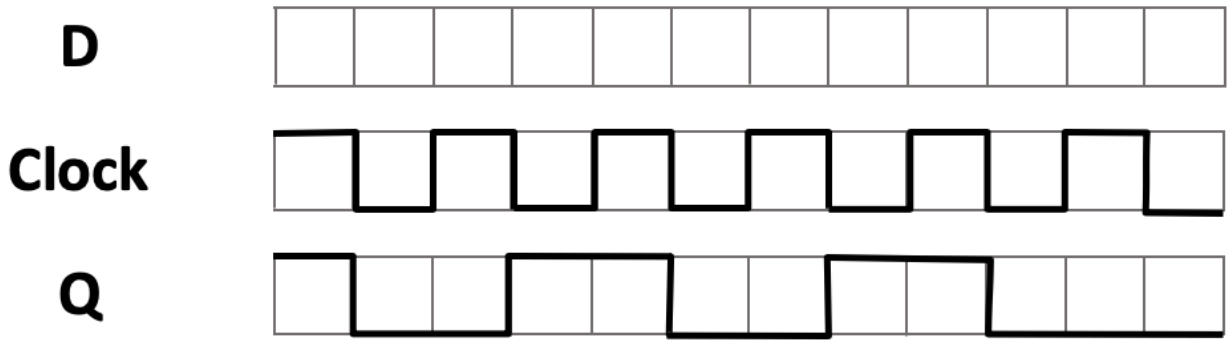
(c) Write down the 32-bit floating point representation (in IEEE 754 format) for 15.0

(d) Convert -53_{10} to an 8-bit binary number in 2's complement representation.

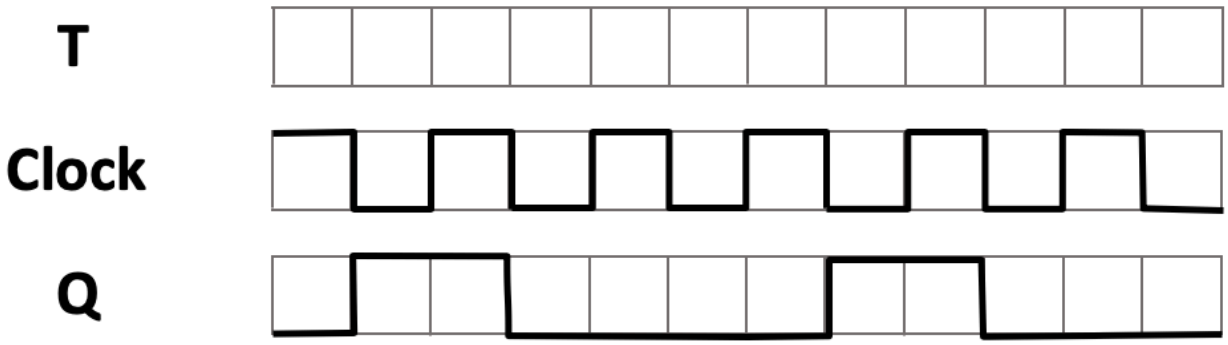
6. Flip-Flops and Timing Diagrams (3 x 5p = 15p)

Complete the timing diagram for the specified flip-flop such that the output Q will be as indicated. Assume that the input signal can change only on the vertical lines. Also, assume that the setup time t_{su} and the hold time t_h are each equal to the width of one square.

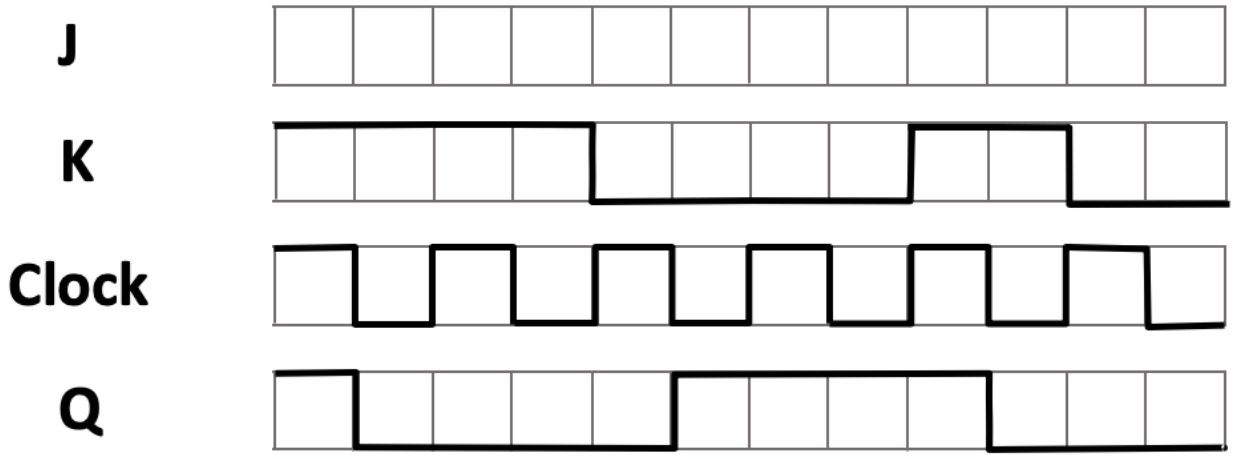
a) Complete the timing diagram for the D input to a negative-edge triggered D flip-flop.



b) Complete the timing diagram for the T input to a negative-edge triggered T flip-flop.



c) Complete the timing diagram for the J input to a negative-edge triggered JK flip-flop.



7. Full Adder (5p + 10p = 15p)

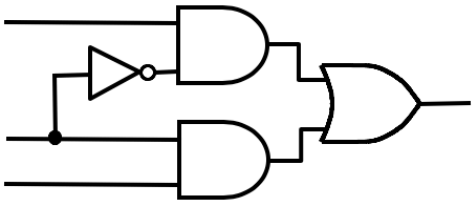
a) Draw the truth table for a full adder with inputs x_i, y_i, and c_i and outputs c_{i+1} and s_i. (5p)

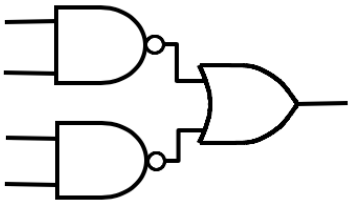
b) Implement a full adder with a <u>minimal</u> number of 4-to-1 multiplexers and <u>no other logic gates</u>. Assume that the input signals are available <u>only</u> in their non-inverted form, along with the constants 0 and 1. Clearly label all inputs, outputs, and pins of your circuit. (10p)

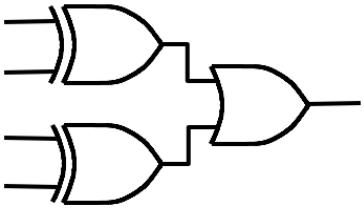
8. Alternative Implementation (10p)

Implement the logic expression in each sub-problem in three different ways using the circuits below. In this problem, you are not allowed to use any other logic gates. Assume that a and b are available in both their inverted and non-inverted form, along with the constants 0 and 1. Indicate with words if some implementations are not possible. Label all inputs and outputs.

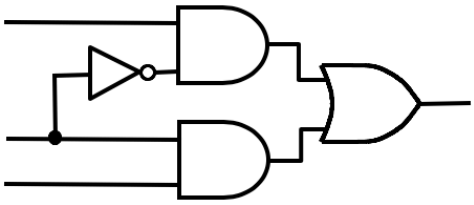
a) Implement in three different ways: $f = a + b$.

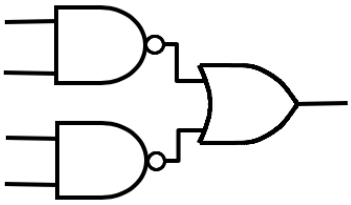


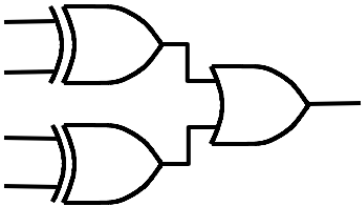




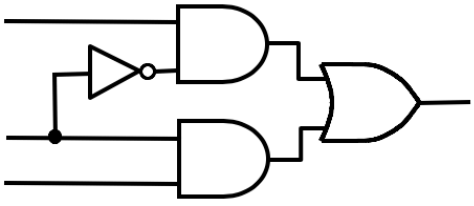
b) Implement in three different ways: $f = a + \overline{b}$.

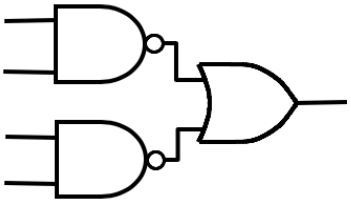


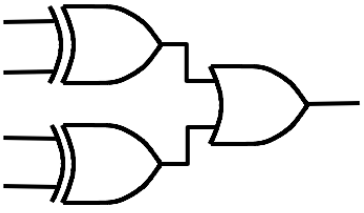




c) Implement in three different ways: $f = \overline{a\ b}$.

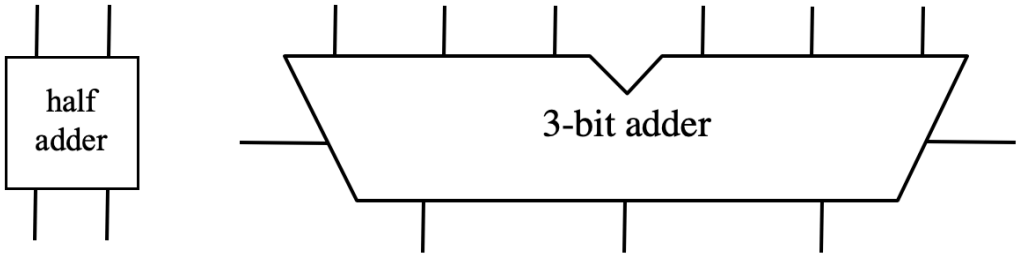






9. Adder/Subtractor with Overflow Detection (10p + 5p = 15p)

(a) You are given a 3-bit adder, but it is too small for what you need, and it also does not compute an overflow flag. Complete the wiring diagram below to implement a functional 4-bit adder/subtractor unit that can also detect when an overflow has occurred. Clearly label all inputs, outputs, and pins of your circuit.



(b) Explain the correct solution in 3-4 sentences.

10. Shifter Circuit (10p + 5p = 15p)

(a) Implement a shifter circuit that takes in a 4-bit unsigned binary number W and shifts all of its bits either to the left or to the right by 1 position. The direction of the shift is determined by one of the inputs to this circuit that is called R. If R=0, then the circuit shifts to the left. If R=1, then the circuit shifts to the right. In both cases the bit that is shifted out is ignored and the empty space that is created is padded with a zero. Label all inputs and outputs.

(b) Explain the correct solution in 3-4 sentences.

Question	Max	Score
1. True/False	10	
2. Venn Diagrams	5	
3. Minimization with K-maps	15	
4. Basic Circuits	15	
5. Number Conversions	15	
6. Flip-Flops	15	
7. Full Adder	15	
8. Alternative Implementation	10	
9. Adder/Subtractor	15	
10. Shifter Circuit	15	
TOTAL:	130	