

**P1 (8 points):** For the grid below, shade the boxes for each number in the column that can be represented with only 3-bits under the format for that particular row.

	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
Unsigned																	
Sign & Magnitude																	
1's Complement																	
2's Complement																	

**P2 (12 points):** Perform the following operations on the numbers and indicate if overflow occurs for each operation. All numbers are 6 bits wide (stored in 2's complement). Show your work and all carry bits.

$$\begin{array}{r}
 011001 \\
 + 000101 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 110011 \\
 - 101100 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 001001 \\
 + 010111 \\
 \hline
 \end{array}$$
  

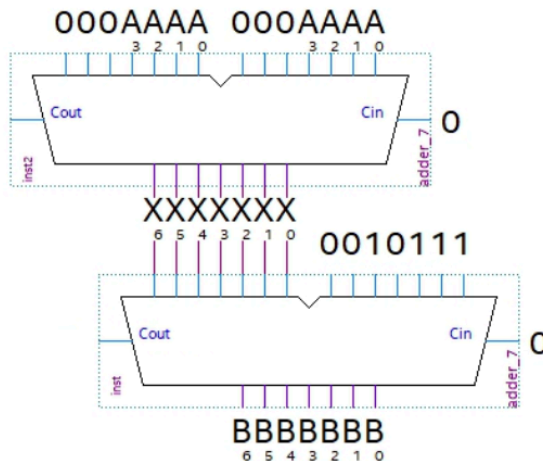
$$\begin{array}{r}
 101101 \\
 + 110110 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 011011 \\
 - 101001 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 110010 \\
 + 110111 \\
 \hline
 \end{array}$$

**P3 (16 points):** Let A be a three-bit unsigned number. Use a seven-bit adder (and NOT gates, as necessary) to design a circuit that calculates the following operations. Note that the output may be assumed as unsigned, unless it is possible for the operation to produce a negative answer, in which case, the output must be correct in 2's complement:

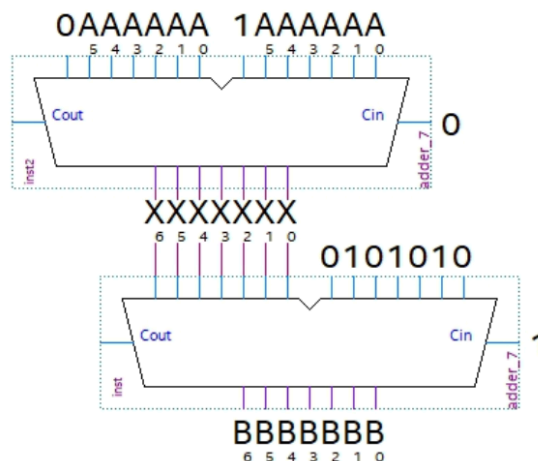
$$\begin{aligned}
 W &= 5A + 4 \\
 X &= A - 14 \\
 Y &= 34A + 18 \\
 Z &= 38 - 4A
 \end{aligned}$$

**P4 (18 points):** In the circuits below, find the algebraic expression for **B(X)** (B in terms of X) and **X(A)** (the expression for X in terms of A). Overflow is ignored, but all results that would produce an overflow are not be accepted as an allowed input.

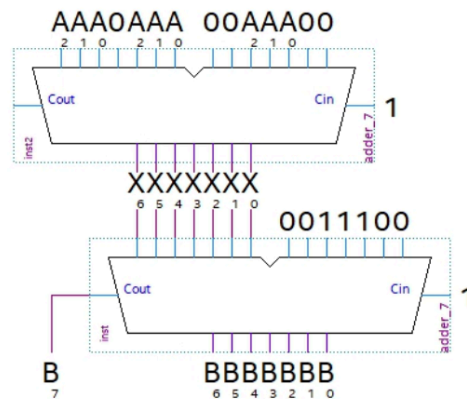
- a) Here, A is a 4-bit unsigned integer, X is a 7-bit unsigned integer, and B is a 7-bit number in 2's complement.



- b) X and B are 7-bit 2's complement integers, but A is a 6-bit unsigned integer.



- c) A is a 3-bit unsigned integer, X is an unsigned 7-bit integer, and B is an 8-bit unsigned number. Hint: consider the role of  $B_7$  when the value of X is large.



**P5 (16 points):** Convert the following numbers to IEEE 754 Single-Precision Floating Point format. Write your answer in **hexadecimal**, and indicate if an answer has a repeating mantissa:

- 49
- 250
- 25/128
- 3.3

**P6 (8 points):** Convert the following numbers from IEEE 754 Single-Precision Floating Point format to decimal. Note that each number is given in hexadecimal. You may leave the result as a fraction.

- $C4000000_{16}$
- $421C0000_{16}$
- $BF700000_{16}$
- $3F840000_{16}$

**P7 (8 Points):** Answer the following questions about MUXes and decoders.

- How many 1-bit 2-to-1 MUXes are necessary to create an 8-bit 2-to-1 MUX?
- How many 1-bit 2-to-1 MUXes are necessary to create a 1-bit 8-to-1 MUX?
- How many 2-to-4 decoders are necessary to create a 4-to-16 decoder?
- How many 3-to-8 decoders are necessary to create a 6-to-64 decoder?

**P8 (14 points):** Implement the function  $G(w, x, y, z) = \sum m(5,7,8,10,13,14,15)$  as follows:

- Use a K-map to show that  $G$  can be written as  $G = xz + w\bar{x}\bar{z} + wy\bar{z}$
- Implement  $G$  using only a minimal number (3) of 2-1 MUXes and no other gates (NOT gates are not allowed, either). Hint: Use Shannon's Expansion Theorem a few times.