

**P1 (10 points):** Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Repeat this problem for a Mealy-type FSM.

**P2 (10 points):** Let us make a Moore FSM that determines if a number is divisible by three.

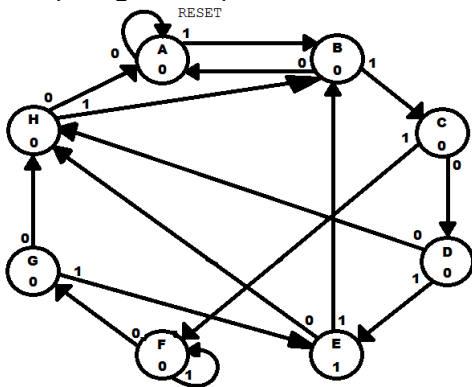
- Draw the state diagram for a Moore FSM that receives an input  $W$  and produces an output  $Z=1$  only if the accumulated value  $V$  is a multiple of 3. When  $W$  is input, the new value is as follows:  $V_{new} = 2V + W$ . The FSM should have only three states, where each state corresponds to the value of  $V \bmod 3$ .
- Use your state diagram to determine if the 36-bit number 101100101110110110010101100101110110110 is a multiple of 3.

**P3 (20 points):**

A counter has a special counting sequence: 0, 5, 7, 1, 0, 5, 7, 1, and so on. Design this counter with minimal number of states.

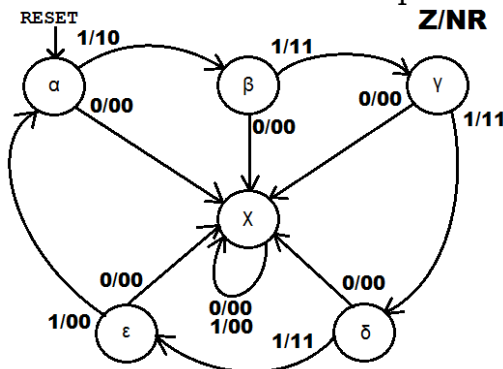
- Draw a state diagram for the counter.
- Construct a state-assigned table including the next state and output.
- Draw the circuit diagram for the counter using D flip-flops.
- Repeat (c) using T flip-flops.
- Repeat (c) using JK flip-flops.

**P4 (10 points):** Reduce the state diagram below to use only five states.



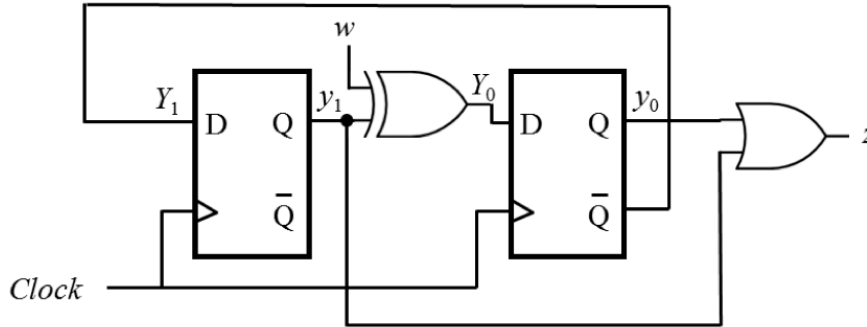
**P5 (25 points):** You have a modulo-256 down counter (**operand counter**) with 8-bit output and one-bit input N (the **operand counter** counts down for each clock cycle where N=1). Assume that this **operand counter** is initially holding an unknown value V. You also have a second modulo-256 up counter (**result counter**) with one-bit input R. The **result counter** counts up for each clock cycle where R=1. This is used to store an 8-bit mathematical result W. Design the following:

- Design a circuit that outputs Z=1 if the **operand counter** is nonzero.
- The following FSM state diagram receives input Z and outputs N (which decrements the down counter) and R (which increments the up counter). When the down counter reaches zero, algebraically describe the value of the up-counter W in terms of the initial value of the down counter V. Also, denote if the answer will be rounded down or rounded up to the nearest integer.



- Design a FSM state diagram that fills the **result counter** with the value  $W = \lfloor \frac{V}{5} \rfloor$  (the result of division rounded down to the nearest integer) using the one-bit input Z, output R (R is the input which enables the up counter), and output N (N is the input which enables the down counter). You only need to draw the state diagram; the destination for each FSM connection should be specified as above. When the result counter contains the correct value, the result counter should remain unchanged for any future clock cycles.
- Repeat part II but produce the result  $W = \lceil \frac{3V}{5} \rceil$  (here, the quotient is rounded up to the nearest integer).
- Repeat part II but produce the result  $W = \lceil \frac{5V}{3} \rceil$  (round up).

**P6 (15 points):** A FSM has two D flip-flops, an input  $w$ , and an output  $z$ . The circuit diagram is shown below.



- Find the logic expressions of  $Y_1$ ,  $Y_0$ , and the output  $z$ .
- Show the state-assigned table of the FSM.
- Draw the state diagram of the FSM.

**P7 (10 points):** The FSM below looks like a counter. Draw a state diagram which illustrates its counting sequence.

