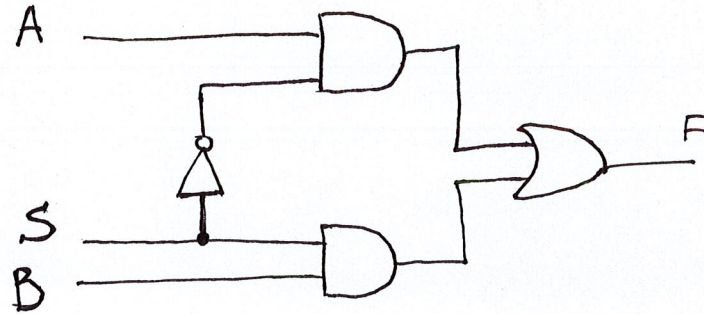
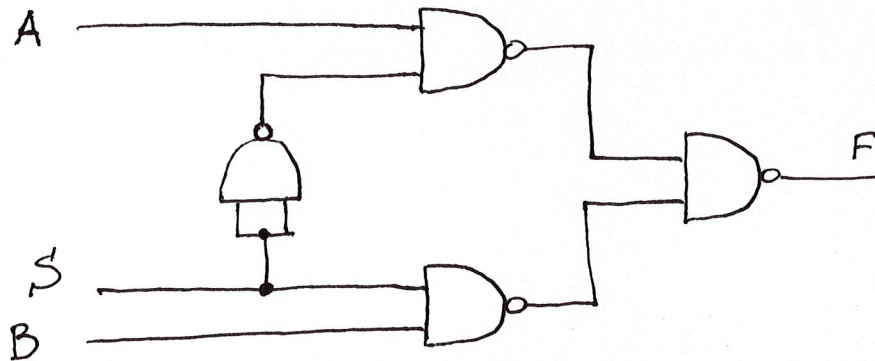


3. Multiplexer (5p + 5p = 10p)

- (a) Draw the circuit diagram for a 2-to-1 multiplexer, which has a Boolean expression $F = \overline{S} A + S B$



- (b) Redraw your circuit form a) using only NAND gates. Clearly label all inputs and outputs of the circuit.



4. Number Conversions (4 x 5p each = 20p)

(a) Convert 10101101_2 to decimal

$$\begin{aligned}
 & 1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = \\
 & = 128 + 0 + 32 + 0 + 8 + 4 + 0 + 1 = \\
 & = 128 + 40 + 5 = \boxed{173}_{10}
 \end{aligned}$$

(b) Convert 123_{10} to binary

$$\begin{array}{r}
 123 / 2 = 61 \quad 1 \\
 61 / 2 = 30 \quad 1 \\
 30 / 2 = 15 \quad 0 \\
 15 / 2 = 7 \quad 1 \\
 7 / 2 = 3 \quad 1 \\
 3 / 2 = 1 \quad 1 \\
 1 / 2 = 0 \quad 1
 \end{array}$$

$\boxed{1111011}_2$

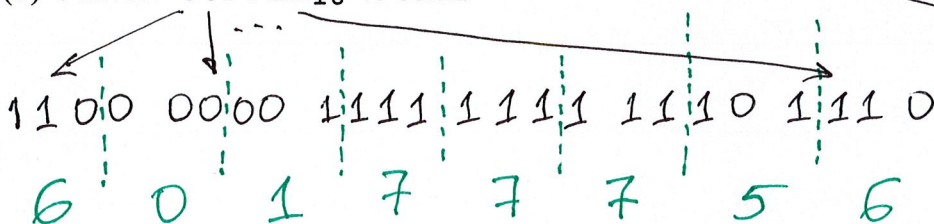
(c) Convert 227_{10} to hexadecimal

$$\begin{array}{r}
 227 / 16 = 14 \quad 3 \\
 14 / 16 = 0 \quad 14
 \end{array}$$

$\boxed{E3}_{16}$

(d) Convert COFFEE_{16} to octal.

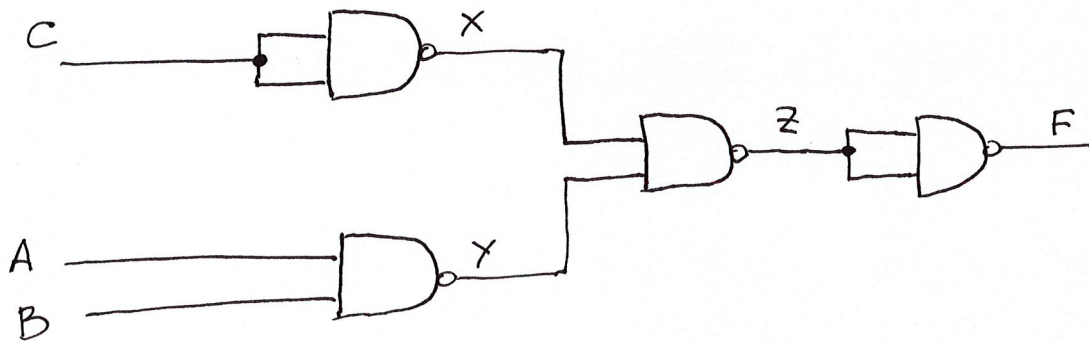
$\boxed{60177756}_8$



5. From Verilog Code to Circuit (10p)

Draw the circuit diagram that corresponds to the Verilog module shown below. Clearly label all inputs, outputs and wires of your circuit.

```
module mystery (A,B,C,F);  
  input A,B,C;  
  output F;  
  
  nand(X, C, C);  
  
  nand(Y, A, B);  
  
  nand(Z, Y, X);  
  
  nand(F, Z, Z);  
  
endmodule
```



6. Truth Tables (3 x 5p = 15p)

(a) Draw the truth table for the Boolean function $F(X, Y) = (X + \bar{Y})(\bar{X} + \bar{Y})$
 Show partial results for each of the two terms.

X	Y	$(X + \bar{Y})$			$(\bar{X} + \bar{Y})$			F
0	0	0	1	1	1	1	1	
0	1	0	0	0	1	0	0	
1	0	1	1	1	0	1	1	
1	1	1	1	0	0	0	0	

(b) Use a truth table to determine if the following Boolean equation is true:

$$\bar{A}\bar{C} + \bar{A}\bar{B} + \bar{A}BC = \bar{A}$$

They are equal.

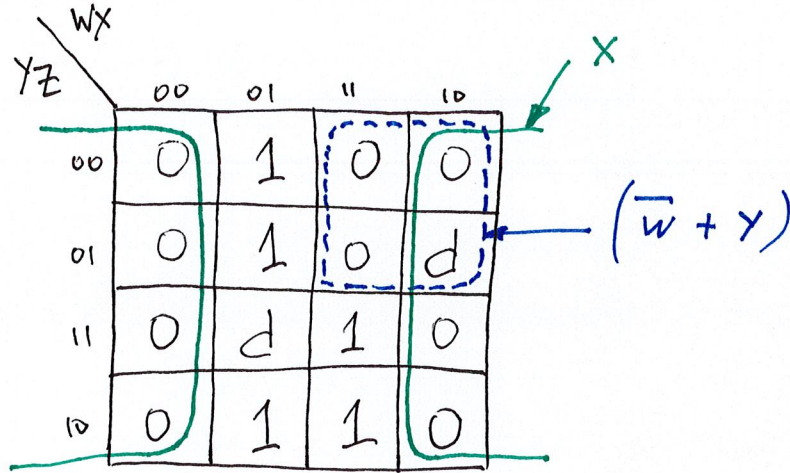
A	B	C	$\bar{A}\bar{C} + \bar{A}\bar{B} + \bar{A}BC$			LHS	RHS = \bar{A}
0	0	0	1	1	0	1	1
0	0	1	0	1	0	1	1
0	1	0	1	0	0	1	1
0	1	1	0	0	1	1	1
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

(c) Draw the truth tables for the following 5 logic gates: AND, OR, XOR, NAND, NOR.
 Clearly label which table corresponds to which gate.

X	Y	AND(x,y)	X	Y	OR(x,y)	X	Y	XOR(x,y)	X	Y	NAND(x,y)	X	Y	NOR(x,y)
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
0	1	0	0	1	1	0	1	1	0	1	1	0	1	0
1	0	0	1	0	1	1	0	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1	0	1	1	0	1	1	0

7. Derive the minimum POS expression using a K-map (10p + 5p = 15p)

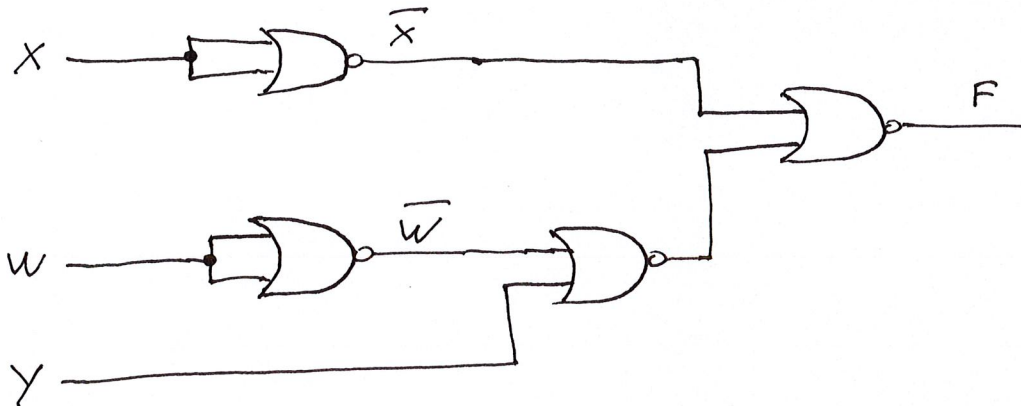
(a) Use a K-map to derive the minimum-cost POS expression for the following function
 $f(w, x, y, z) = \Sigma m(4, 5, 6, 14, 15) + D(7, 9)$



$$f = x \cdot (\bar{w} + y)$$

(b) Draw the circuit diagram for the expression derived in (a) using only NOR gates. Clearly label all inputs and outputs.

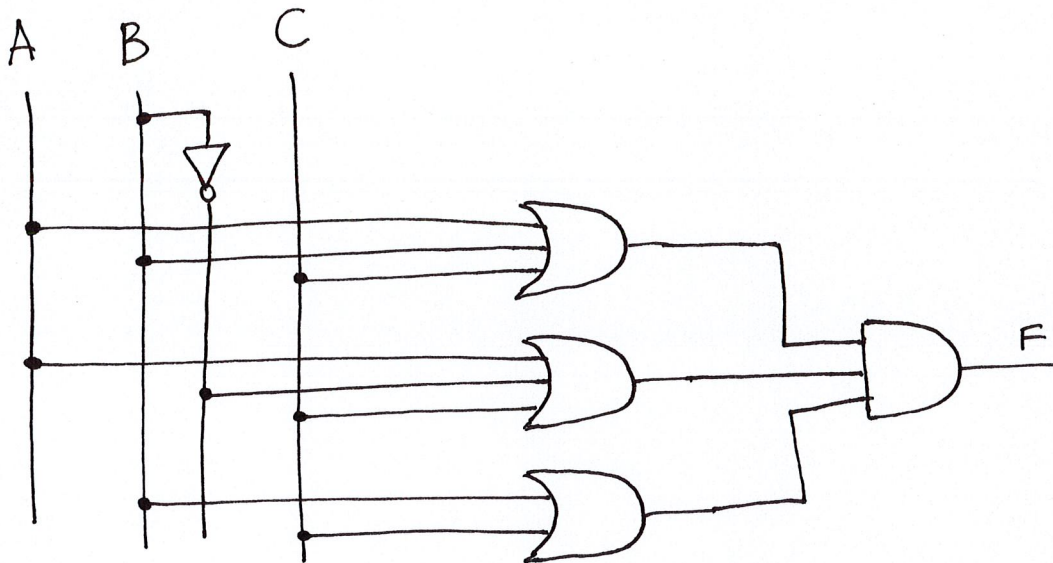
$$f = x \cdot (\bar{w} + y) = \overline{\overline{x \cdot (\bar{w} + y)}} = \overline{\overline{x} + \overline{(\bar{w} + y)}}$$



8. Circuit Simplification (3 x 5p = 15p)

(a) Draw the circuit diagram for this Boolean expression (don't simplify it yet)

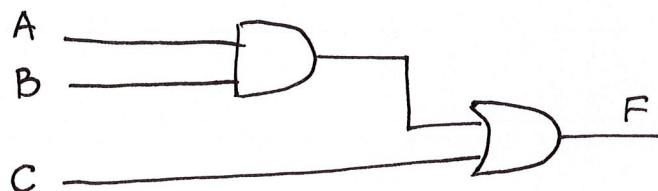
$$F(A, B, C) = (A + B + C) (A + \bar{B} + C) (B + C)$$



(b) Use the theorems of Boolean algebra to find a minimum-cost SOP expression for F.

$$\begin{aligned}
 F &= (\underline{A} + B + \underline{C}) (\underline{A} + \bar{B} + \underline{C}) (B + C) && // \text{Theorem 14.b} \\
 &= (A + C)(B + C) && // \text{expand} \\
 &= AB + AC + CB + \underbrace{CC}_C && // \text{Theorem 7.a} \\
 &= AB + C(\underbrace{A+B+1}_1) && // \text{Theorem 5.b} \\
 &= AB + C
 \end{aligned}$$

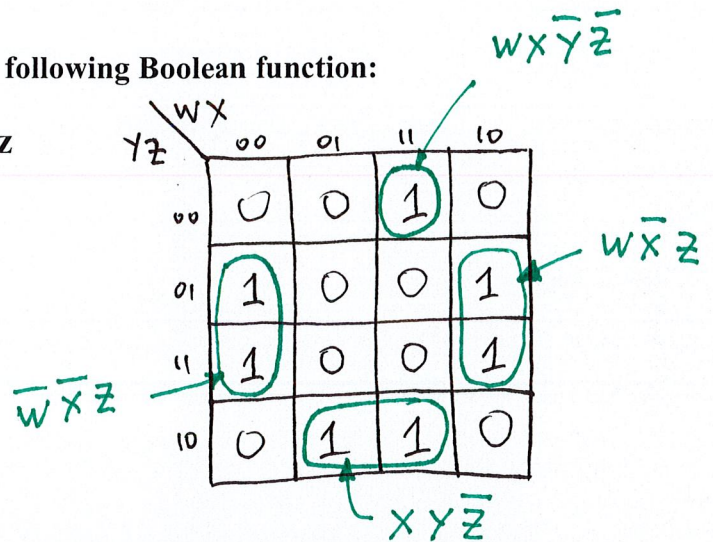
(c) Draw the circuit for the minimum-cost SOP expression. Label all inputs and outputs.



9. Minimization (3 x 5p = 15p)

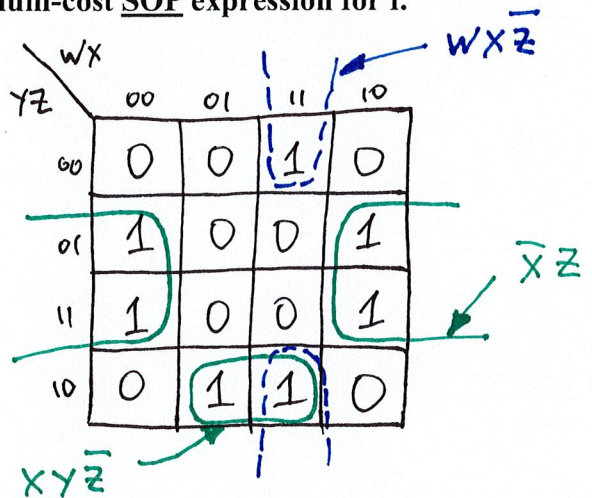
(a) Draw the K-map that corresponds to the following Boolean function:

$$f = w\bar{x}z + wx\bar{y}\bar{z} + xy\bar{z} + \bar{w}\bar{x}z$$

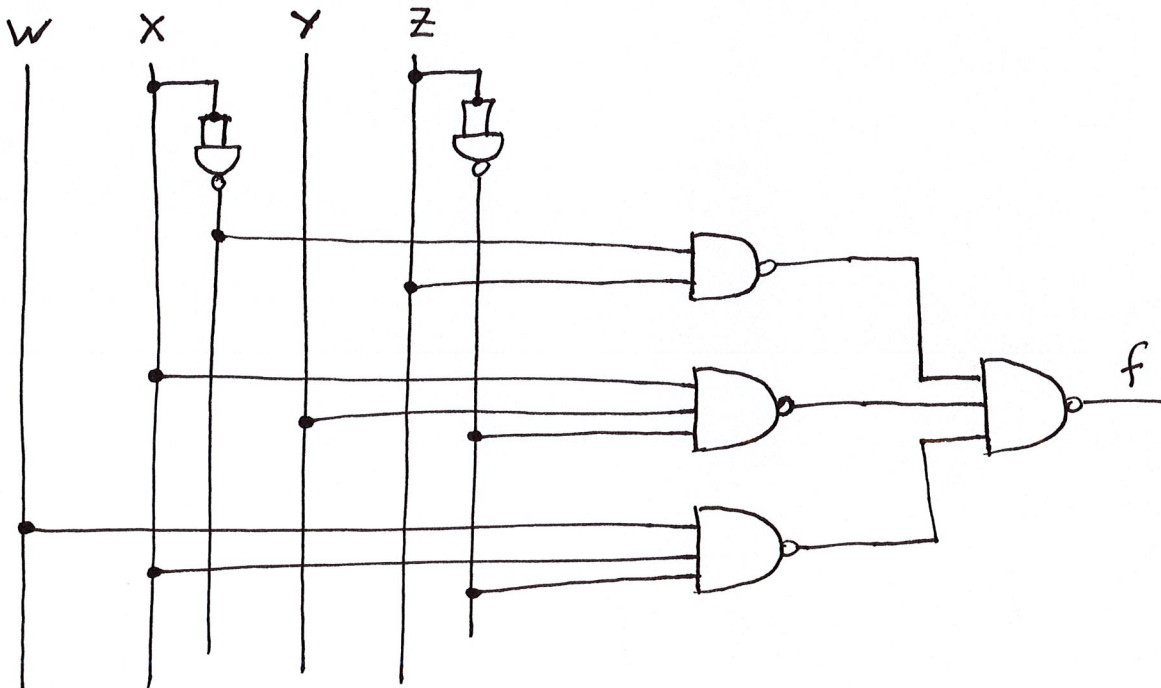


(b) Redraw the K-map from (a) and derive the minimum-cost SOP expression for f.

$$f = \bar{x}z + xy\bar{z} + wx\bar{z}$$



(c) Draw the circuit for the minimum-cost SOP expression using only NAND gates. Clearly label all inputs and outputs.



10. Boolean Algebra (10p + 5p = 15p)

- (a) Use the theorems of Boolean algebra to simplify the formula given below into a minimum-cost expression.
 (b) Draw the circuit diagram for the simplified expression using only NOR gates.

$$F(X, Y, Z) = \underbrace{\overline{(X + \bar{X}\bar{Y})}}_{\alpha} \underbrace{(X + Y + \bar{Z})}_{\beta} + \underbrace{\overline{(X + \bar{Y} + X\bar{Y})}}_{\gamma} \underbrace{(\bar{X}\bar{Y}Z)}_{\delta}$$

$$\alpha = \overline{X + \bar{X}\bar{Y}} = \overline{X + \bar{Y}} = \bar{X} \cdot \bar{\bar{Y}} = \bar{X}Y$$

→ Theorem 16.9

$$\beta = X + Y + \bar{Z} \quad // \text{no simplification here}$$

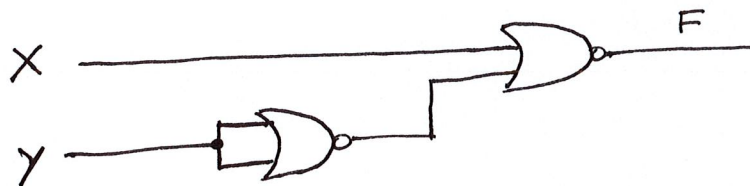
$$\gamma = \overline{X + \bar{Y} + X\bar{Y}} = \overline{X + \bar{Y}} = \bar{X} \cdot \bar{\bar{Y}} = \bar{X}Y = \alpha$$

$$\delta = \bar{X}\bar{Y}Z = \overline{\overline{\bar{X}\bar{Y}Z}} = \overline{\bar{\bar{X}} + \bar{\bar{Y}} + \bar{Z}} = \overline{X + Y + \bar{Z}} = \bar{\beta}$$

$$F = \alpha \cdot \beta + \underbrace{\gamma}_{\alpha} \cdot \underbrace{\delta}_{\bar{\beta}} = \alpha \beta + \alpha \bar{\beta} = \alpha (\underbrace{\beta + \bar{\beta}}_1) = \alpha = \bar{X}Y$$

(b) Draw using only NOR gates.

$$F = \bar{X}Y = \overline{\overline{\bar{X}Y}} = \overline{\bar{\bar{X}} + \bar{Y}} = \overline{X + \bar{Y}}$$



Question	Max	Score
1. True/False	10	
2. Three-Variable K-map	5	
3. Multiplexer	10	
4. Number Conversions	20	
5. Verilog Module	10	
6. Truth Tables	15	
7. POS with K-Map	15	
8. Circuit Simplification	15	
9. Minimization	15	
10. Boolean Algebra	15	
TOTAL:	130	