Sample Solutions

CprE 281: Digital Logic
Midterm 2: Friday Oct. 23, 2020

Name: _____ **ID Number:** _____

Lab Section:	**Tue 11-2 (#16)**	**Wed 8-11 (#8)**	**Thur 11-2 (#14)**	**Fri 11-2 (#7)**
(circle one)	**Tue 2-5 (#11)**	**Wed 11-2 (#18)**	**Thur 11-2 (#17)**	
			Thur 2-5 (#10)	

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name, lab section, and student ID number. TRUE / (FALSE)

(b) A 4-to-1 multiplexer can be used to construct a 2-to-1 multiplexer. (TRUE) / FALSE

(c) The total delay through an 8-bit ripple-carry adder is 4 gate delays. TRUE / (FALSE)

(d) A 1-to-16 demultiplexer can be made with five 2-to-4 decoders with enable. (TRUE) / FALSE

(e) A shift register can be used to divide the number stored in it by 2. (TRUE) / FALSE

(f) A negative-edge-triggered D flip-flop updates the value of the master latch when the clock is equal to 1. (TRUE) / FALSE

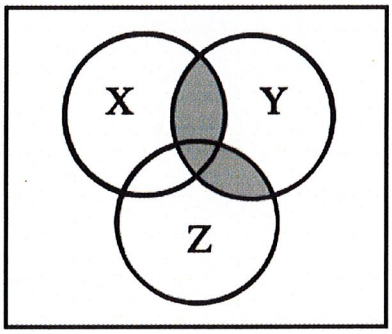
(g) A synchronous clear can be added to any D flip-flop using one AND gate. (TRUE) / FALSE

(h) A JK flip-flop can be constructed from a D flip-flop and one XOR gate. TRUE / (FALSE)

(i) For normal operation of a D flip-flop both clear_n and preset_n must be 0. TRUE / (FALSE)

(j) The plans for the first Death Star are kept in a safe on Scarif. (TRUE) / FALSE

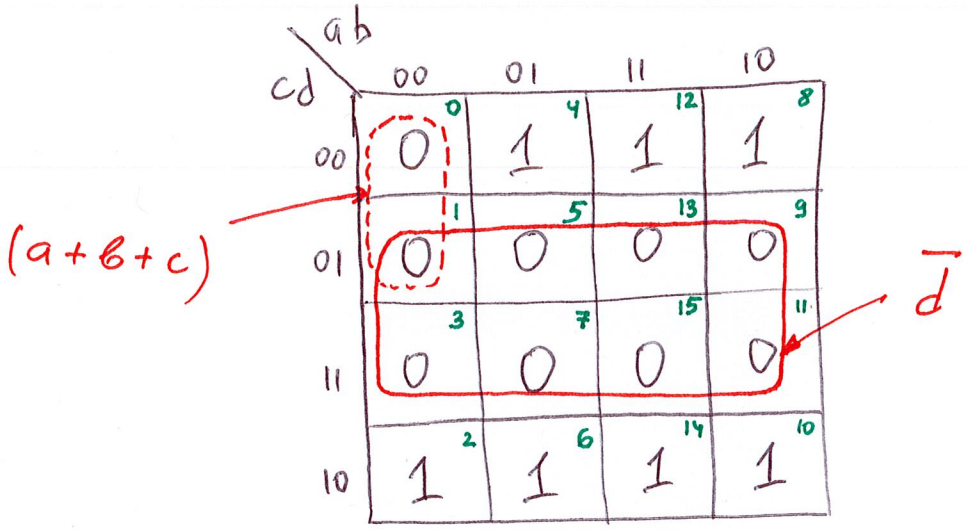
2. Venn Diagram (5p)
Draw the truth table that corresponds to the Venn diagram shown below.



X	Y	Z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

3. Even Numbers (3 x 5p each = 15p)

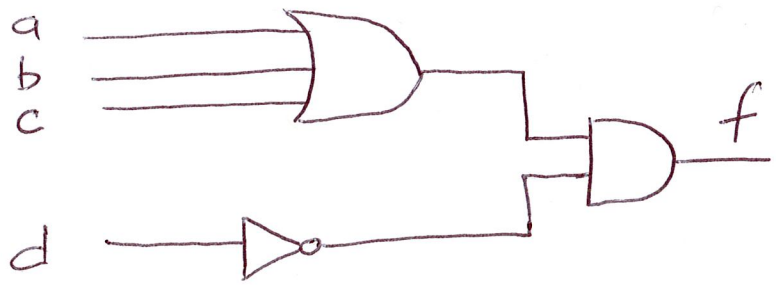
a) Draw the K-map for the Boolean function f(a,b,c,d) that is described as follows. The output of this function is 1 if the decimal representation of the 4-bit binary number abcd is a non-zero even number (i.e., 0 is treated as odd). Otherwise, the output is equal to 0. (5p)



b) Use the K-map to derive the minimum-cost POS expression for this function. (5p)

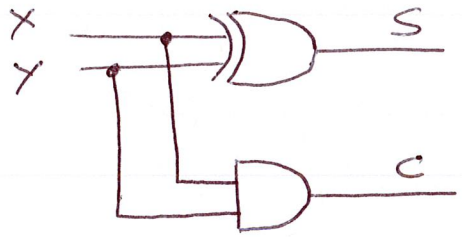
$$f(a,b,c,d) = \bar{d} \cdot (a+b+c)$$

c) Draw the circuit diagram for this function. Label all inputs and outputs. (5p)



4. Basic Circuits (3 x 5p each = 15p).
Draw the wiring diagrams for the circuits below. <u>Clearly label all inputs and outputs.</u>

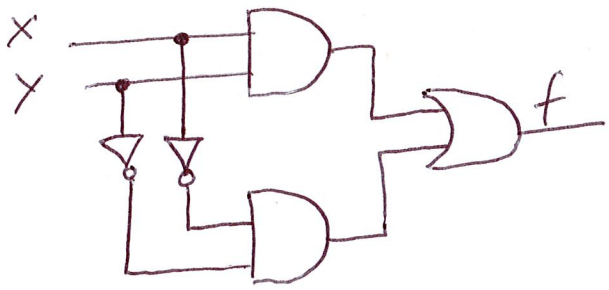
(a) Half-adder.



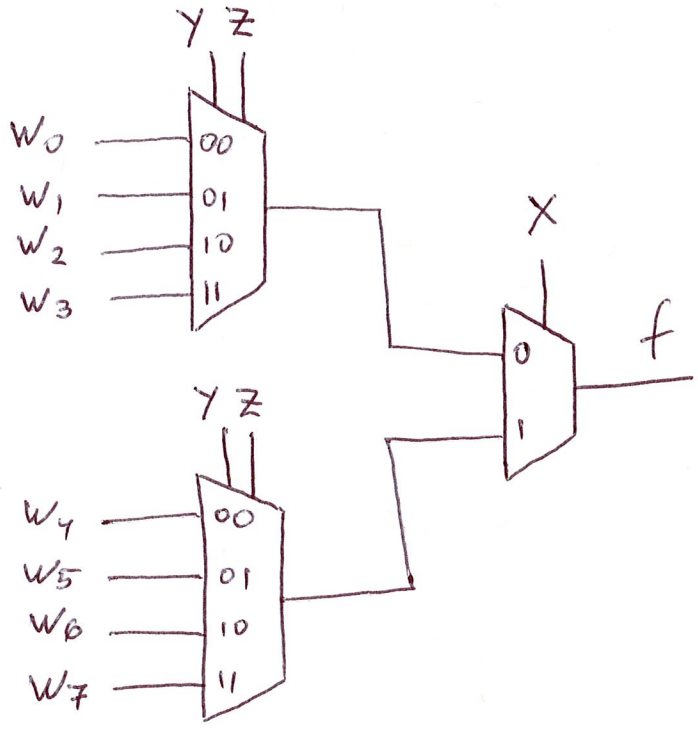
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b) XNOR gate, implemented using only AND, OR, and NOT gates.

$XNOR(X,Y) = X \cdot Y + \bar{X} \cdot \bar{Y}$



(c) 8-to-1 multiplexer implemented with two 4-to-1 multiplexers and one 2-to-1 multiplexer.



5. Number Conversions (3p + 4p + 4p + 4p = 15p)

(a) Convert 95_{10} to binary.

1011111_2

95/2 = 47 1
47/2 = 23 1
23/2 = 11 1
11/2 = 5 1
5/2 = 2 1
2/2 = 1 0
1/2 = 0 1

(b) Convert 5735_8 to hexadecimal.

Convert to binary and then to hexadecimal.

5 7 3 5
101 111 011 101

1011 1101 1101
B D D

(c) Write down the 32-bit floating point representation (in IEEE 754 format) for 6.5

6.5 / 4 = 1.625

6.5 = 4 × 1.625
= 2^2 × (1 + 0.5 + 0.125)
$2^{129-127}$ (2^{-1}, 2^{-3})

0 10000001 10100...0
20 zeros

(d) Convert -49_{10} to an <u>8-bit</u> binary number in 2's complement representation.

49/2 = 24 1
24/2 = 12 0
12/2 = 6 0
6/2 = 3 0
3/2 = 1 1
1/2 = 0 1

110001 (6-bit)
00110001 pad to 8-bit
negate
11001111

6. Comparison Logic (3 x 5p = 15p)

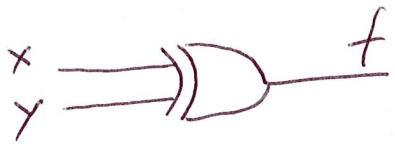
Given two Boolean variables x and y (i.e., both are 1-bit) your task is to draw truth tables and circuit diagrams for functions that perform the comparisons listed below.

a) Equal: draw the truth table <u>and</u> the circuit for a function f that outputs a 1 if x=y.

X	Y	X=Y
0	0	1
0	1	0
1	0	0
1	1	1

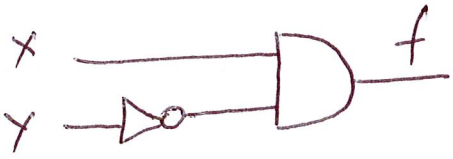
b) Not equal: draw the truth table <u>and</u> the circuit for a function f that outputs a 1 if x ≠ y.

X	Y	X≠Y
0	0	0
0	1	1
1	0	1
1	1	0



c) Greater: draw the truth table <u>and</u> the circuit for a function f that outputs a 1 if x>y.

X	Y	X>Y
0	0	0
0	1	0
1	0	1
1	1	0



7. Code Converter (8p + 7p = 15p)

A code converter has two inputs S_1 and S_0 and four outputs F_3, F_2, F_1, and F_0. The equations for the outputs are:

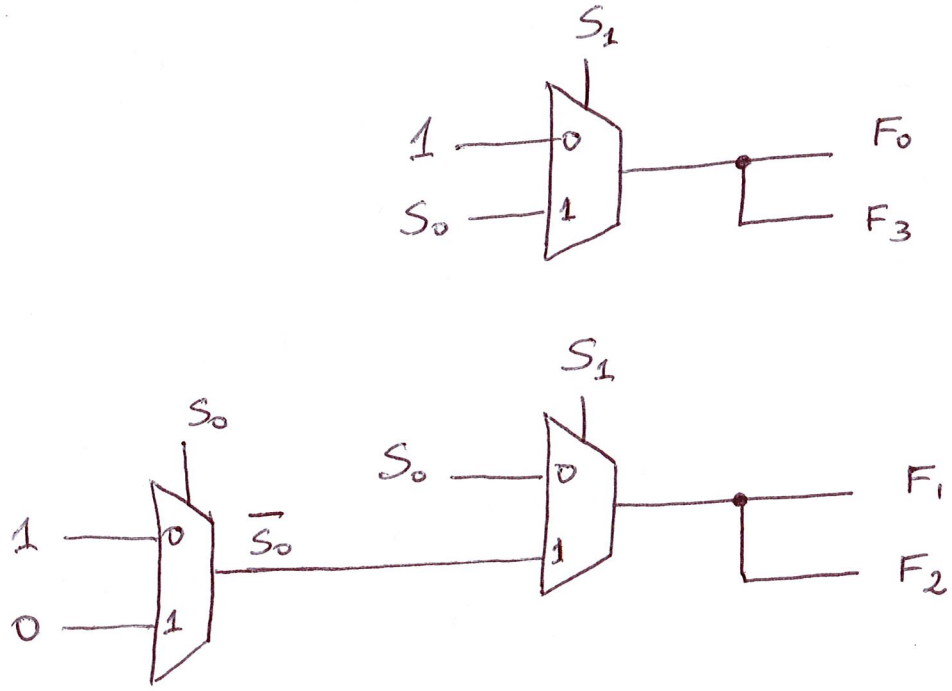
$F_3 = F_0 = \Sigma m(0, 1, 3)$

$F_2 = F_1 = (\overline{S_1}\ \&\ S_0)\ |\ (S_1\ \&\ \overline{S_0})$

a) Draw the truth table for this code converter, showing the 2 inputs and 4 outputs. (8p)

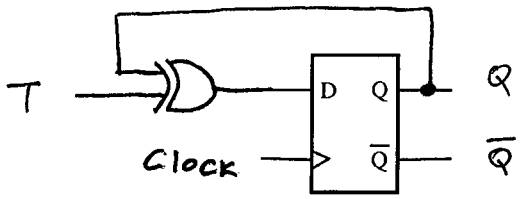
S_1	S_0	F_3	F_2	F_1	F_0
0	0	1	0	0	1
0	1	1	1	1	1
1	0	0	1	1	0
1	1	1	0	0	1

b) Implement this code converter using a <u>minimal</u> number of 2-to-1 multiplexers and <u>no other logic gates</u>. Assume that the input signals are available <u>only</u> in their non-inverted form, along with the constants 0 and 1. Label all inputs, outputs, and pins of your circuit. (7p)

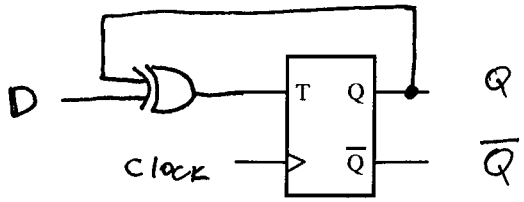


8. Alternative Implementation (5 x 2p each = 10p)
Complete the circuits below by drawing any additional logic gates, components, or wires to implement the specified flip-flop given another flop-flop type. Label all inputs and outputs.

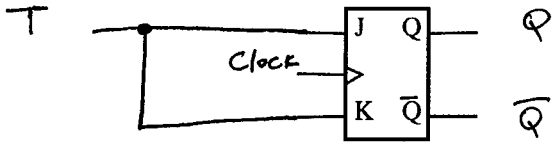
a) Implement a T Flip-Flop using a D Flip-Flop.



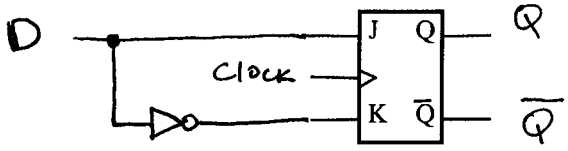
b) Implement a D Flip-Flop using a T Flip-Flop.



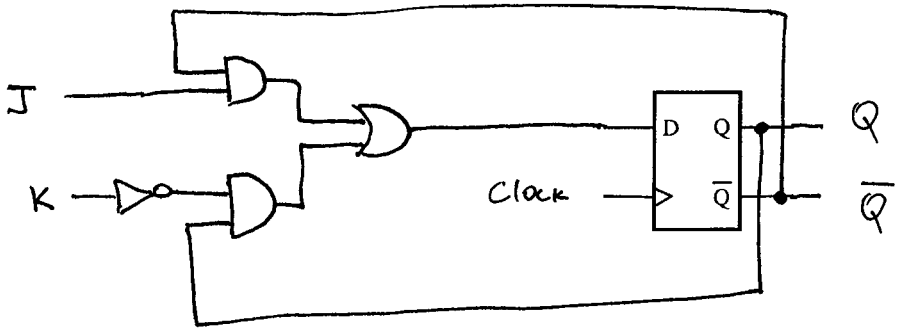
c) Implement a T Flip-Flop using a JK Flip-Flop.



d) Implement a D Flip-Flop using a JK Flip-Flop.

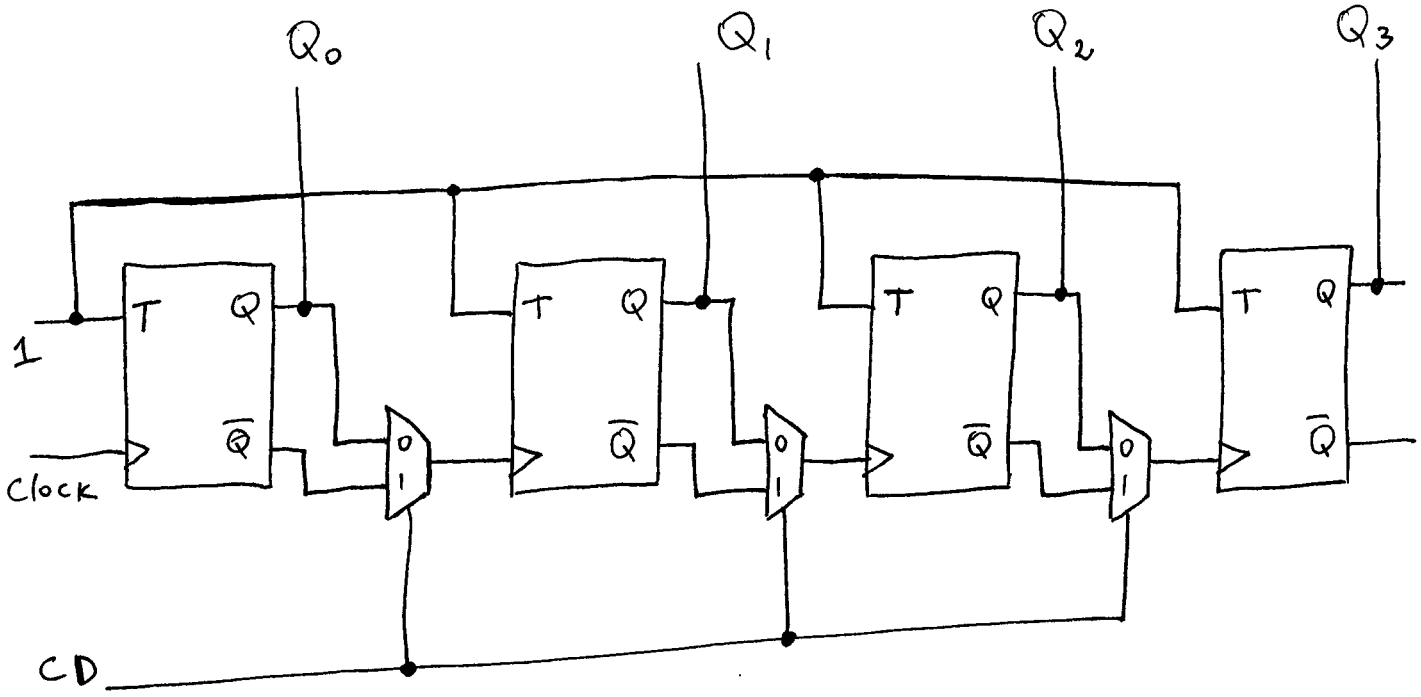


e) Implement a JK Flip-Flop using a D Flip-Flop.



9. Up and Down Counter (10p + 5p = 15p)

(a) Use four T Flip-Flops and any other logical gates or high-level components that are needed to implement a 4-bit <u>asynchronous</u> counter that can count either up or down. The counting direction is determined by one of the inputs to this circuit that is called CD. If this input is equal to 0 then the counter counts down. Alternatively, if CD = 1, then the counter counts up. Draw your circuit below. Clearly label all inputs, outputs, and pins.

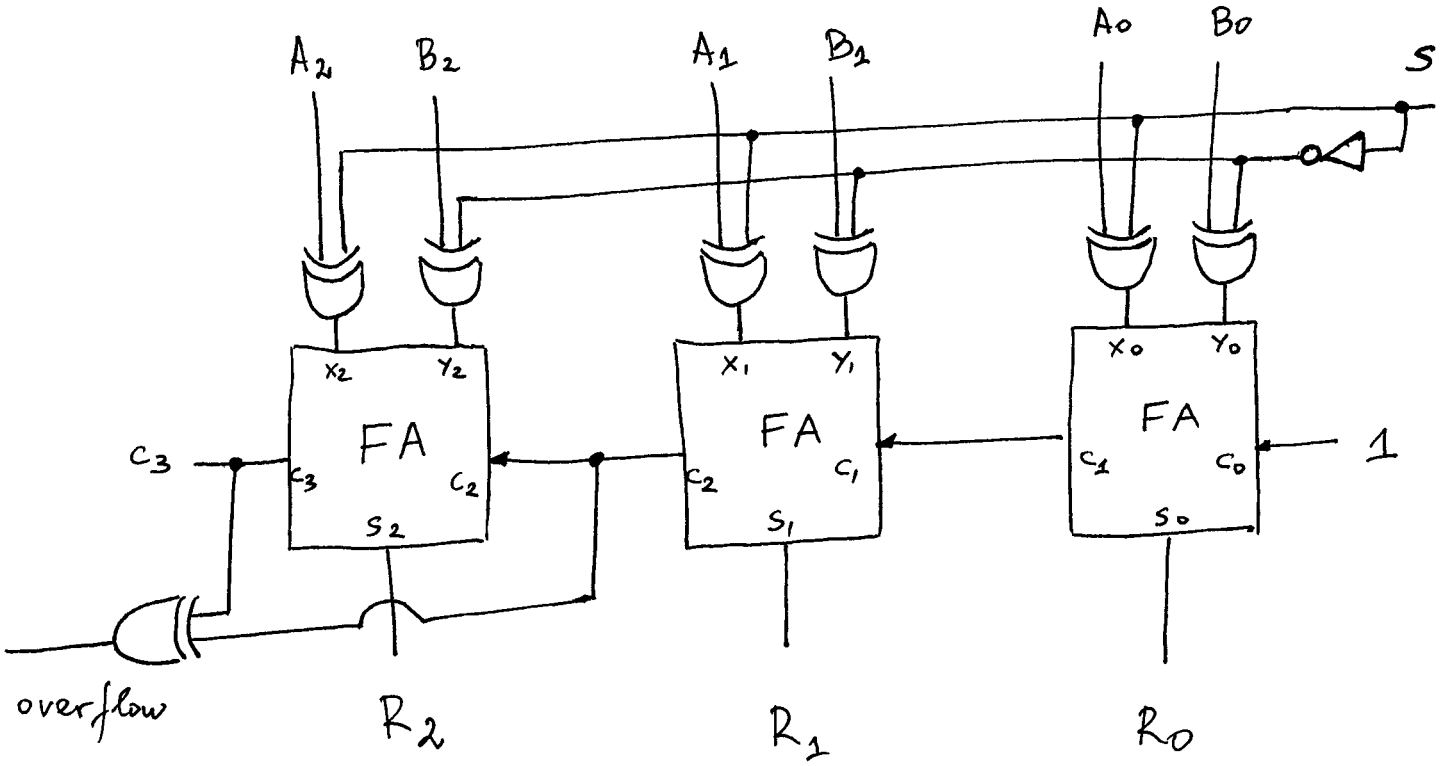


(b) Explain the correct solution in 3-4 sentences.

The asynchronous down counter uses the Q output of the previous flip-flop as the clock. But the asynchronous up counter uses the $\overline{Q}$ output. By adding a 2-to-1 multiplexer between the flip-flops we can select which of these signals is used as the clock depending on the value of CD. The T input of all flip-flops is set to 1.

10. Arithmetic Circuit (10p + 5p = 15p)

(a) Let $A=A_2\ A_1\ A_0$ and $B=B_2\ B_1\ B_0$ be two 3-bit binary numbers in 2's complement representation. You are given three full-adders, one NOT gate, and seven XOR gates. Your task is to design a circuit that can perform two different arithmetic operations: A-B and B-A. The operation is selected by one of the inputs to this circuit that is called S. When S=0 the 3-bit result $R= R_2\ R_1\ R_0$ is equal to A-B. Alternatively, when S=1 the result is B-A. The circuit must also detect if an overflow has occurred. Draw the wiring diagram for your circuit below. Clearly label all inputs, outputs, and pins.



(b) Explain the correct solution in 3-4 sentences.

A regular adder/subtractor circuit needs XORs on only one of the inputs. In this case XORs are used on both inputs. The control input S selects which set of XORs will act as NOT gates and which will act as repeaters. The carry C_0 input is set to 1 because this circuit always performs subtraction. The overflow detection is done with the last XOR gate.

Question	Max	Score
1. True/False	10	
2. Venn Diagram	5	
3. Even Numbers	15	
4. Basic Circuits	15	
5. Number Conversions	15	
6. Comparison Logic	15	
7. Code Converter	15	
8. Alternative Implementation	10	
9. Up and Down Counter	15	
10. Arithmetic Circuit	15	
TOTAL:	130	