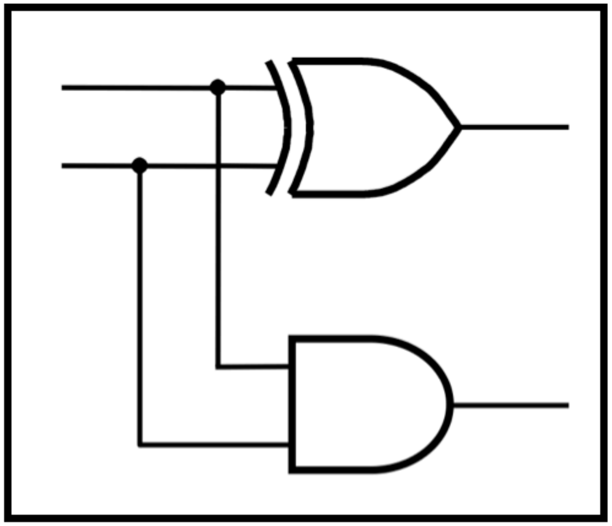


CprE 281: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Code Converters

CprE 281: Digital Logic
Iowa State University, Ames, IA

Administrative Stuff

- HW 7 is out

- It is due on Monday (Oct 12) @ 4pm

Quick Review

Decoders

2-to-4 Decoder (Definition)

- Has two inputs: w_1 and w_0

- Has four outputs: y_0 , y_1 , y_2 , and y_3

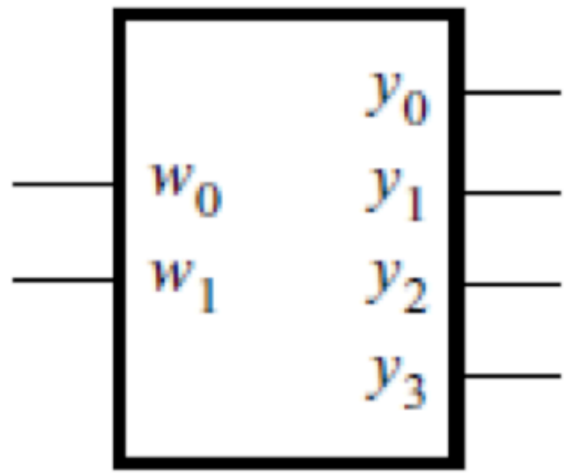
- If w_1=0 and w_0=0, then the output y_0 is set to 1
- If w_1=0 and w_0=1, then the output y_1 is set to 1
- If w_1=1 and w_0=0, then the output y_2 is set to 1
- If w_1=1 and w_0=1, then the output y_3 is set to 1

- Only one output is set to 1. All others are set to 0.

Truth Table and Graphical Symbol for a 2-to-4 Decoder

w_1	w_0	y_0	y_1	y_2	y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

(a) Truth table



(b) Graphical symbol

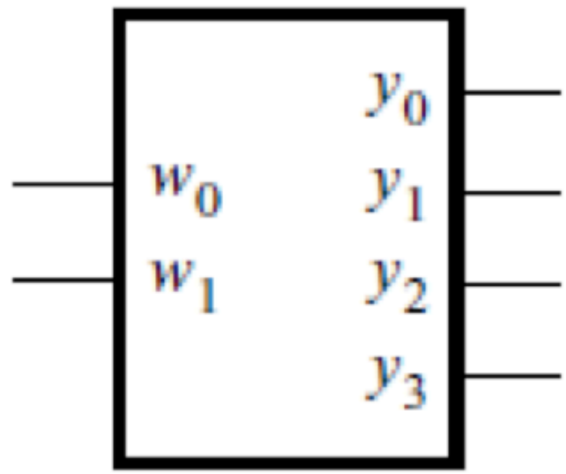
[Figure 4.13a-b from the textbook]

Truth Table and Graphical Symbol for a 2-to-4 Decoder

w_1	w_0	y_0	y_1	y_2	y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

The outputs are "one-hot" encoded

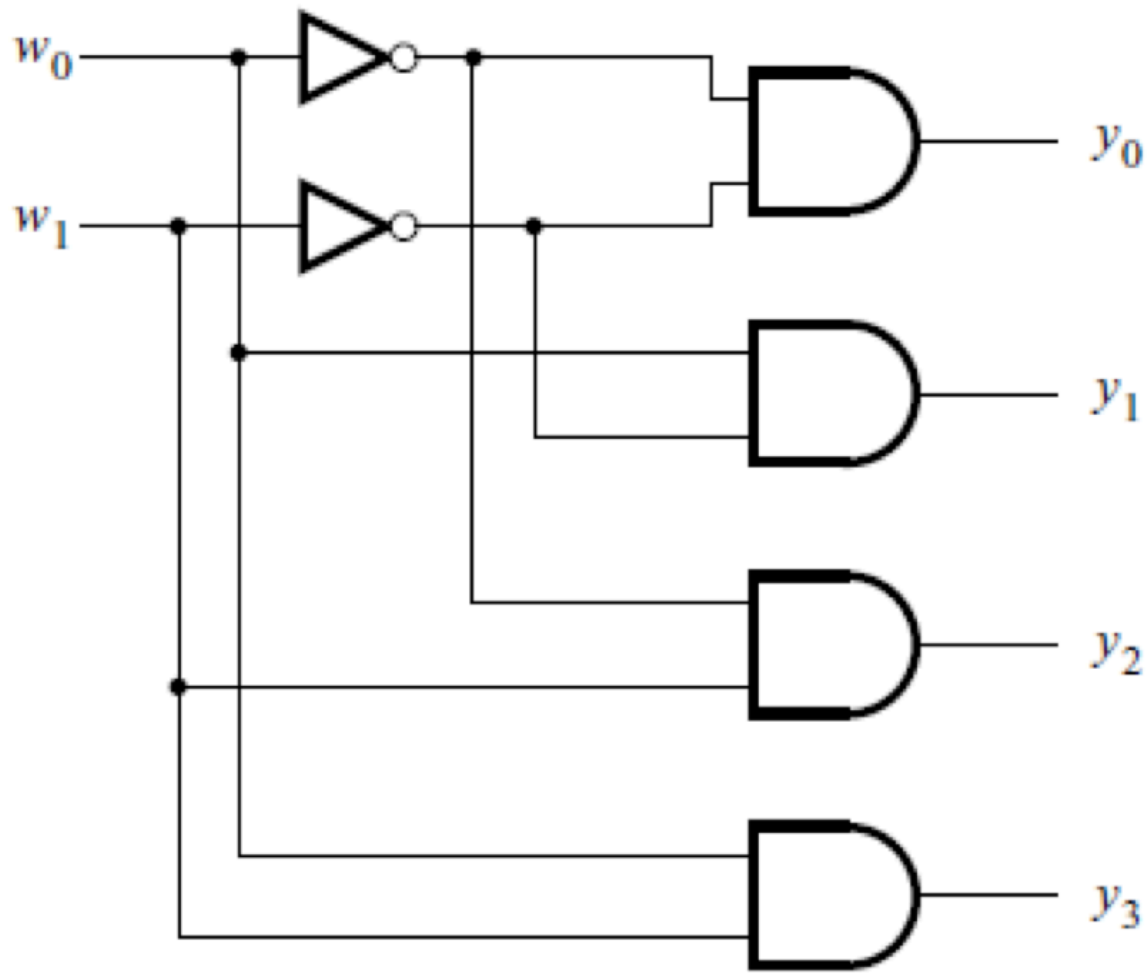
(a) Truth table



(b) Graphical symbol

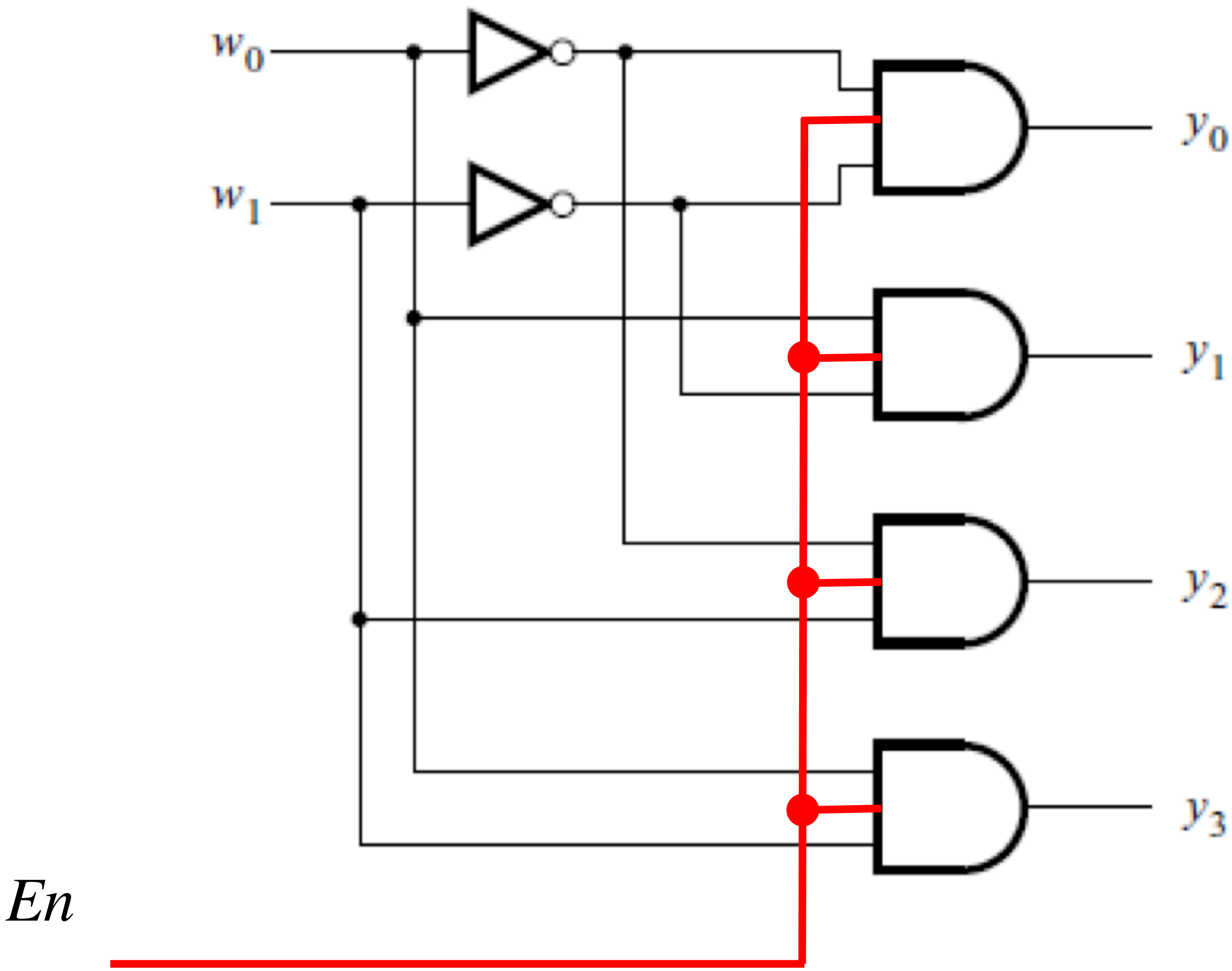
[Figure 4.13a-b from the textbook]

Truth Logic Circuit for a 2-to-4 Decoder



[Figure 4.13c from the textbook]

Adding an Enable Input

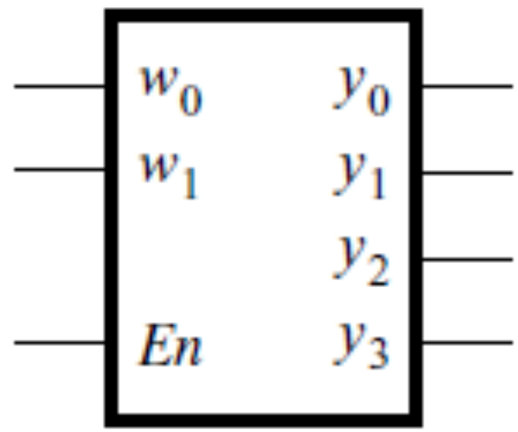


[Figure 4.13c from the textbook]

Truth Table and Graphical Symbol for a 2-to-4 Decoder with an Enable Input

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a) Truth table



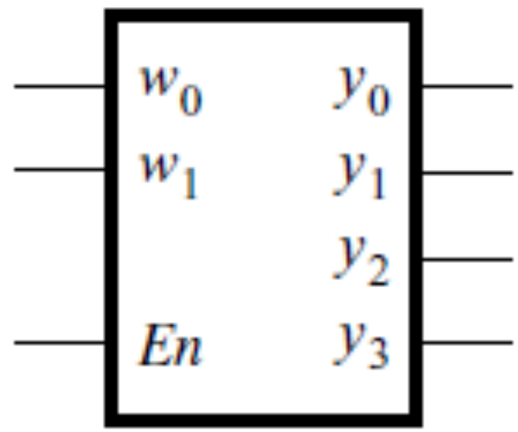
(b) Graphical symbol

[Figure 4.14a-b from the textbook]

Truth Table and Graphical Symbol for a 2-to-4 Decoder with an Enable Input

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a) Truth table

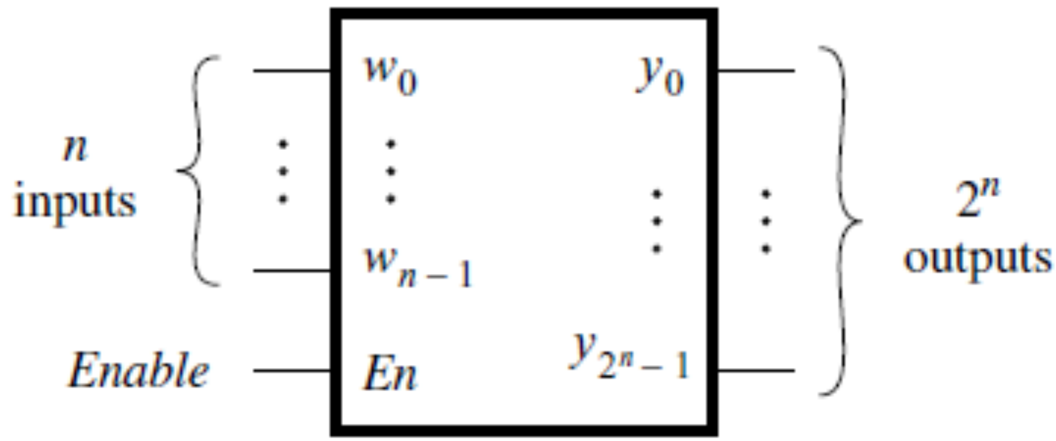


(b) Graphical symbol

x indicates that it does not matter what the value of these variable is for this row of the truth table

[Figure 4.14a-b from the textbook]

Graphical Symbol for a Binary n-to-2^n Decoder with an Enable Input



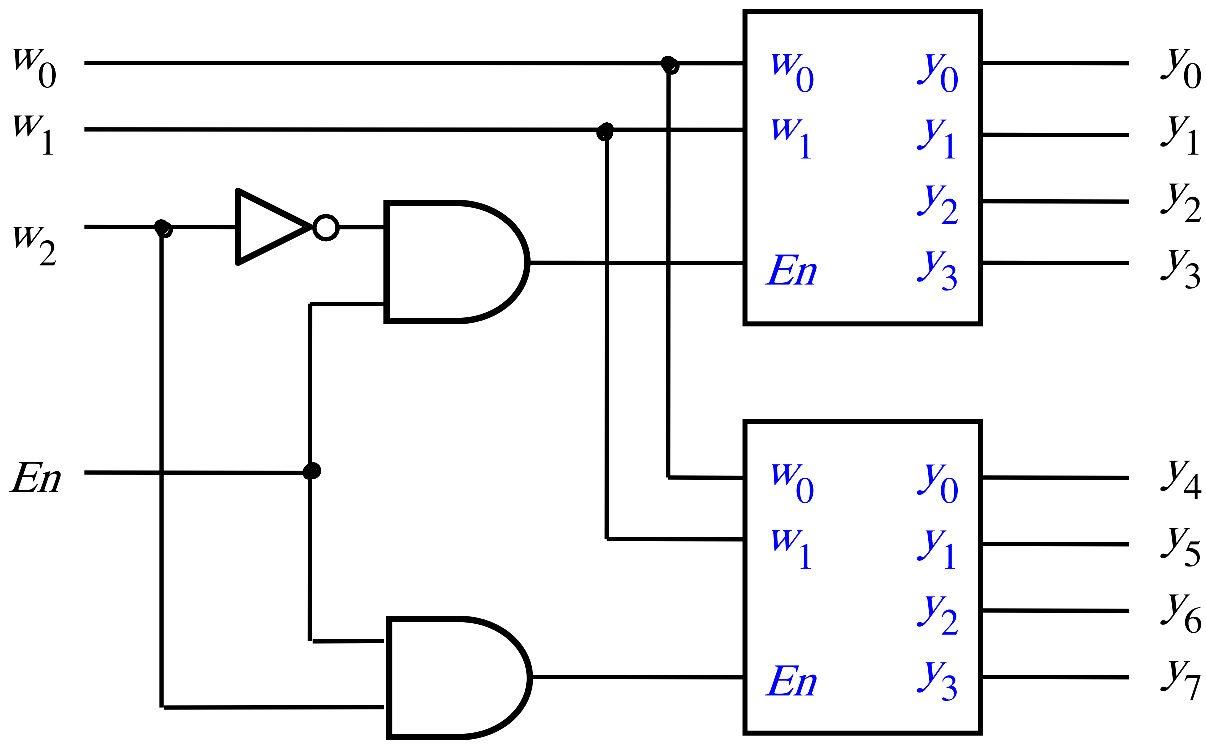
(d) An n-to-2^n decoder

A binary decoder with n inputs has 2^n outputs

The outputs of an enabled binary decoder are "one-hot" encoded, meaning that only a single bit is set to 1, i.e., it is *hot*.

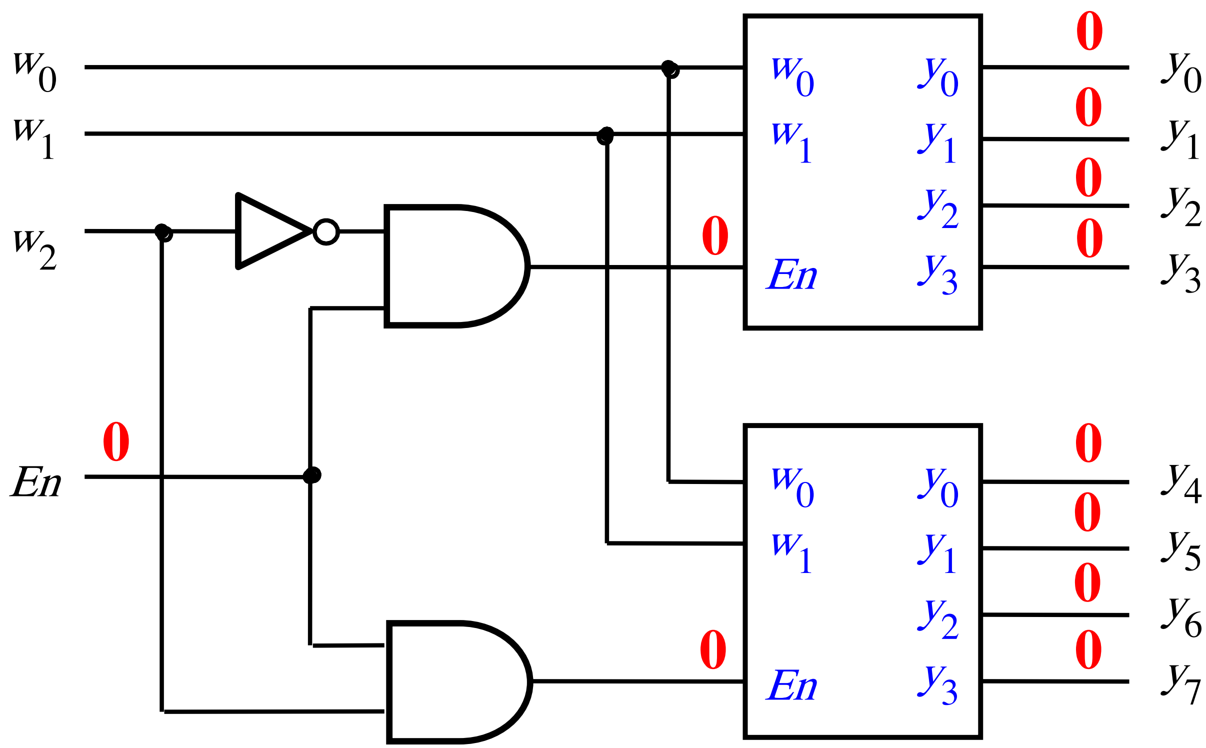
[Figure 4.14d from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



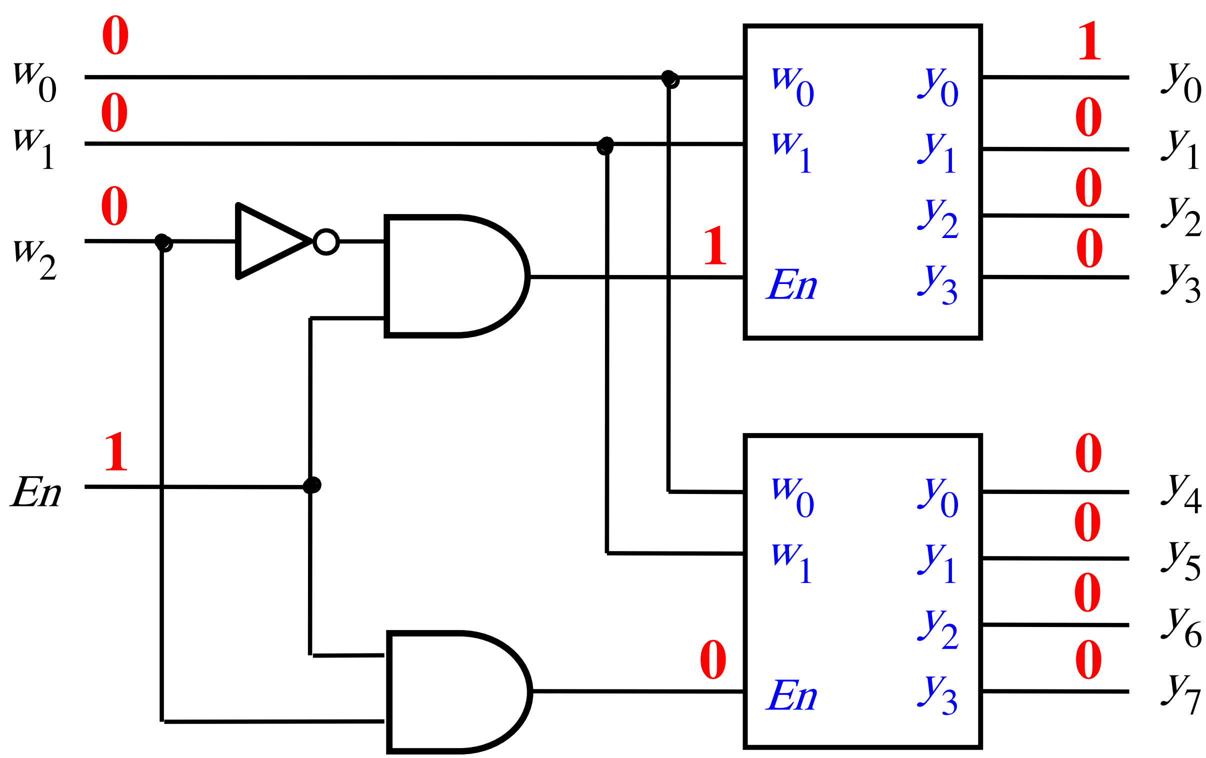
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



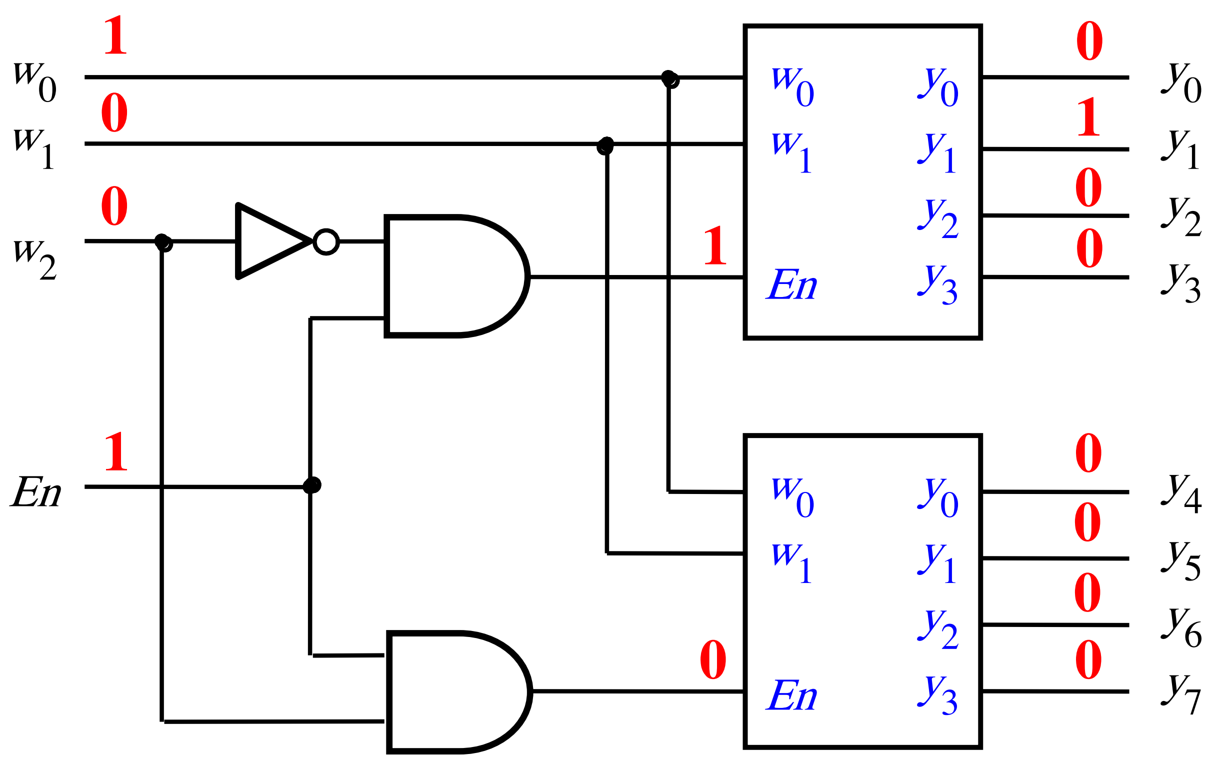
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



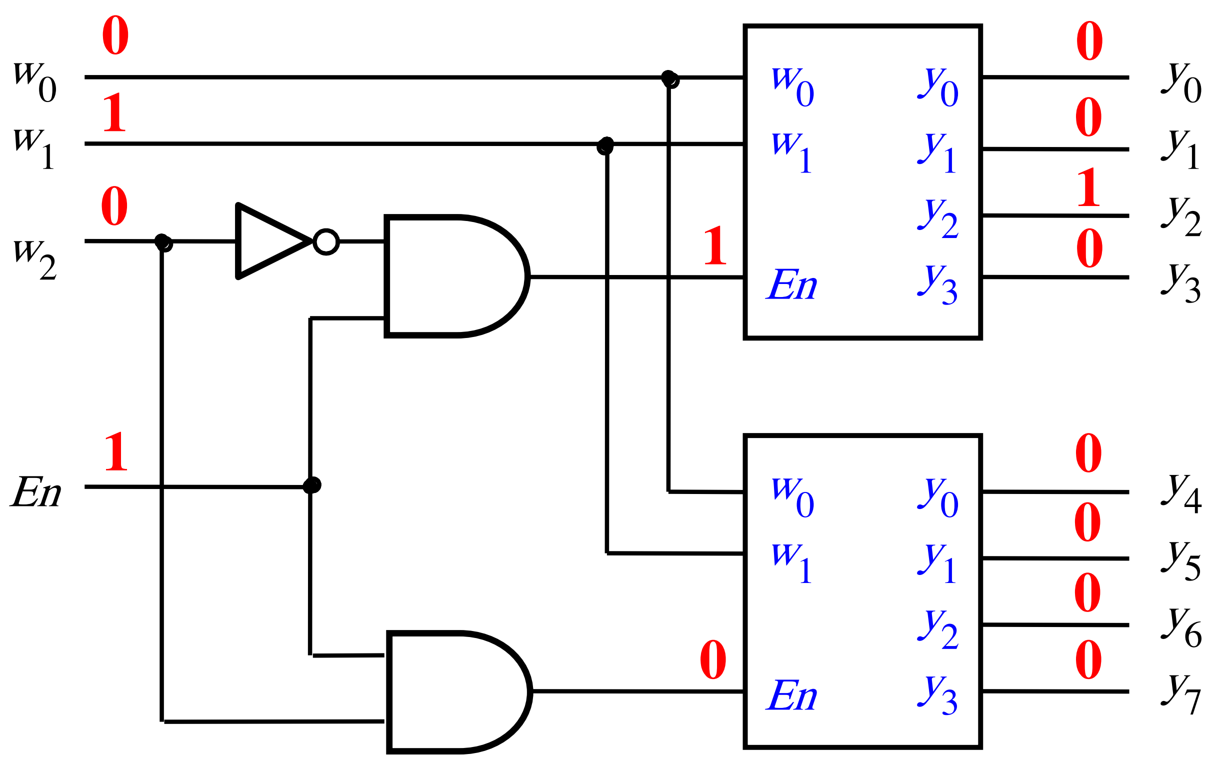
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



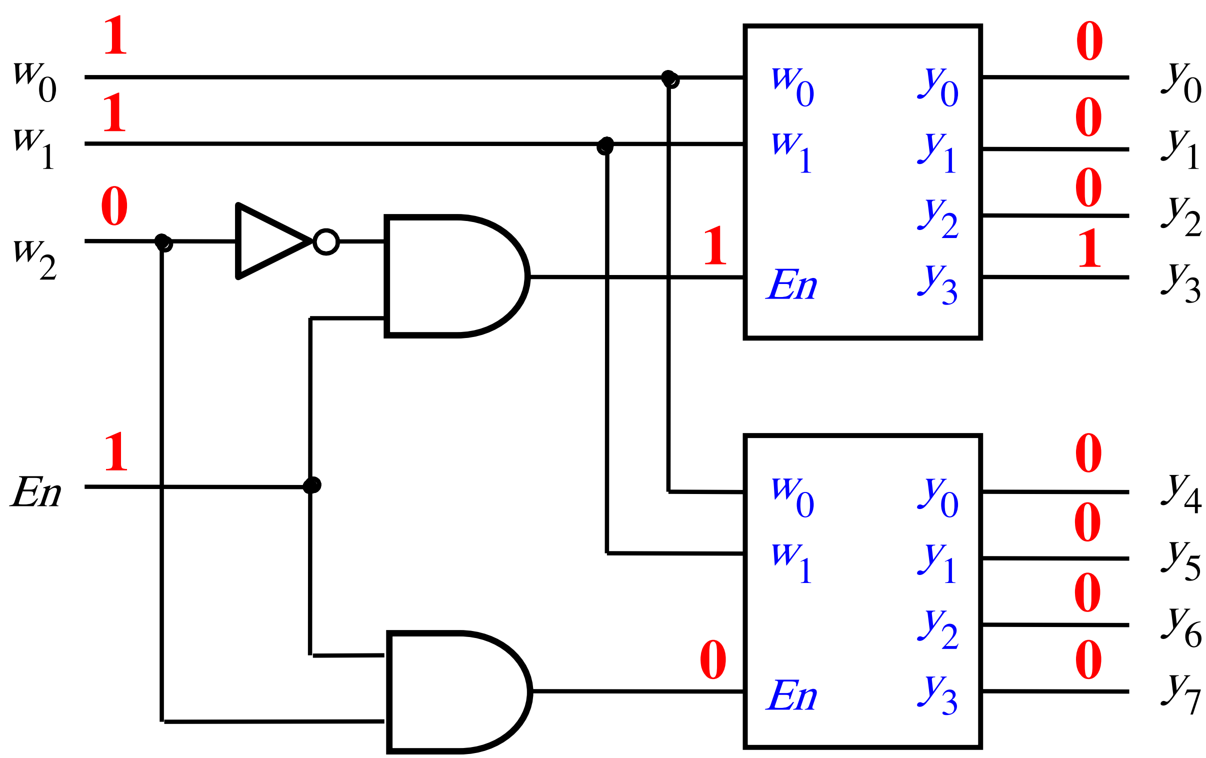
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



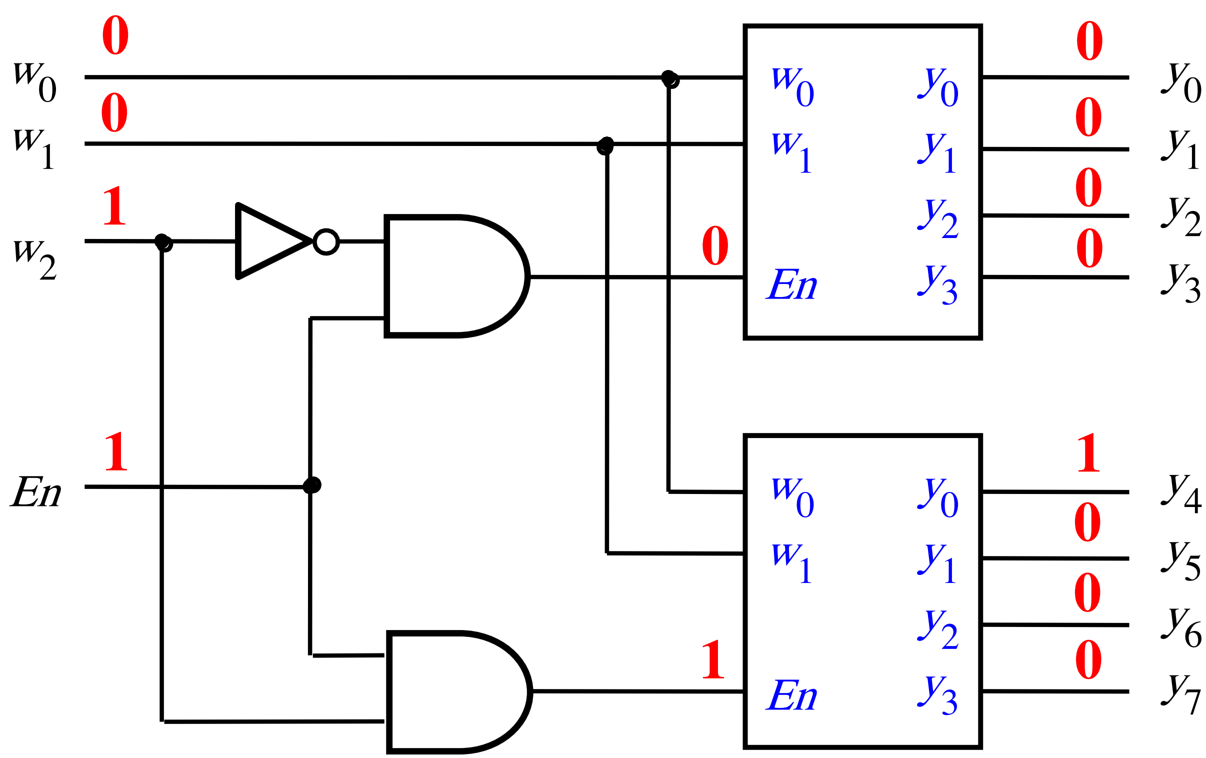
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



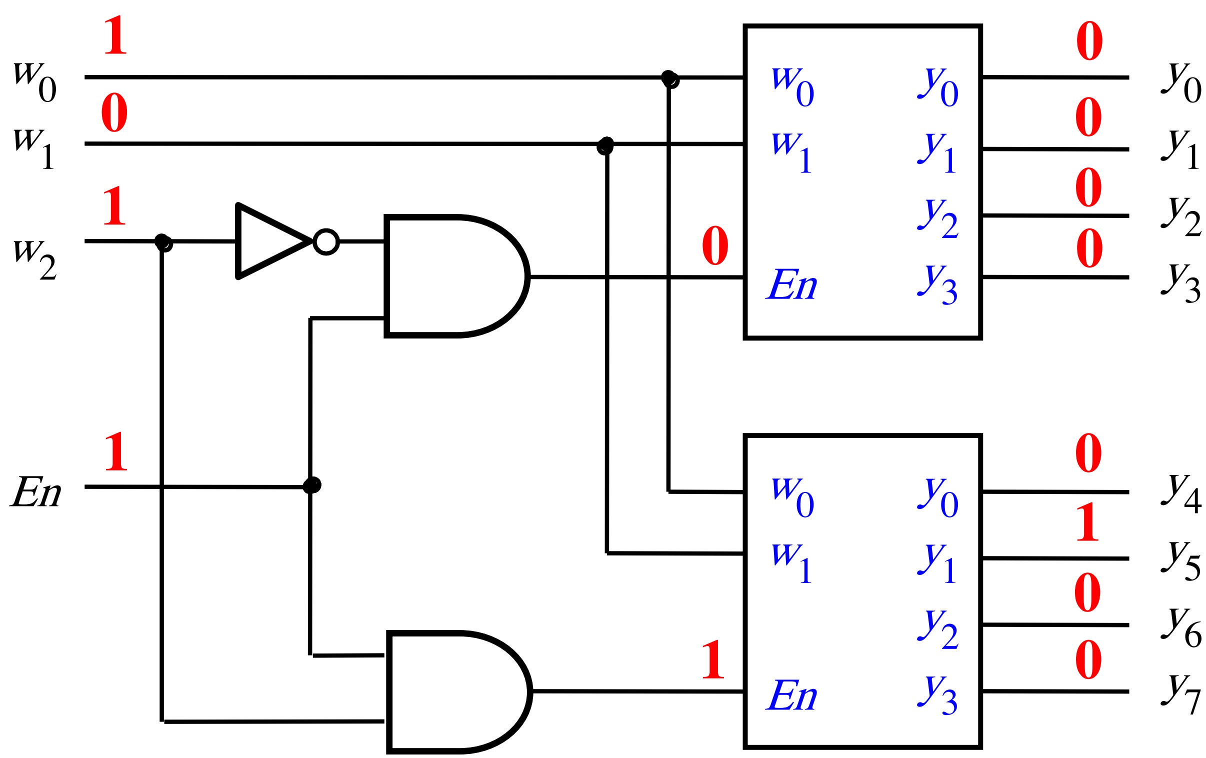
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



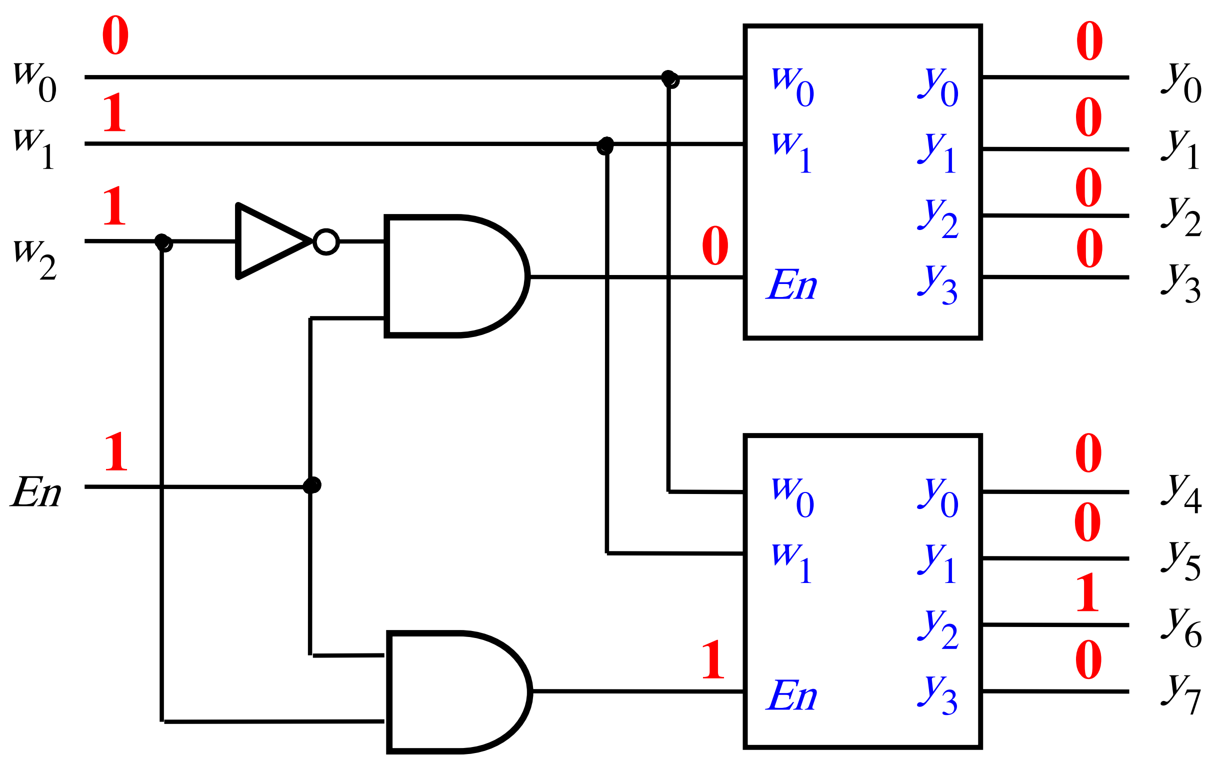
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



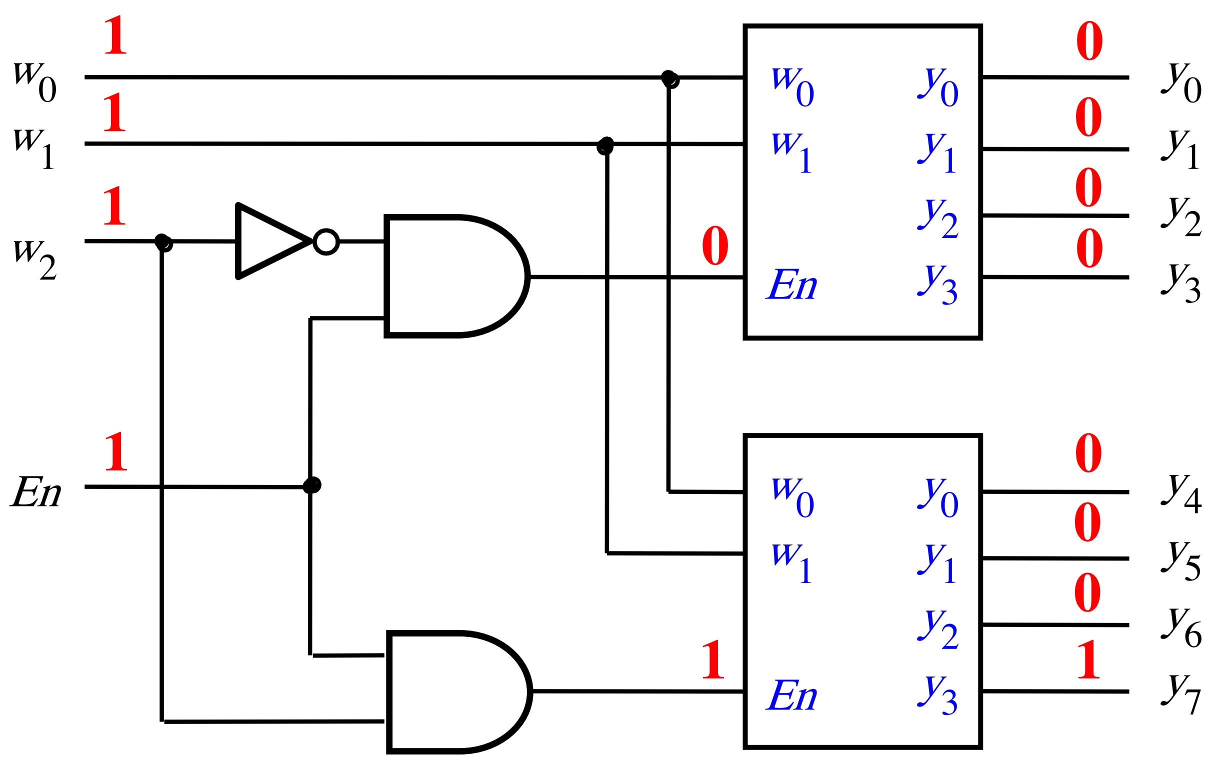
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



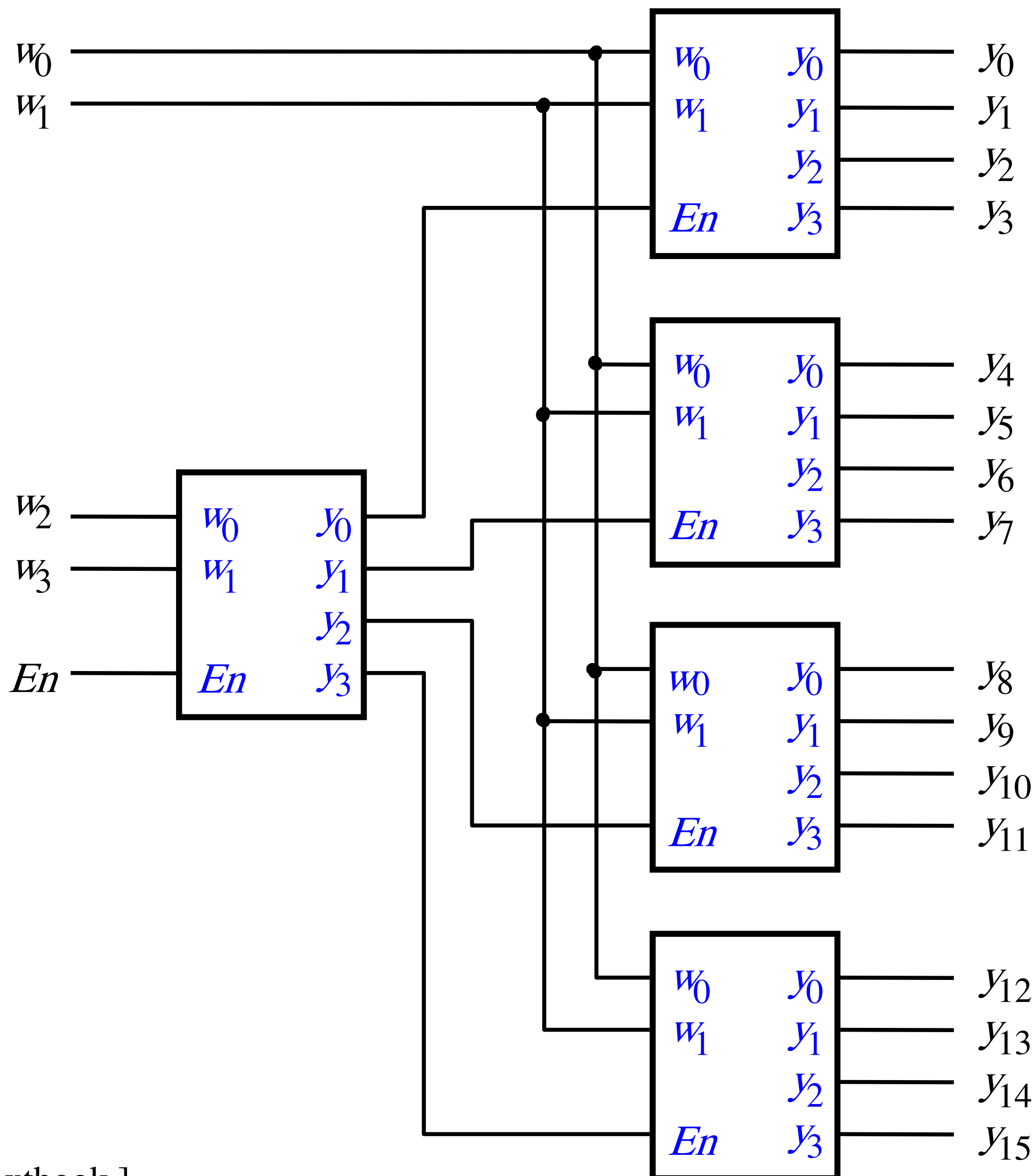
[Figure 4.15 from the textbook]

A 3-to-8 decoder using two 2-to-4 decoders



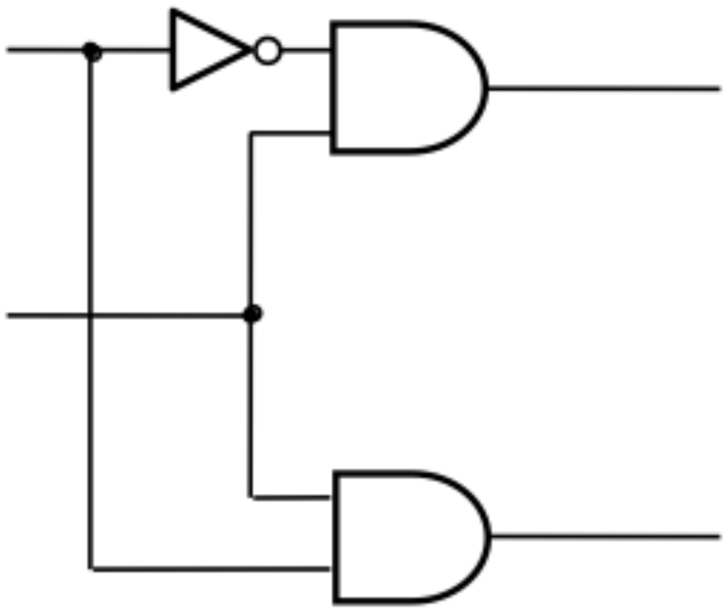
[Figure 4.15 from the textbook]

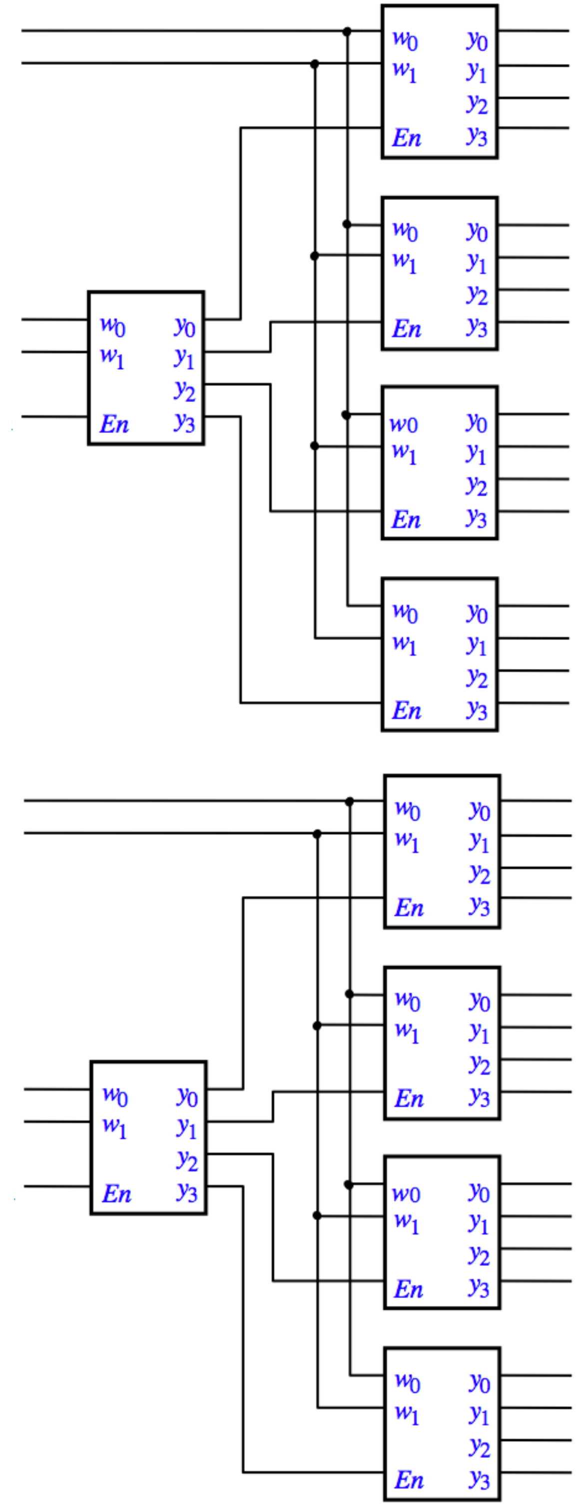
A 4-to-16 decoder built using a decoder tree



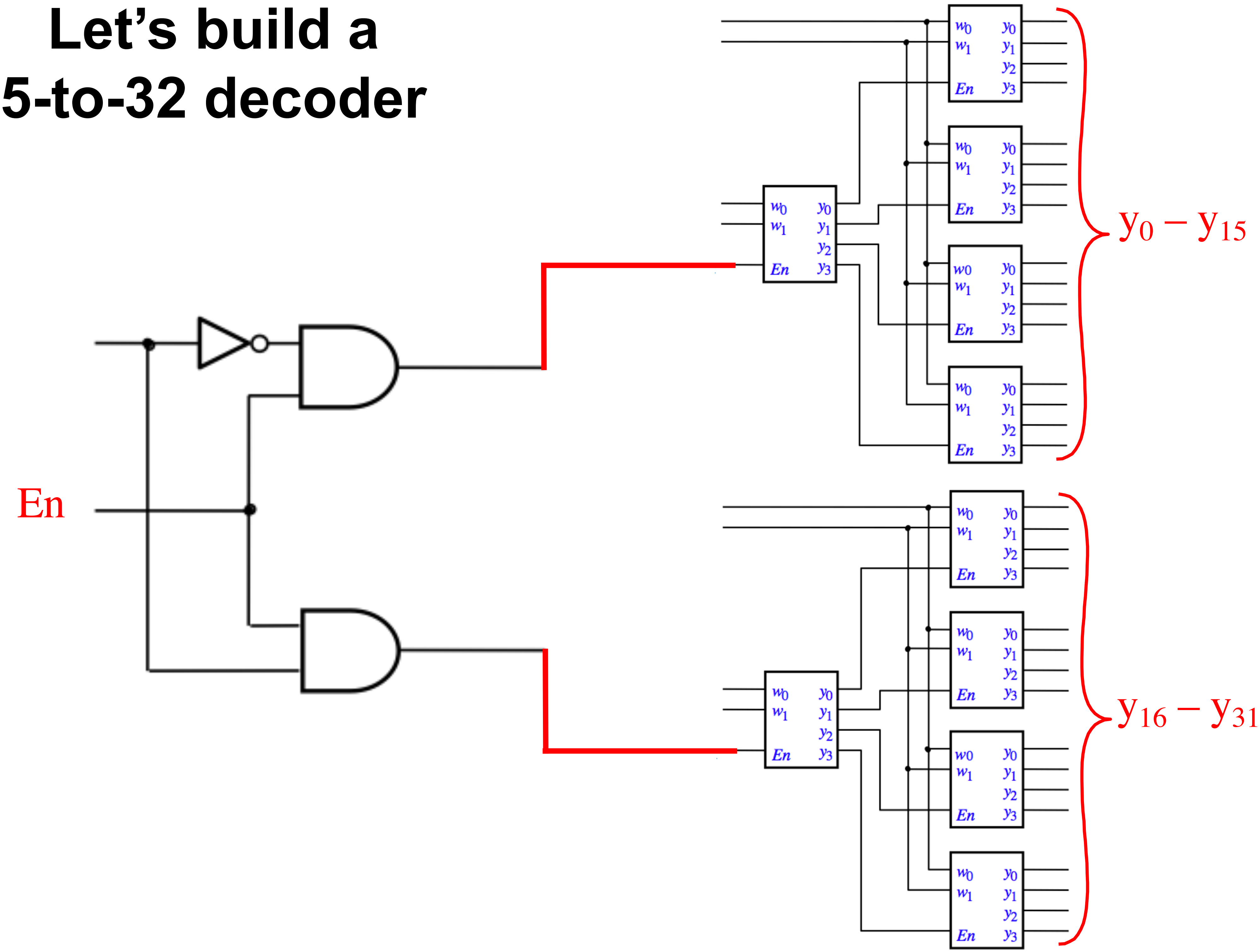
[Figure 4.16 from the textbook]

Let's build a 5-to-32 decoder

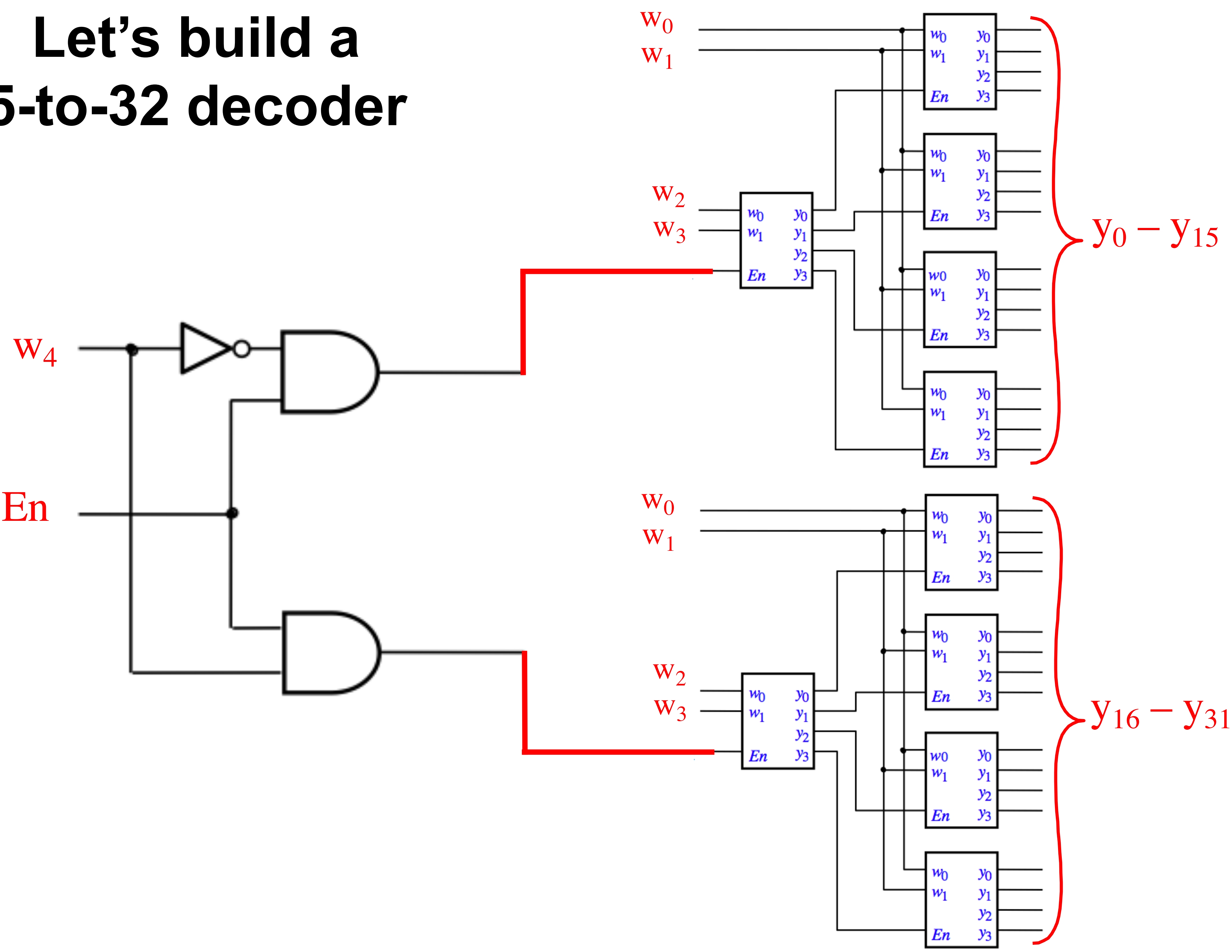




Let's build a 5-to-32 decoder



Let's build a 5-to-32 decoder

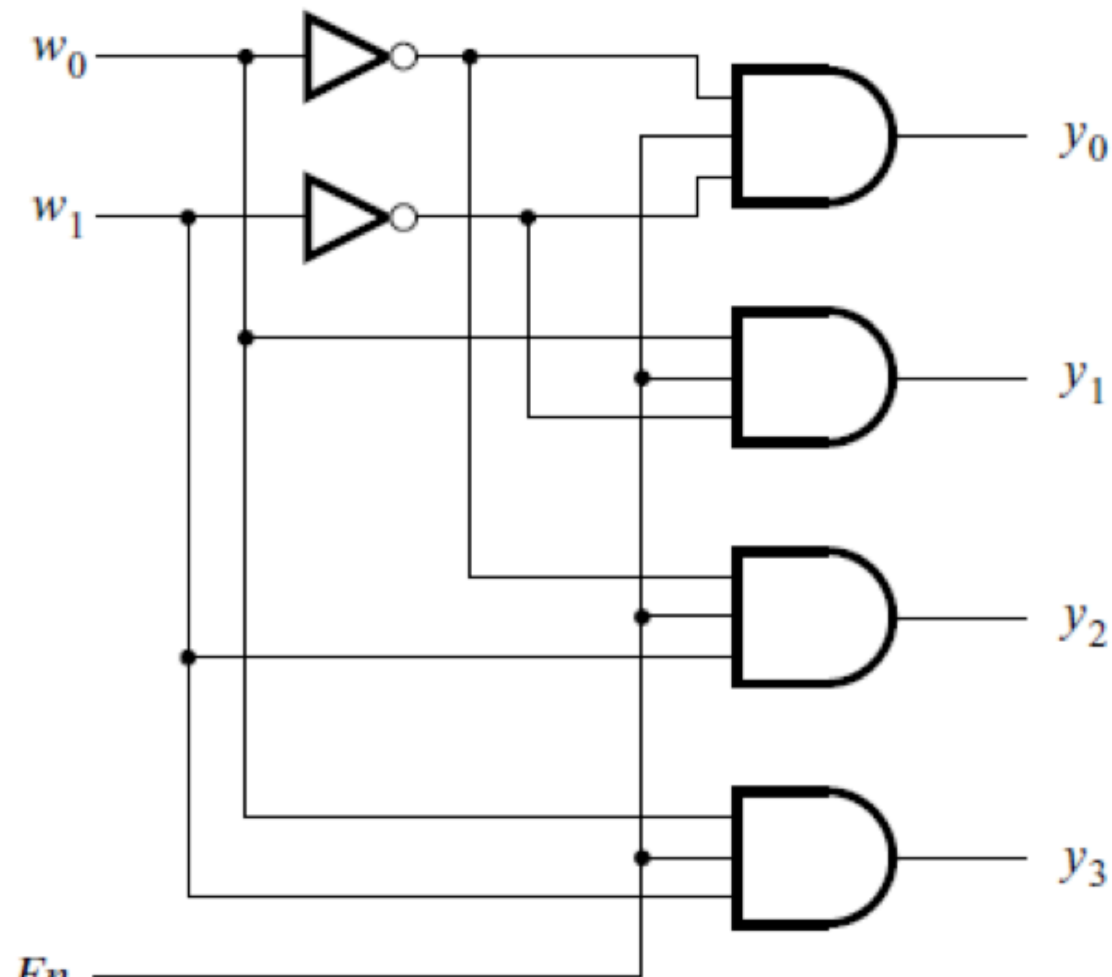


Demultiplexers

1-to-4 Demultiplexer (Definition)

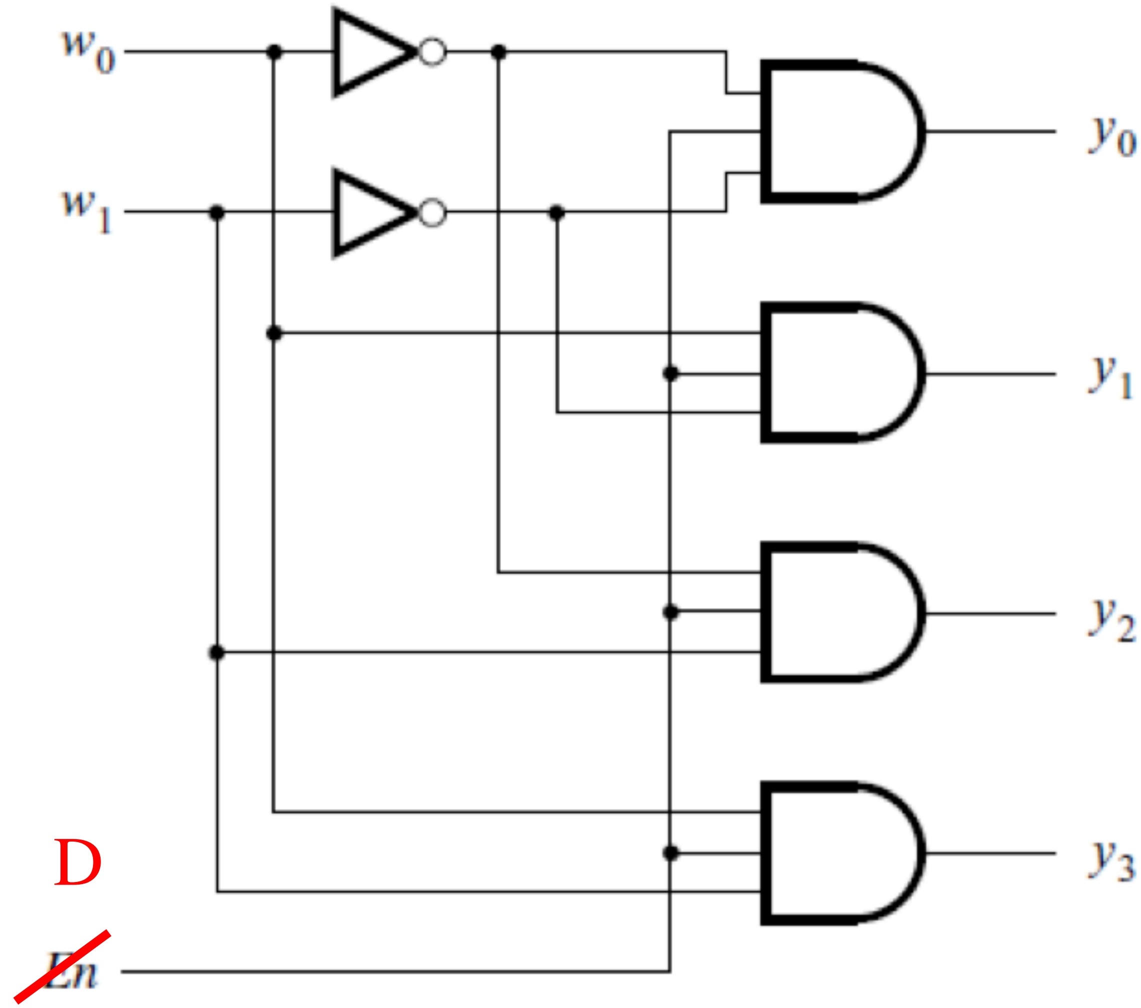
- Has one data input line: D
- Has two output select lines: w_1 and w_0
- Has four outputs: y_0 , y_1 , y_2 , and y_3
- If w_1=0 and w_0=0, then the output y_0 is set to D
- If w_1=0 and w_0=1, then the output y_1 is set to D
- If w_1=1 and w_0=0, then the output y_2 is set to D
- If w_1=1 and w_0=1, then the output y_3 is set to D
- Only one output is set to D. All others are set to 0.

A 1-to-4 demultiplexer built with a 2-to-4 decoder



[Figure 4.14c from the textbook]

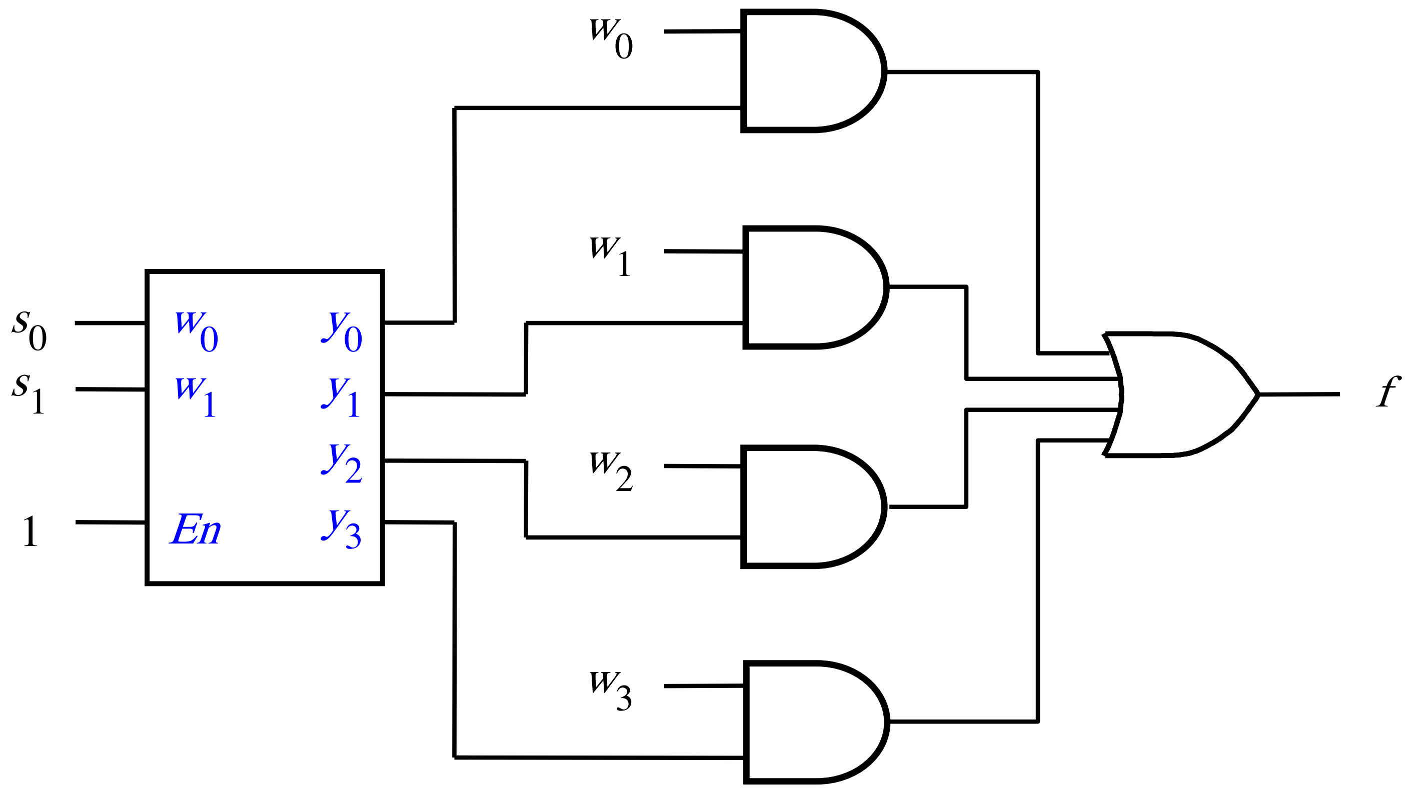
A 1-to-4 demultiplexer built with a 2-to-4 decoder



[Figure 4.14c from the textbook]

Multiplexers
(Implemented with Decoders)

A 4-to-1 multiplexer built using a 2-to-4 decoder



[Figure 4.17 from the textbook]

Encoders

Binary Encoders

4-to-2 Binary Encoder (Definition)

- Has four inputs: w_3 , w_2 , w_1 , and w_0
- Has two outputs: y_1 and y_0
- Only one input is set to 1 (“one-hot” encoded). All others are set to 0.

- If w_0=1 then y_1=0 and y_0=0
- If w_1=1 then y_1=0 and y_0=1
- If w_2=1 then y_1=1 and y_0=0
- If w_3=1 then y_1=1 and y_0=1

Truth table for a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

[Figure 4.19 from the textbook]

Truth table for a 4-to-2 binary encoder

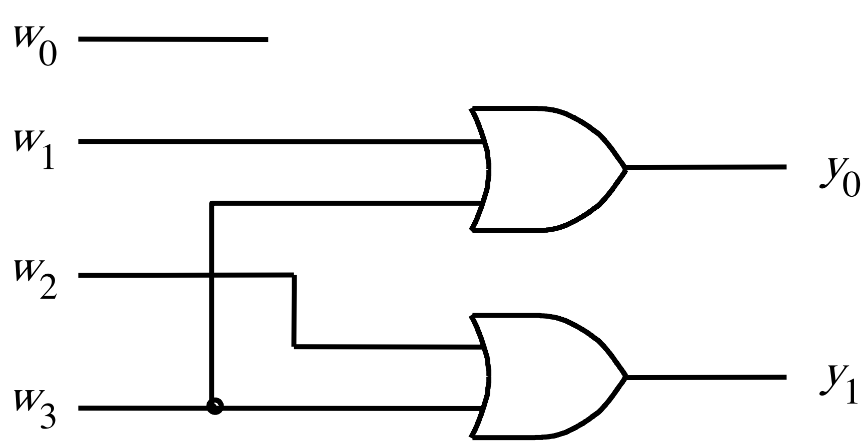
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

The inputs are “one-hot” encoded

[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

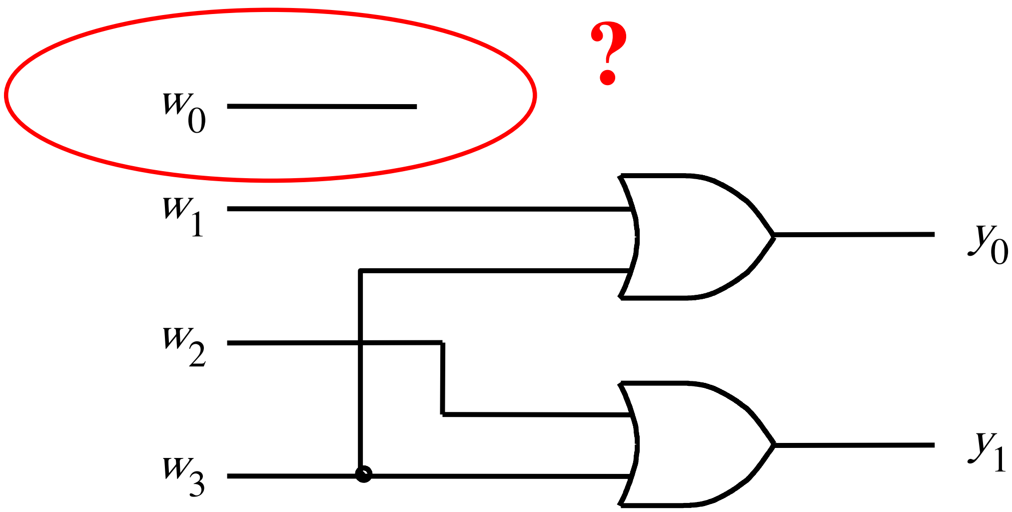
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

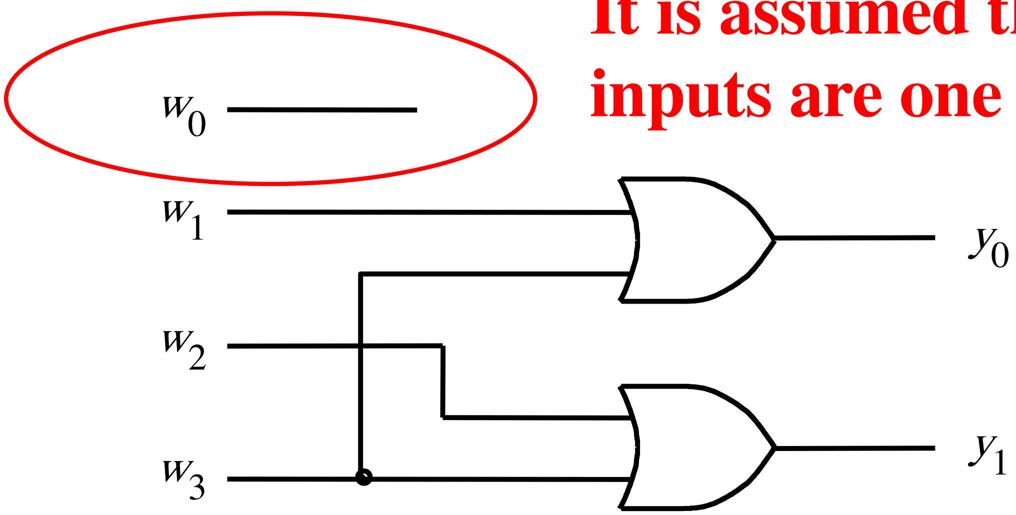


[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

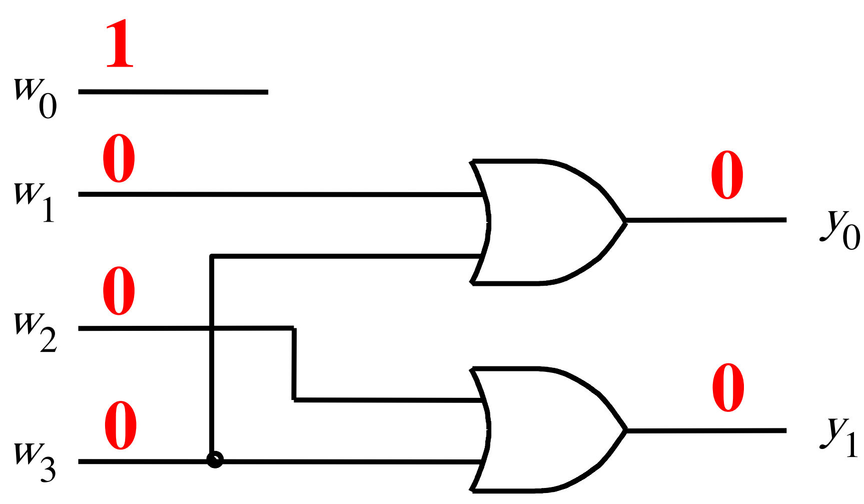
It is assumed that the inputs are one hot encoded



[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

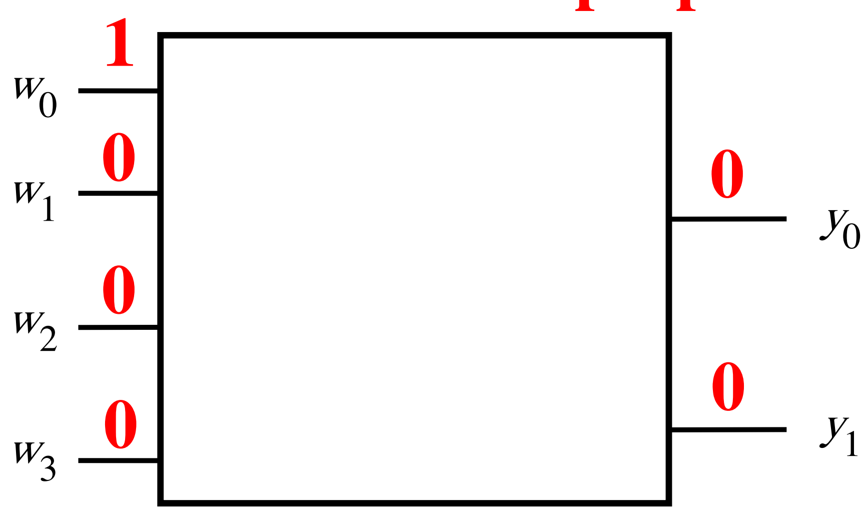


[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

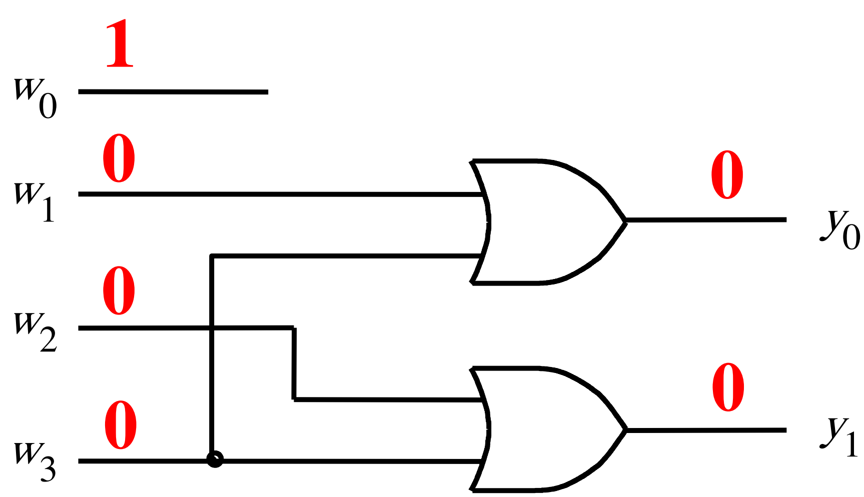
As this level of abstraction we need that w_0 input for this to be a proper 4-to-2 binary encoder.



[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

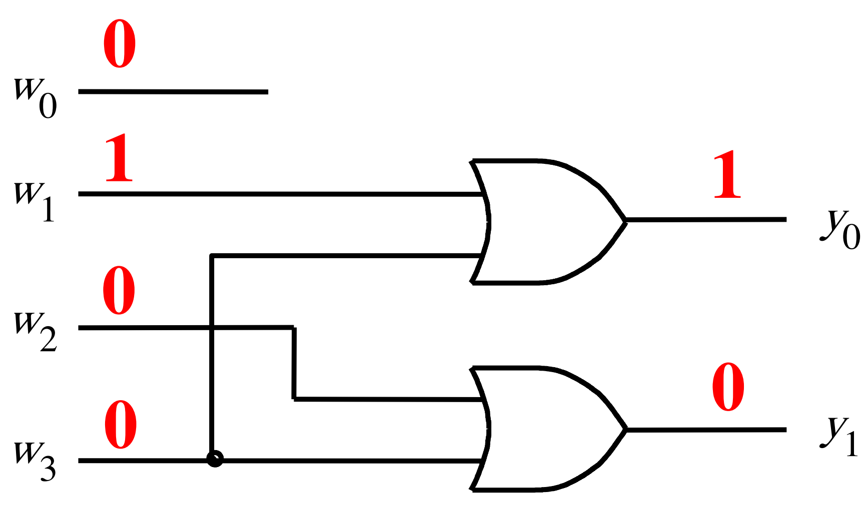
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

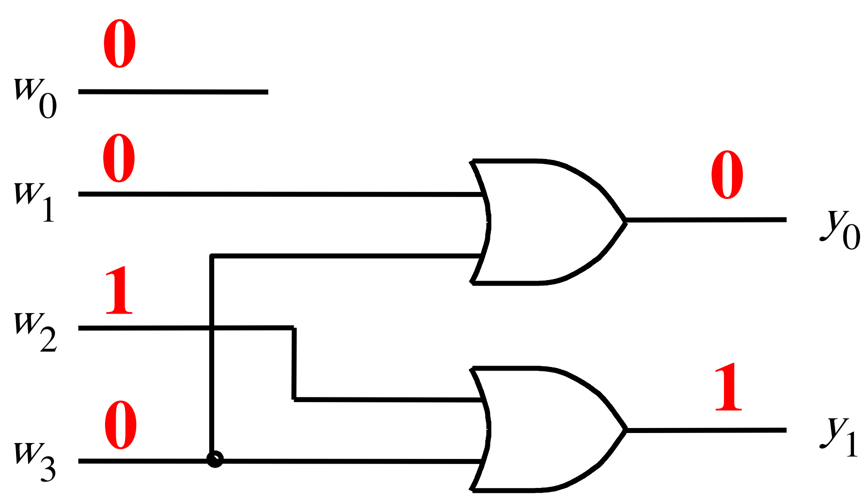
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

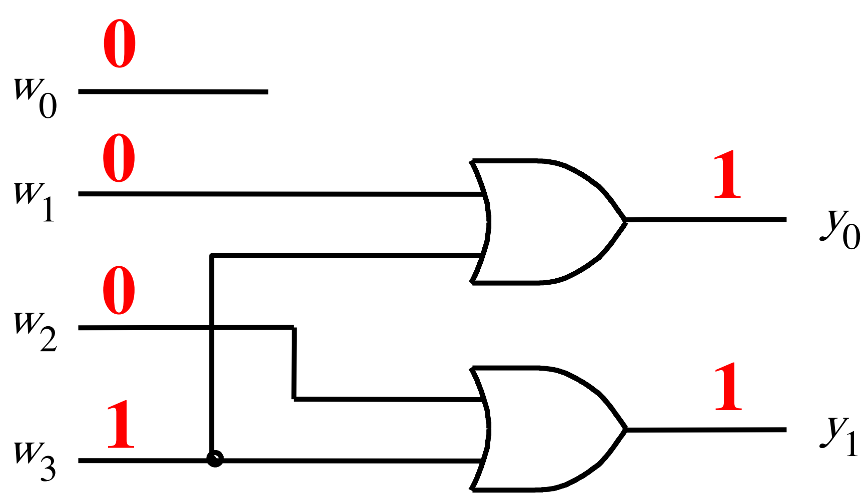
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



[Figure 4.19 from the textbook]

Circuit for a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



[Figure 4.19 from the textbook]

Expressions for 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	0		
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1		
0	1	0	0	1	0
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	1	1
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Expressions for 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	0	d	d
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	d	d
0	1	0	0	1	0
0	1	0	1	d	d
0	1	1	0	d	d
0	1	1	1	d	d
1	0	0	0	1	1
1	0	0	1	d	d
1	0	1	0	d	d
1	0	1	1	d	d
1	1	0	0	d	d
1	1	0	1	d	d
1	1	1	0	d	d
1	1	1	1	d	d

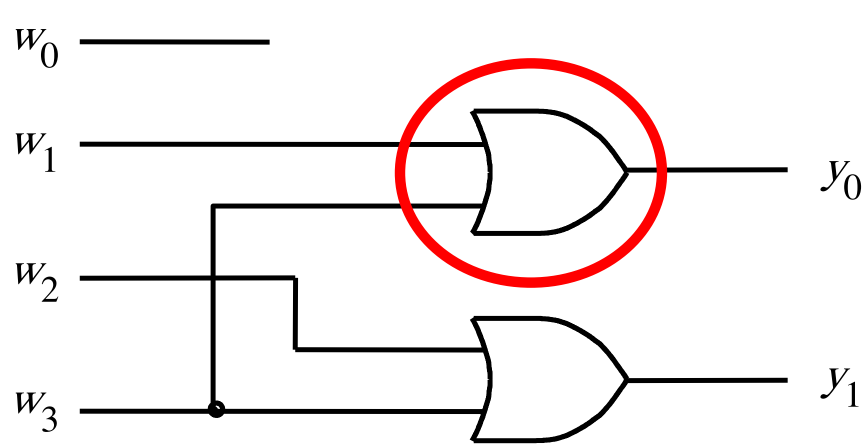
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Expressions for 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	0	d	d
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	d	d
0	1	0	0	1	0
0	1	0	1	d	d
0	1	1	0	d	d
0	1	1	1	d	d
1	0	0	0	1	1
1	0	0	1	d	d
1	0	1	0	d	d
1	0	1	1	d	d
1	1	0	0	d	d
1	1	0	1	d	d
1	1	1	0	d	d
1	1	1	1	d	d

$w_1 w_0$ \ $w_3 w_2$	00	01	11	10
00	d	0	d	1
01	0	d	d	d
11	d	d	d	d
10	1	d	d	d

$$y_0 = (w_1 + w_3)$$

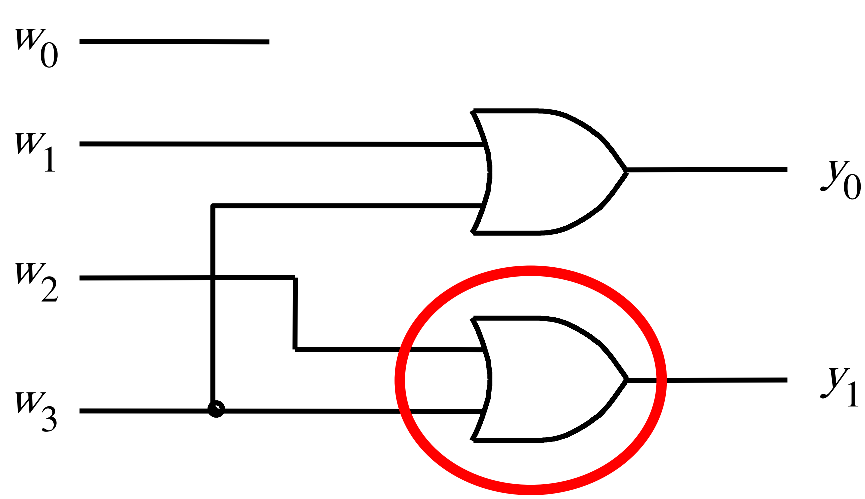


Expressions for 4-to-2 binary encoder

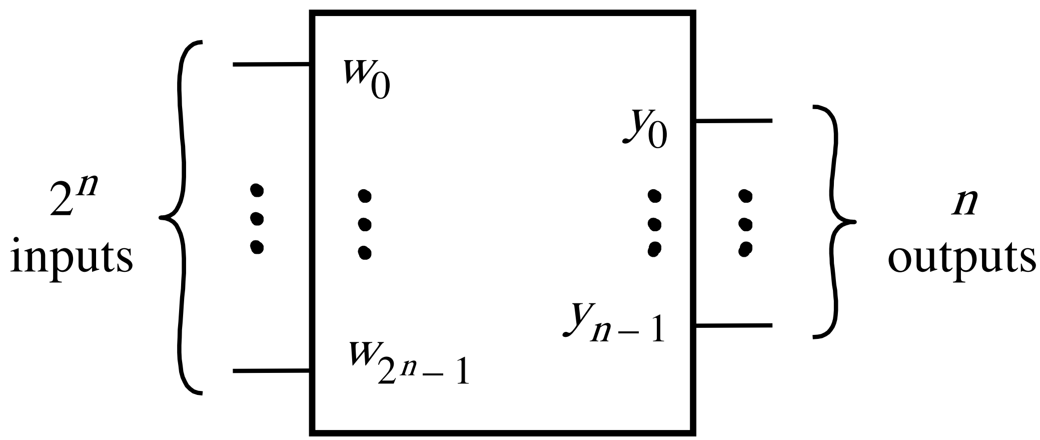
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	0	d	d
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	d	d
0	1	0	0	1	0
0	1	0	1	d	d
0	1	1	0	d	d
0	1	1	1	d	d
1	0	0	0	1	1
1	0	0	1	d	d
1	0	1	0	d	d
1	0	1	1	d	d
1	1	0	0	d	d
1	1	0	1	d	d
1	1	1	0	d	d
1	1	1	1	d	d

$w_1 w_0$ \ $w_3 w_2$	00	01	11	10
00	d	1	d	1
01	0	d	d	d
11	d	d	d	d
10	0	d	d	d

$$y_1 = (w_3 + w_2)$$



A 2^n-to-n binary encoder



[Figure 4.18 from the textbook]

Priority Encoders

Truth table for a 4-to-2 priority encoder (abbreviated version)

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

[Figure 4.20 from the textbook]

Truth table for a 4-to-2 priority encoder (abbreviated version)

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

[Figure 4.20 from the textbook]

Truth table for a 4-to-2 priority encoder

	w_3	w_2	w_1	w_0	y_1	y_0	z
0 0 0 0	0	0	0	0	d	d	0
0 0 0 1	0	0	0	1	0	0	1
0 0 1 x	0	0	1	0	0	1	1
	0	0	1	1	0	1	1
0 1 x x	0	1	0	0	1	0	1
	0	1	0	1	1	0	1
	0	1	1	0	1	0	1
	0	1	1	1	1	0	1
1 x x x	1	0	0	0	1	1	1
	1	0	0	1	1	1	1
	1	0	1	0	1	1	1
	1	0	1	1	1	1	1
	1	1	0	0	1	1	1
	1	1	0	1	1	1	1
	1	1	1	0	1	1	1
	1	1	1	1	1	1	1

Expressions for 4-to-2 priority encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

$w_1 w_0$ \ $w_3 w_2$	00	01	11	10
00	d	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

$$y_1 = w_3 + w_2$$

Expressions for 4-to-2 priority encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

$w_1 w_0$ \ $w_3 w_2$	00	01	11	10
00	d	0	1	1
01	0	0	1	1
11	1	0	1	1
10	1	0	1	1

$$y_0 = w_3 + w_1 \overline{w_2}$$

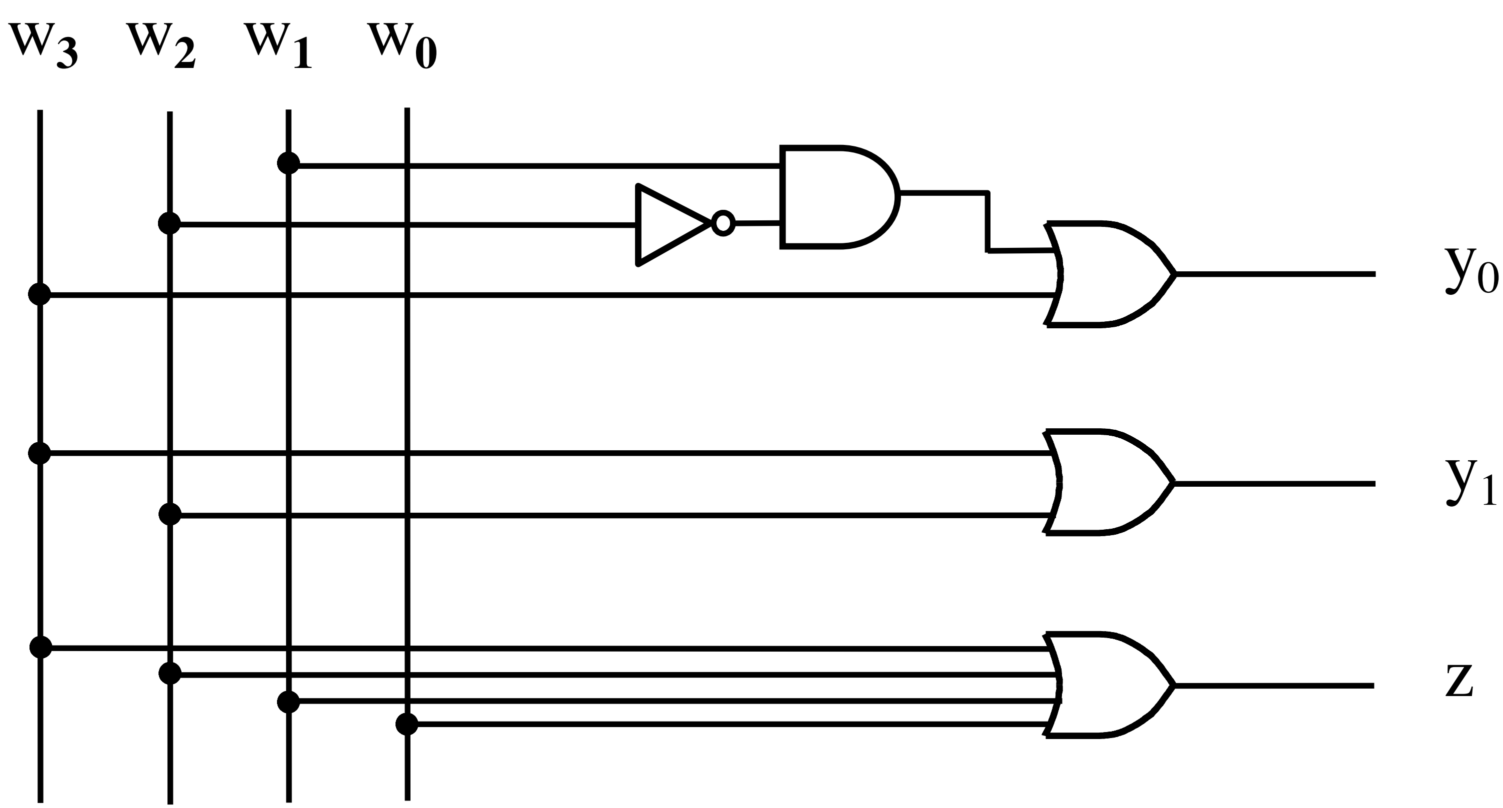
Expressions for 4-to-2 priority encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

$w_1 w_0$ \ $w_3 w_2$	00	01	11	10
00	$\boxed{0}$	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$$Z = w_3 + w_2 + w_1 + w_0$$

Circuit for the 4-to-2 priority encoder



The textbook derives a different circuit for the 4-to-2 priority encoder using a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$$i_0 = \overline{w}_3\overline{w}_2\overline{w}_1 w_0$$
$$i_1 = \overline{w}_3\overline{w}_2 w_1$$
$$i_2 = \overline{w}_3 w_2$$
$$i_3 = w_3$$

$$y_0 = i_1 + i_3$$
$$y_1 = i_2 + i_3$$

$$z = i_0 + i_1 + i_2 + i_3$$

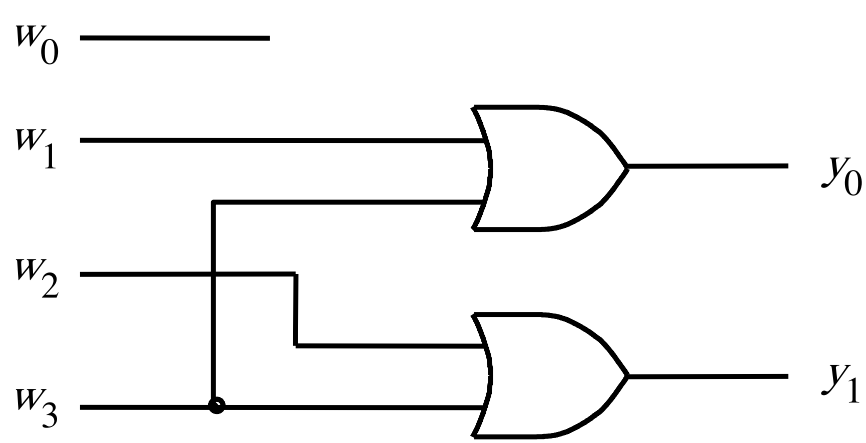
The textbook derives a different circuit for the 4-to-2 priority encoder using a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$$i_0 = \overline{w}_3\overline{w}_2\overline{w}_1 w_0$$
$$i_1 = \overline{w}_3\overline{w}_2 w_1$$
$$i_2 = \overline{w}_3 w_2$$
$$i_3 = w_3$$

$$y_0 = i_1 + i_3$$
$$y_1 = i_2 + i_3$$

$$z = i_0 + i_1 + i_2 + i_3$$



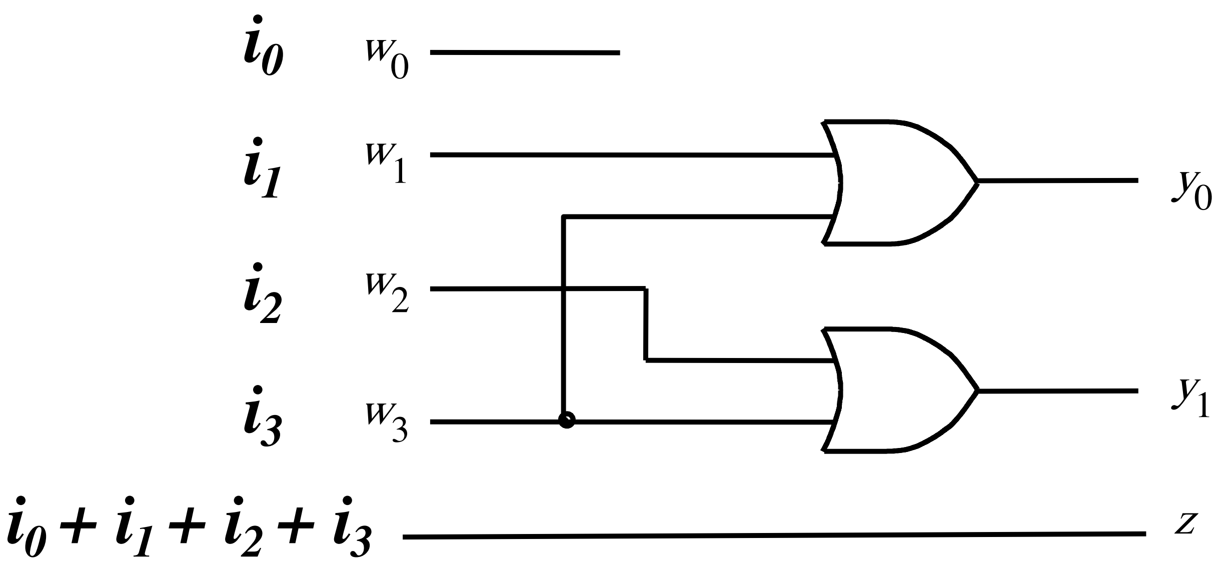
The textbook derives a different circuit for the 4-to-2 <u>priority</u> encoder using a 4-to-2 <u>binary</u> encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$$i_0 = \overline{w}_3\overline{w}_2\overline{w}_1 w_0$$
$$i_1 = \overline{w}_3\overline{w}_2 w_1$$
$$i_2 = \overline{w}_3 w_2$$
$$i_3 = w_3$$

$$y_0 = i_1 + i_3$$
$$y_1 = i_2 + i_3$$

$$z = i_0 + i_1 + i_2 + i_3$$



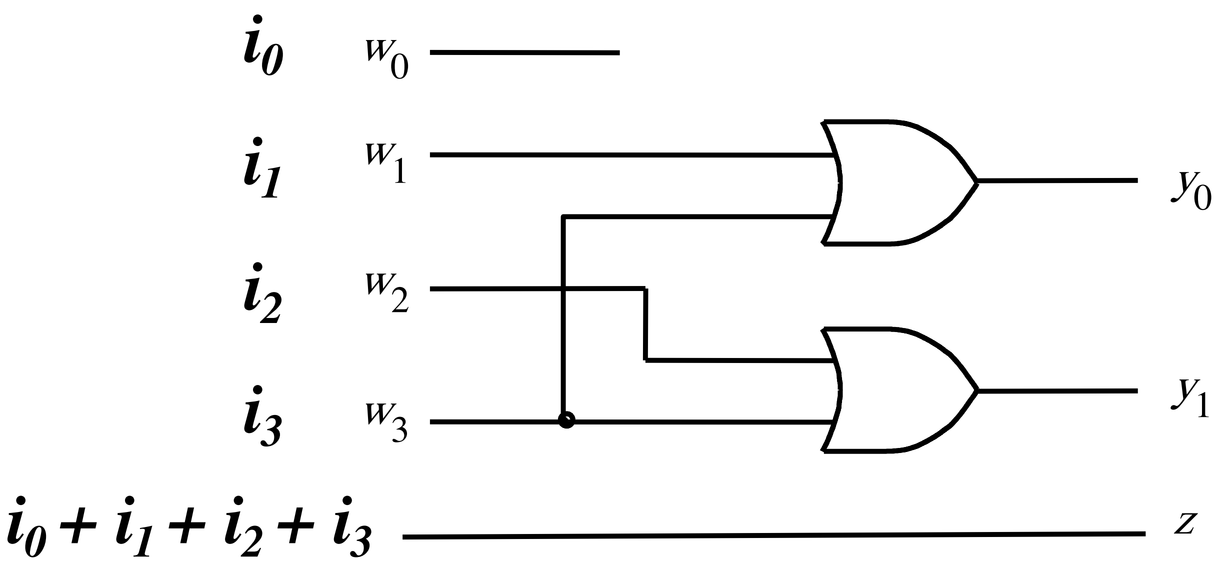
The textbook derives a different circuit for the 4-to-2 priority encoder using a 4-to-2 binary encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$$i_0 = \overline{w}_3\overline{w}_2\overline{w}_1 w_0$$
$$i_1 = \overline{w}_3\overline{w}_2 w_1$$
$$i_2 = \overline{w}_3 w_2$$
$$i_3 = w_3$$

$$y_0 = i_1 + i_3$$
$$y_1 = i_2 + i_3$$

$$z = i_0 + i_1 + i_2 + i_3$$



Try to prove that this is equivalent to the circuit that was derived above.

Code Converters

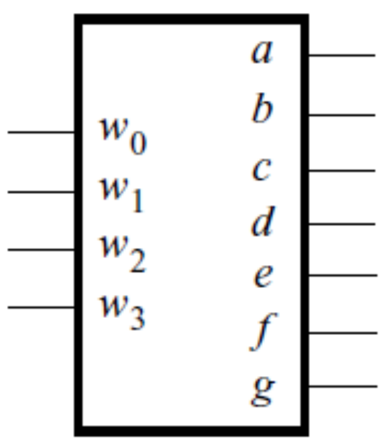
Code Converter (Definition)

- Converts from one type of input encoding to a different type of output encoding.

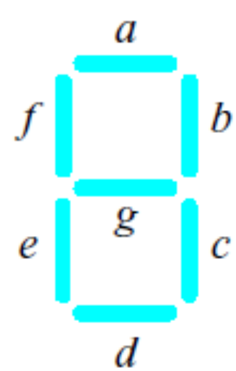
Code Converter (Definition)

- Converts from one type of input encoding to a different type of output encoding.
- A decoder does that as well, but its outputs are always one-hot encoded so the output code is really only one type of output code.
- A binary encoder does that as well but its inputs are always one-hot encoded so the input code is really only one type of input code.

A hex-to-7-segment display code converter



(a) Code converter



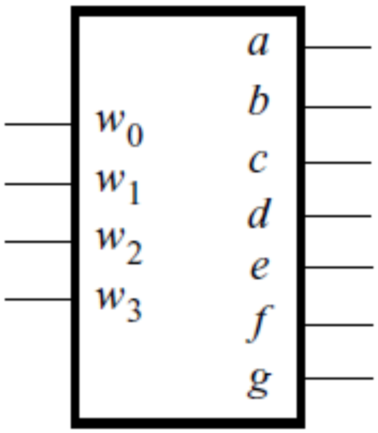
(b) 7-segment display

w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

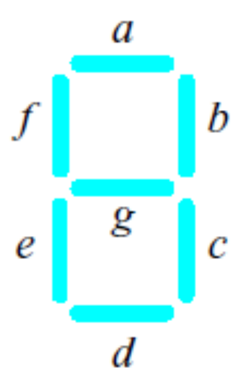
(c) Truth table

[Figure 4.21 from the textbook]

A hex-to-7-segment display code converter



(a) Code converter



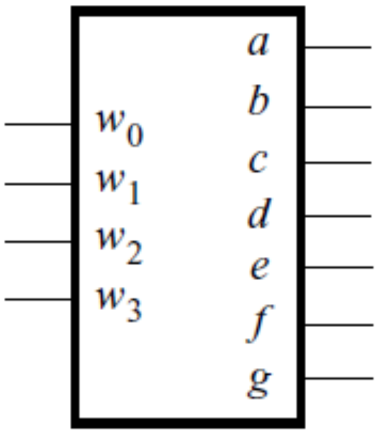
(b) 7-segment display

w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

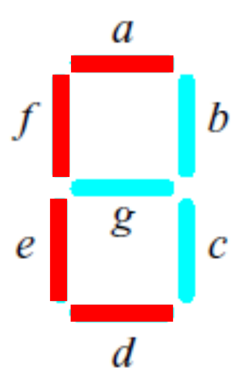
(c) Truth table

[Figure 4.21 from the textbook]

A hex-to-7-segment display code converter



(a) Code converter



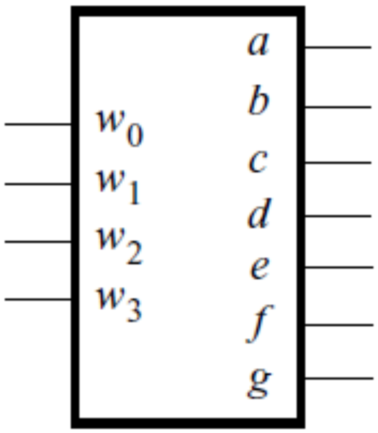
(b) 7-segment display

w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

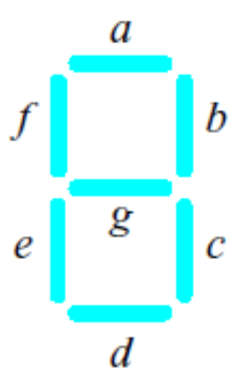
(c) Truth table

[Figure 4.21 from the textbook]

A hex-to-7-segment display code converter



(a) Code converter



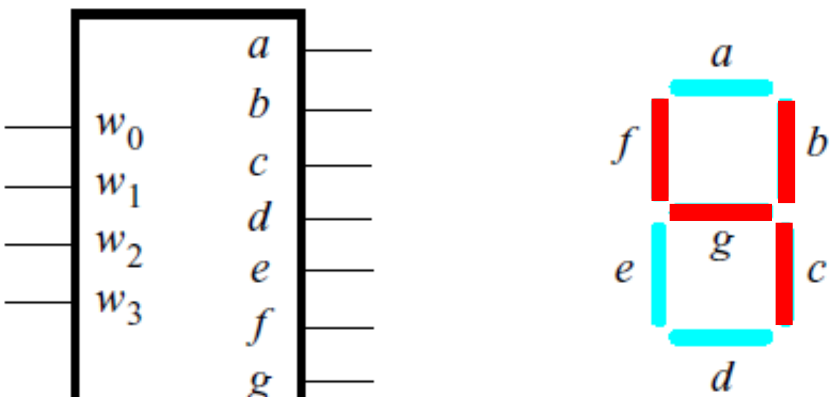
(b) 7-segment display

w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

(c) Truth table

[Figure 4.21 from the textbook]

A hex-to-7-segment display code converter



(a) Code converter

(b) 7-segment display

w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

(c) Truth table

[Figure 4.21 from the textbook]

What is the circuit for this code converter?

x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

What is the circuit for this code converter?

x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

$$f(x_1, x_2, x_3, x_4) = \Sigma\, m(0, 2, 3, 5, 6, 7, 8, 9, 10, 12, 14, 15)$$

What is the circuit for this code converter?

x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

x_3x_4 \ x_1x_2	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	1	1	1	0
10	1	1	1	1

$$f(x_1, x_2, x_3, x_4) = \Sigma\, m(0, 2, 3, 5, 6, 7, 8, 9, 10, 12, 14, 15)$$

What is the circuit for this code converter?

x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

What is the circuit for this code converter?

x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

$x_3 x_4$ \ $x_1 x_2$	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	1	0	0	1
10	1	1	1	0

$$f(x_1, x_2, x_3, x_4) = \Sigma\, m(0, 2, 3, 5, 6, 8, 9, 11, 12, 13, 14)$$

Arithmetic Comparison Circuits

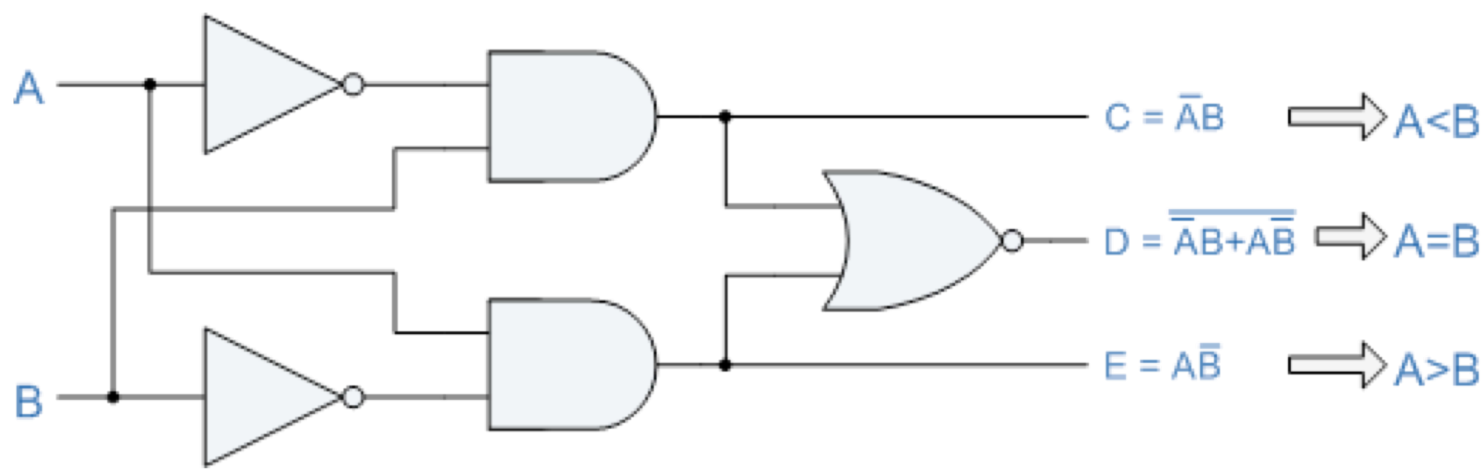
Truth table for a one-bit digital comparator

Inputs		Outputs		
A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

[http://en.wikipedia.org/wiki/Digital_comparator]

A one-bit digital comparator circuit

Inputs		Outputs		
A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0



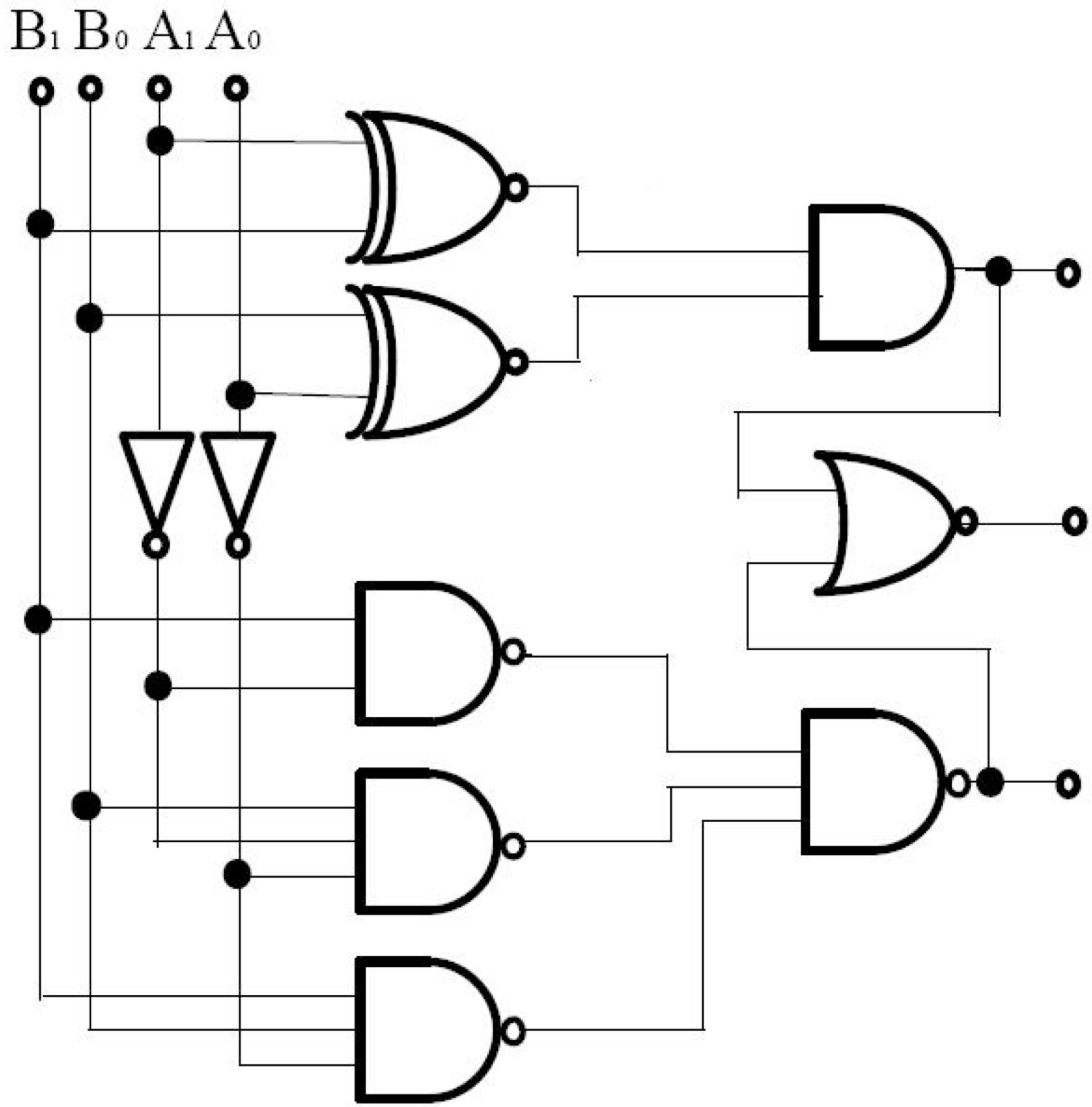
[http://www.personal.psu.edu/users///c/w/cwb5096/Old%20Site/index_files/cmpenlab4.htm]

Truth table for a two-bit digital comparator

Inputs				Outputs		
A_1	A_0	B_1	B_0	$A < B$	$A = B$	$A > B$
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

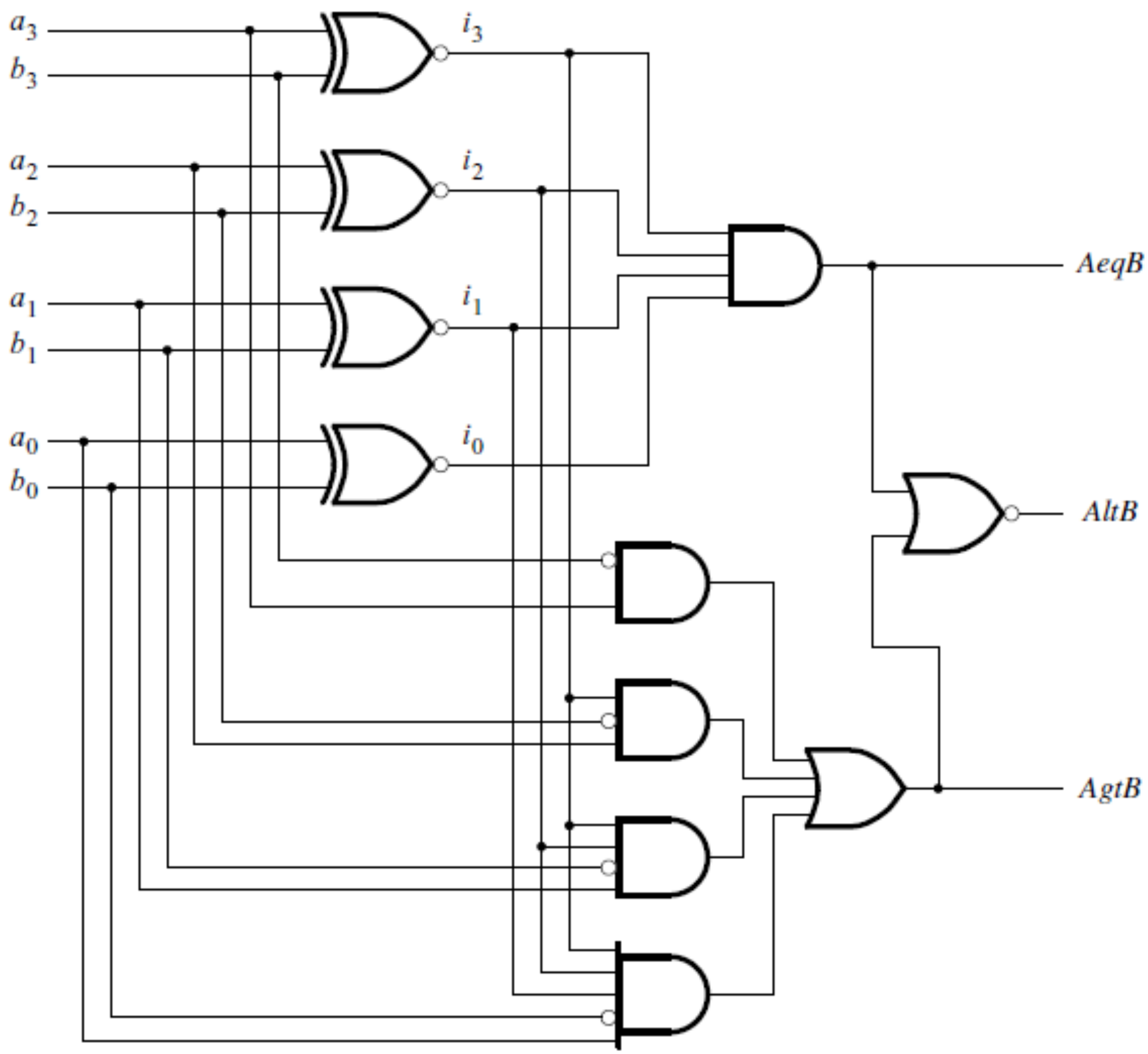
[http://en.wikipedia.org/wiki/Digital_comparator]

A two-bit digital comparator circuit



[http://forum.allaboutcircuits.com/showthread.php?t=10561]

A four-bit comparator circuit



[Figure 4.22 from the textbook]

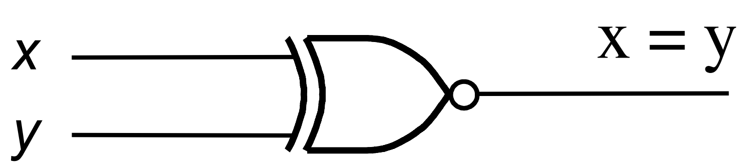
Comparison of 1-bit numbers

Equal

x	y	x = y
0	0	1
0	1	0
1	0	0
1	1	1

Equal

x	y	x = y
0	0	1
0	1	0
1	0	0
1	1	1

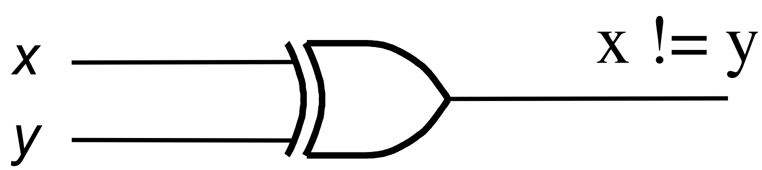


Not Equal

x	y	x != y
0	0	0
0	1	1
1	0	1
1	1	0

Not Equal

x	y	x != y
0	0	0
0	1	1
1	0	1
1	1	0



Less

x	y	x < y
0	0	0
0	1	1
1	0	0
1	1	0

Less or Equal

x	**y**	**x <= y**
0	0	1
0	1	1
1	0	0
1	1	1

Less or Equal

x	y	x < y
0	0	0
0	1	1
1	0	0
1	1	0

or

x	y	x = y
0	0	1
0	1	0
1	0	0
1	1	1

=

x	y	x <= y
0	0	1
0	1	1
1	0	0
1	1	1

Greater

x	y	x > y
0	0	0
0	1	0
1	0	1
1	1	0

Greater or Equal

x	y	x >= y
0	0	1
0	1	0
1	0	1
1	1	1

Greater or Equal

x	y	x > y
0	0	0
0	1	0
1	0	1
1	1	0

or

x	y	x = y
0	0	1
0	1	0
1	0	0
1	1	1

=

x	y	x <= y
0	0	1
0	1	0
1	0	1
1	1	1

Some Interesting Dualities

Equal

x	y	x = y
0	0	1
0	1	0
1	0	0
1	1	1

Not Equal

x	y	x != y
0	0	0
0	1	1
1	0	1
1	1	0

Greater

x	y	x > y
0	0	0
0	1	0
1	0	1
1	1	0

Less or Equal

x	y	x <= y
0	0	1
0	1	1
1	0	0
1	1	1

Greater or Equal

x	y	x >= y
0	0	1
0	1	0
1	0	1
1	1	1

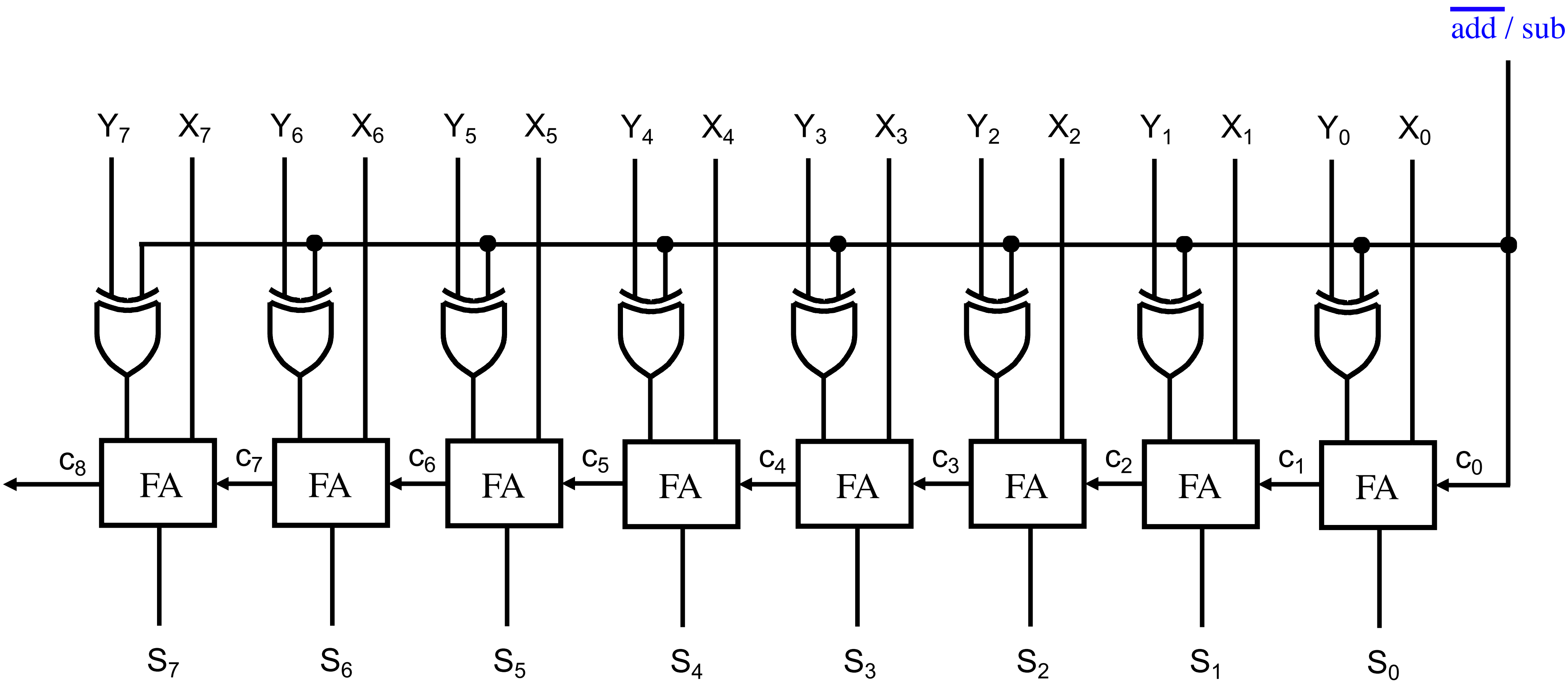
Less

x	y	x < y
0	0	0
0	1	1
1	0	0
1	1	0

Some Interesting Dualities

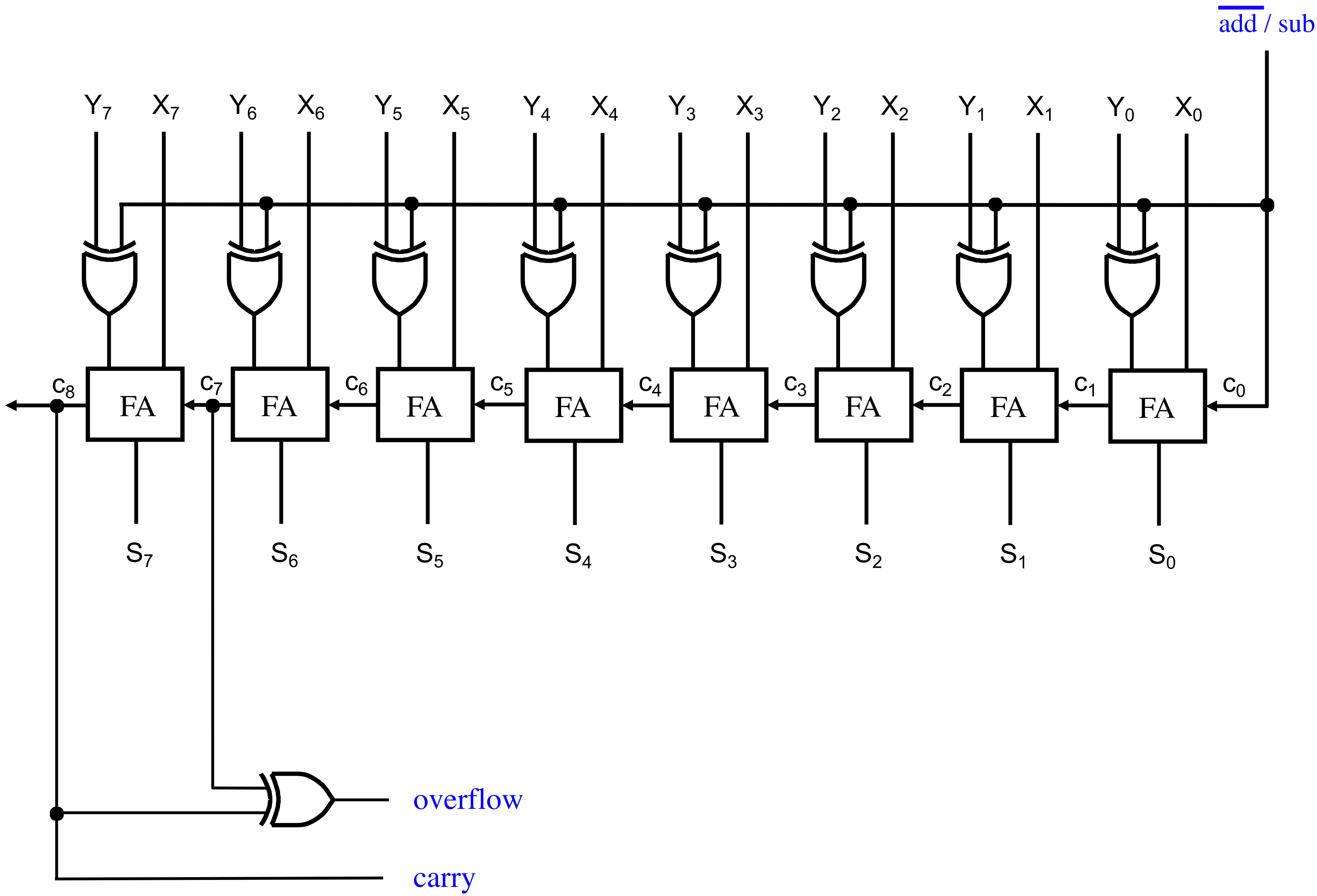
- $\overline{\text{Equal}}$ = Not Equal
- $\overline{\text{Greater}}$ = Less or Equal
- $\overline{\text{Less}}$ = Greater or Equal

The Adder / Subtractor

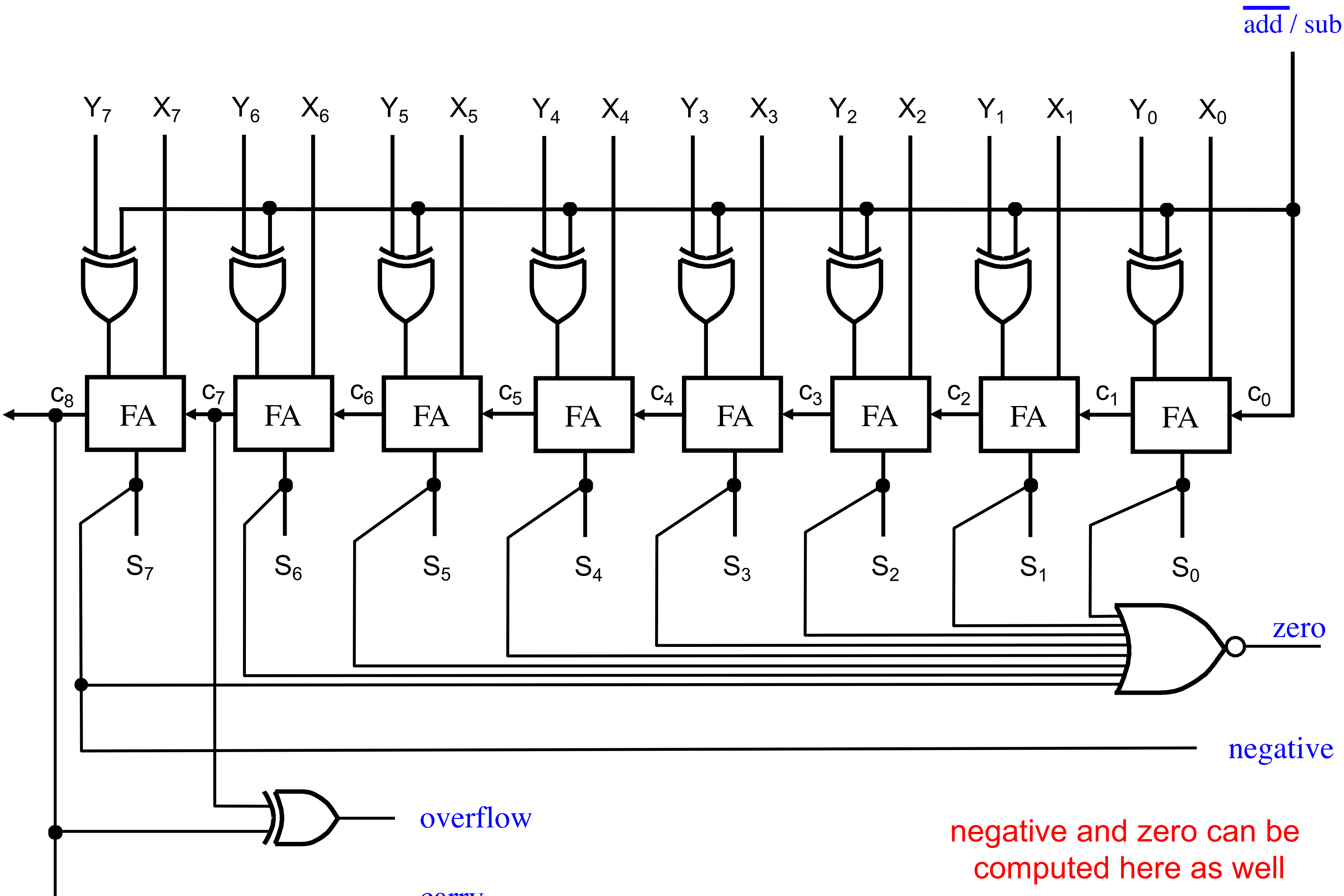


This is an 8-bit ripple-carry adder. Note that the X and Y lines are swapped.

The Adder / Subtractor



The Adder / Subtractor



negative and zero can be computed here as well

Abbreviations for the Flags

- Carry Flag (CF)
- Overflow Flag (OF)
- Negative Flag (NF)
- Zero Flag (ZF)

Abbreviations for the Flags

In some CPU architectures the carry flag means borrow. And it could be inverted relative to the previous diagram.

- **Carry Flag (CF)**
- **Overflow Flag (OF)**
- **Negative Flag (NF)**
- **Zero Flag (ZF)**

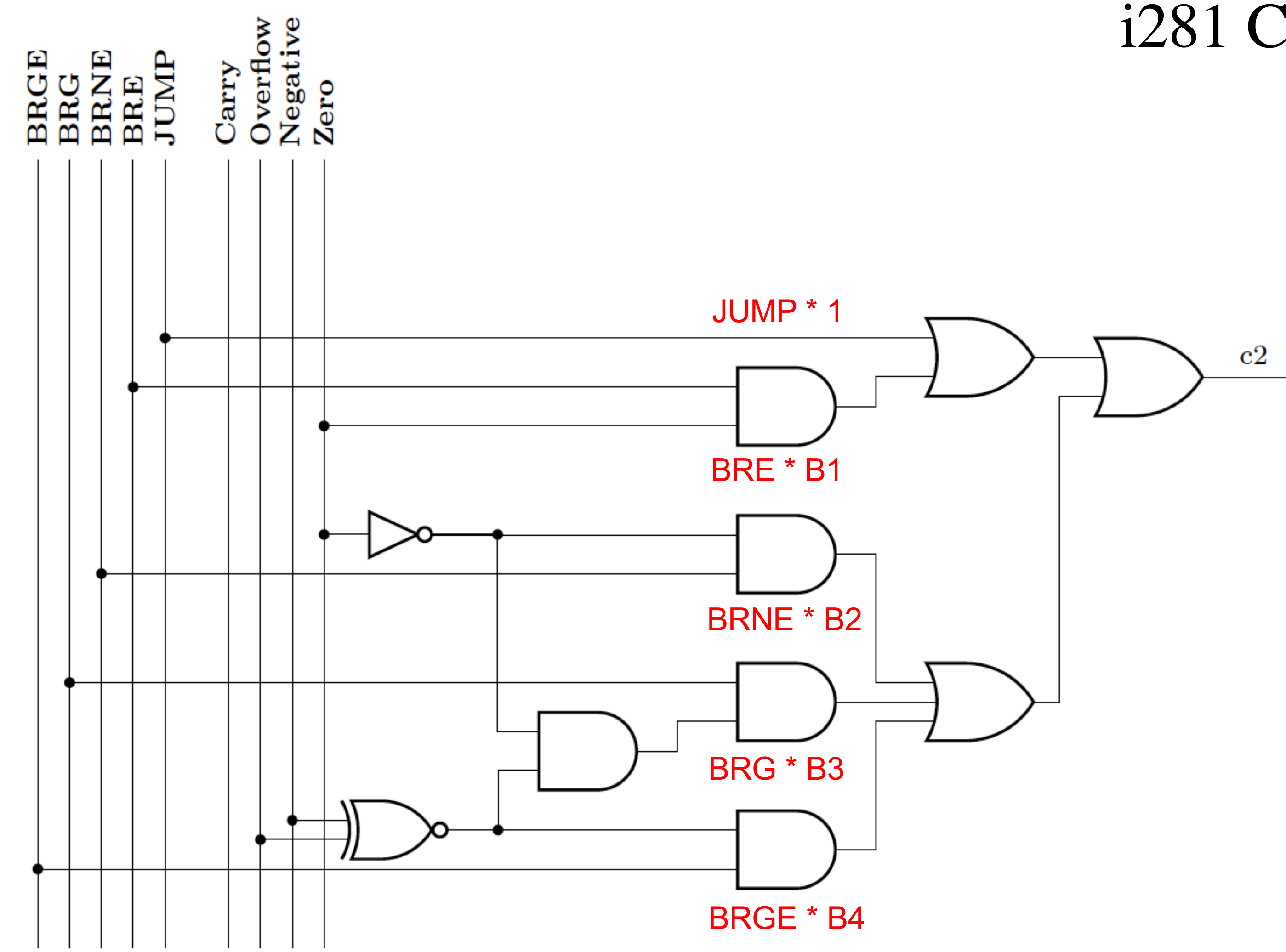
Comparison of Signed Numbers

• Equal	ZF = 1
• Not equal	ZF = 0
• Greater	ZF = 0 and NF = OF
• Greater or Equal	NF = OF
• Less	NF != OF
• Less or Equal	ZF = 1 or NF != OF

Comparison of Signed Numbers

• Equal	ZF
• Not equal	$\overline{ZF}$
• Greater	$\overline{ZF} \bullet \text{XNOR}(NF, OF)$
• Greater or Equal	$\text{XNOR}(NF, OF)$
• Less	$\text{XOR}(NF, OF)$
• Less or Equal	$ZF + \text{XOR}(NF, OF)$

i281 CPU



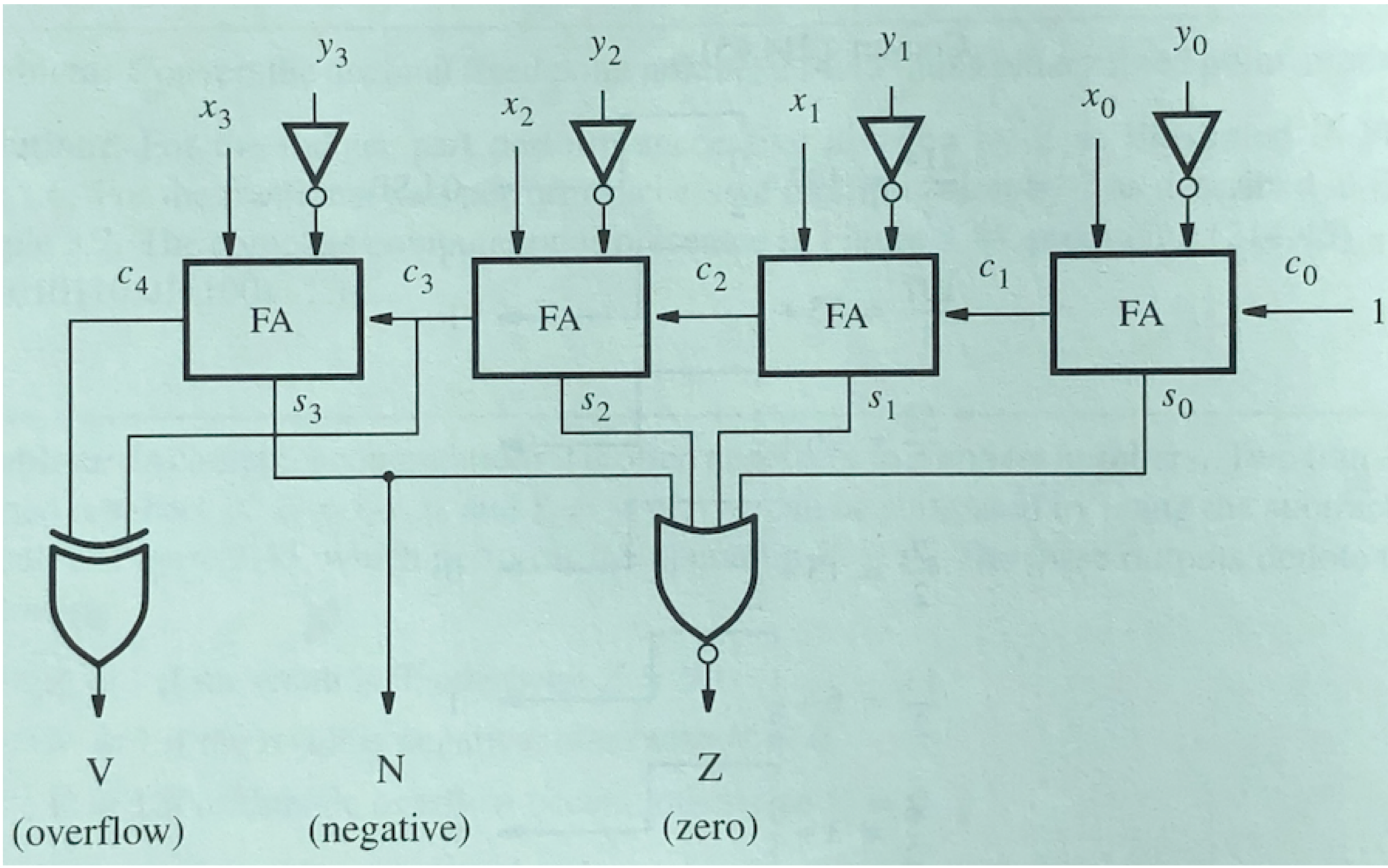
JUMP		1	1															
BRE/BRZ		B1	1															
BRNE/BRNZ		B2	1															
BRG		B3	1															
BRGE		B4	1															

C_2 is the OR of these five times the OPCODE

```
B1=  ZF
B2= ~ZF
B3= AND(~ZF, XNOR(NF, OF))
B4= XNOR(NF, OF)
```

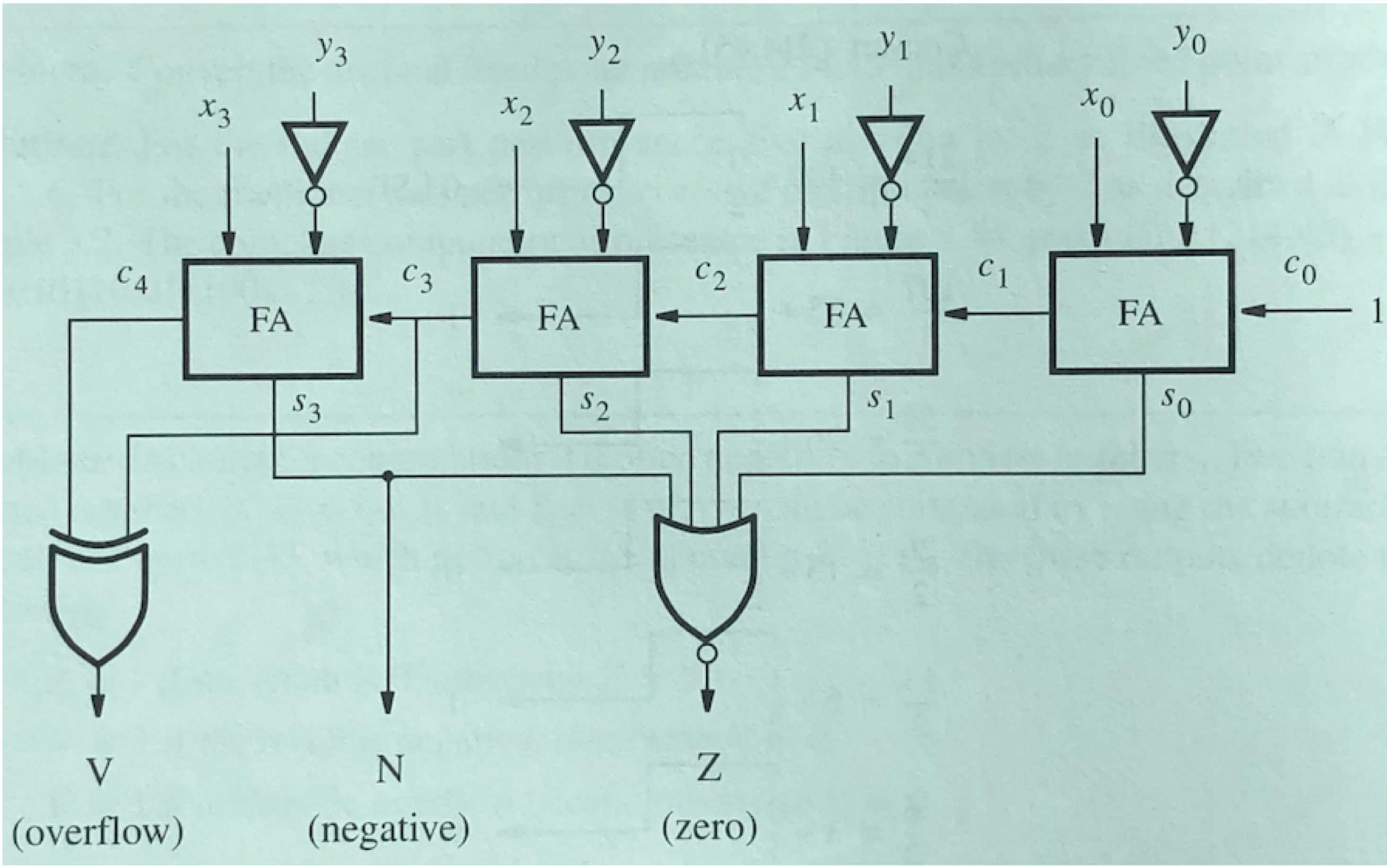
Zero Flag (ZF)
Negative Flag (NF)
Overflow Flag (OF)

A four-bit comparator circuit



[Figure 3.45 from the textbook]

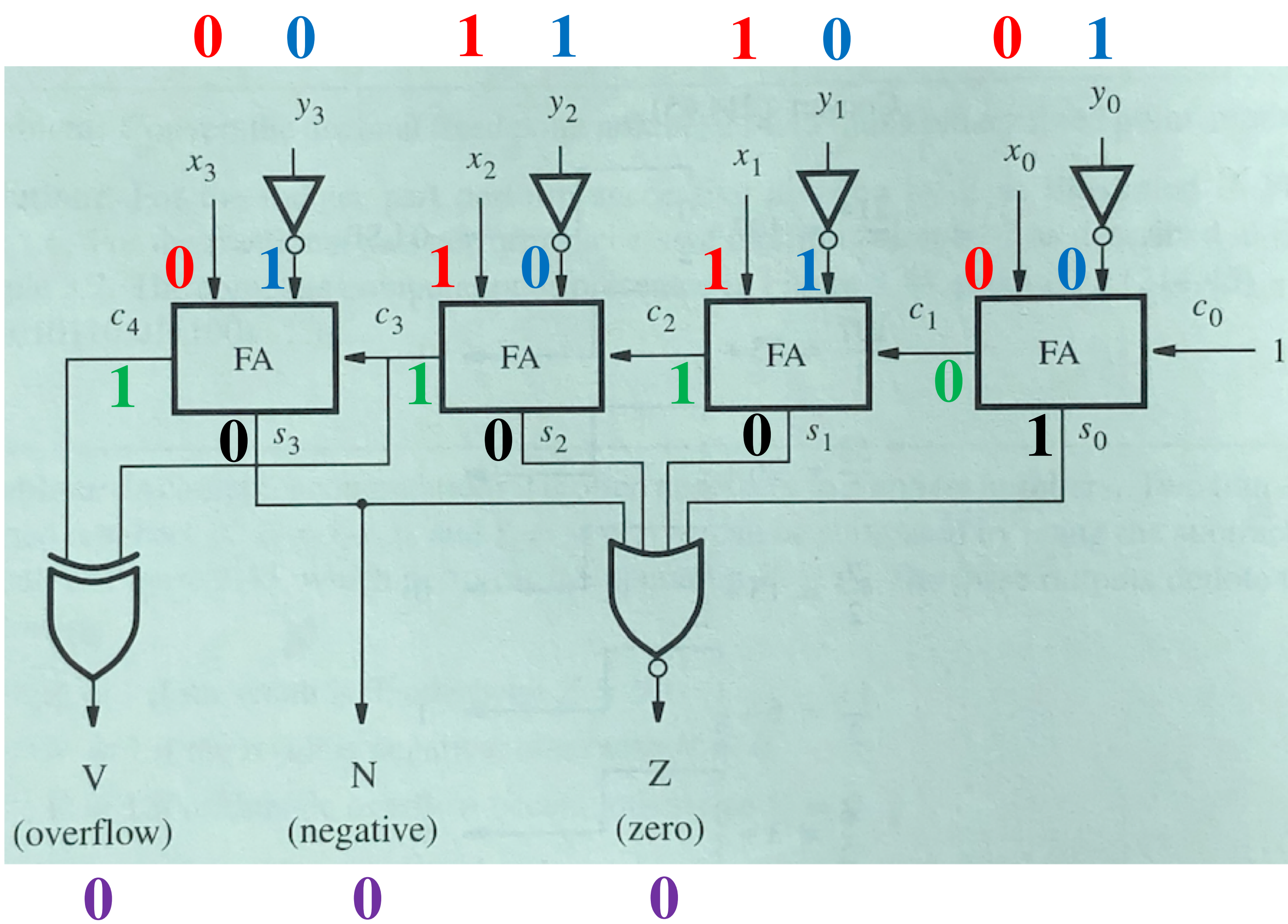
A four-bit comparator circuit



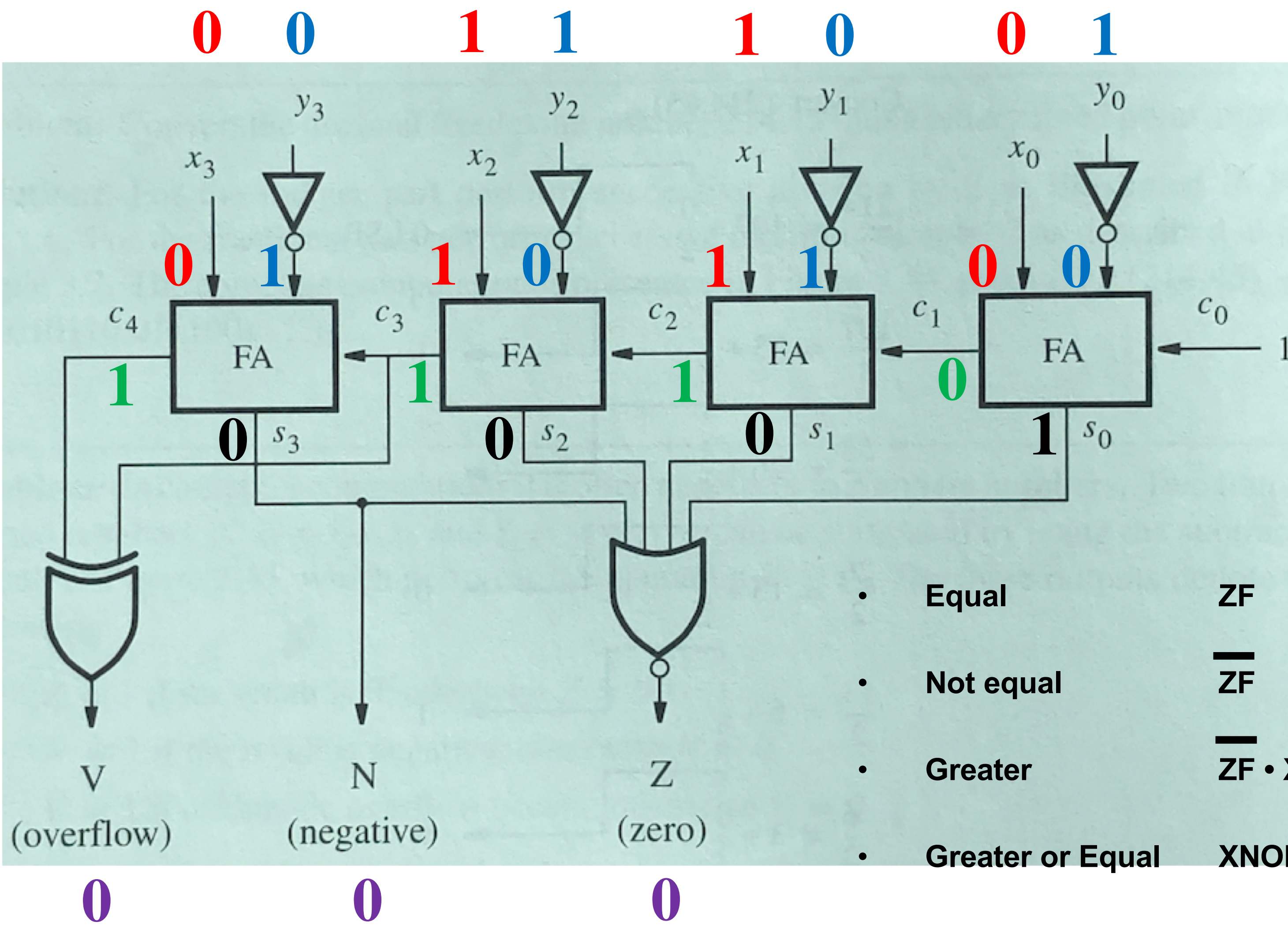
OF NF ZF

alternative names for the flags

Compare 6 with 5: (+6) - (+5)

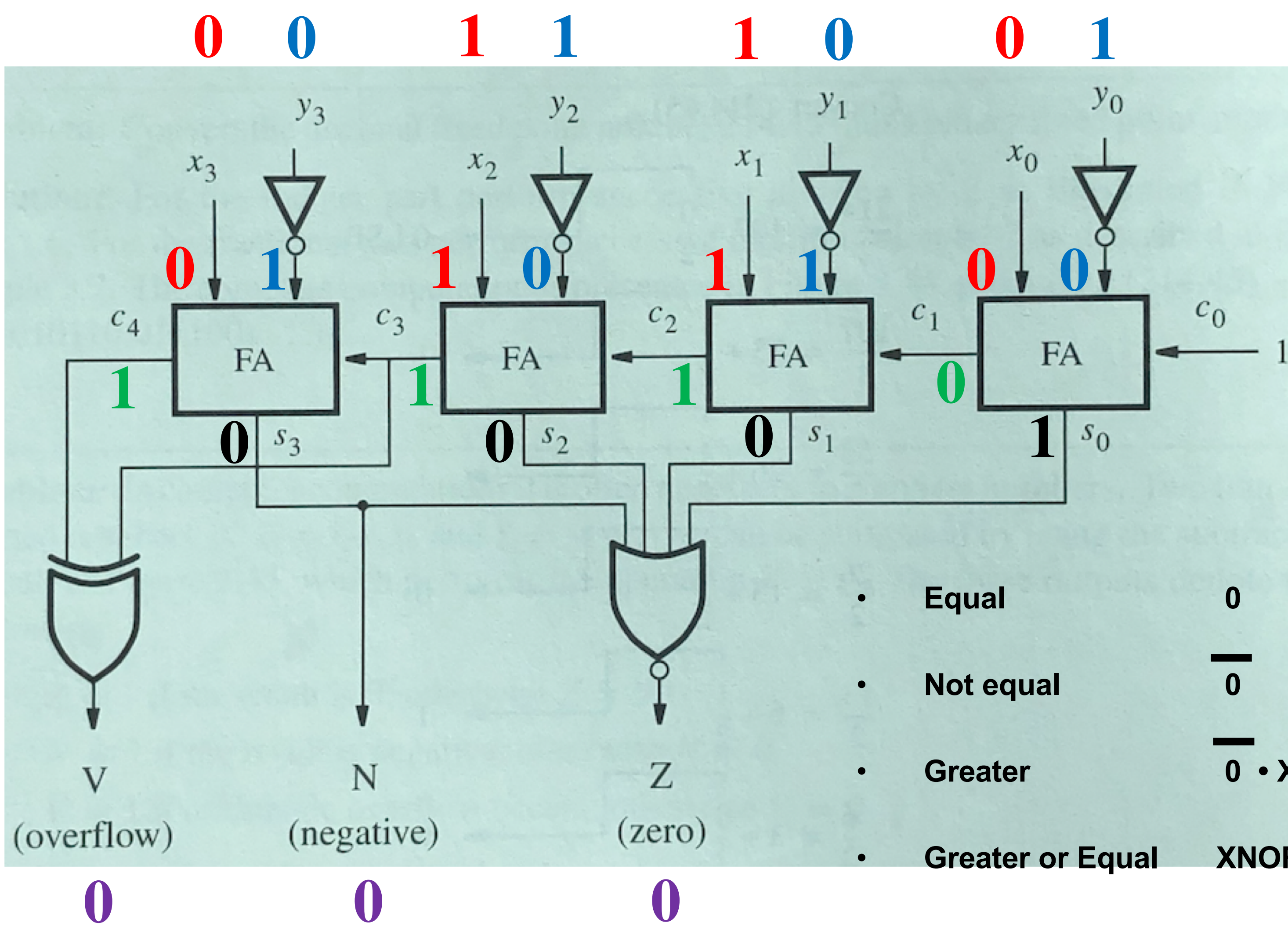


Compare 6 with 5: (+6) - (+5)



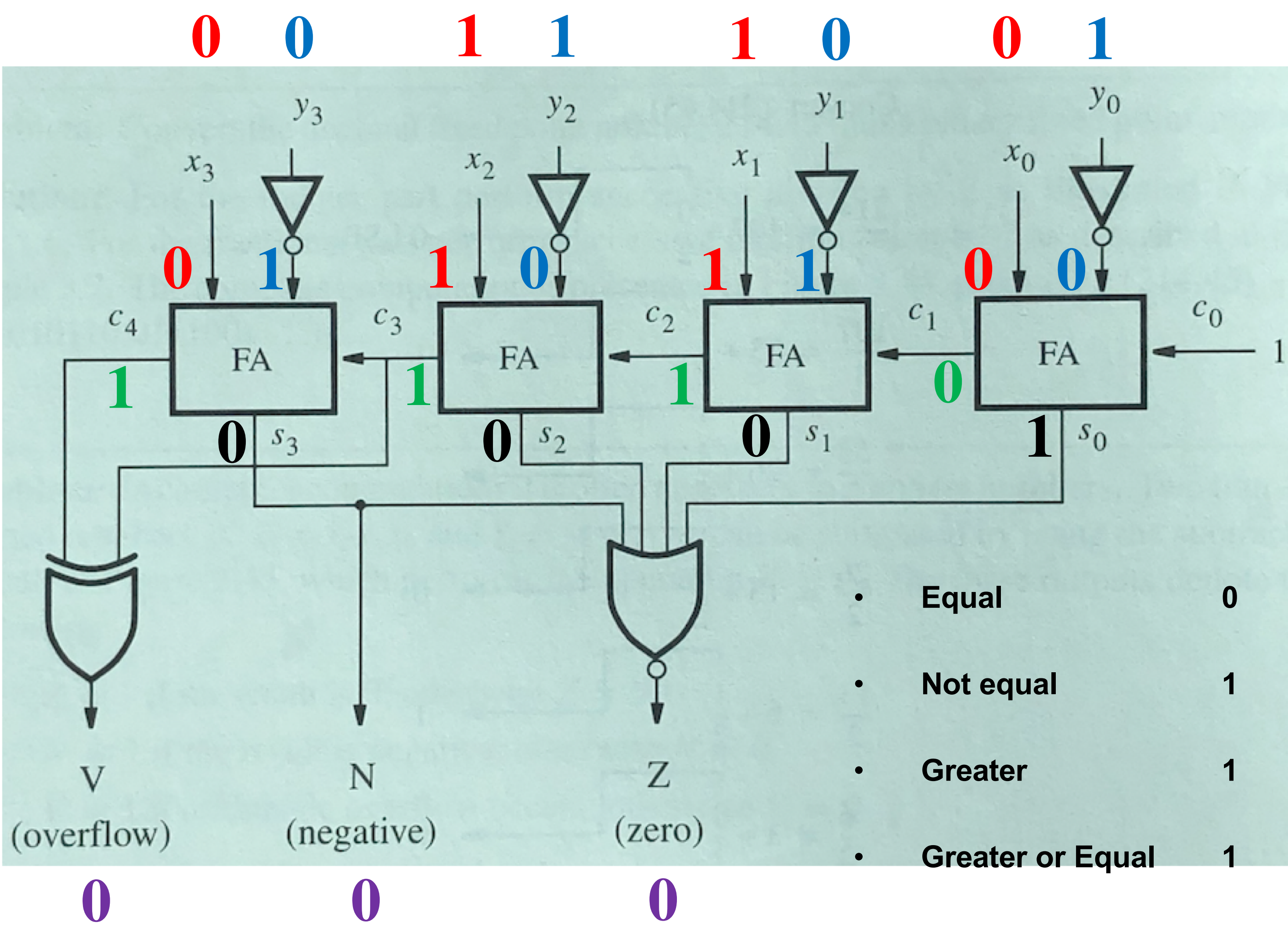
- Equal — ZF
- Not equal — $\overline{\text{ZF}}$
- Greater — $\overline{\text{ZF}}$ • XNOR(NF, OF)
- Greater or Equal — XNOR(NF, OF)
- Less — XOR(NF, OF)
- Less or Equal — ZF + XOR(NF, OF)

Compare 6 with 5: (+6) - (+5)



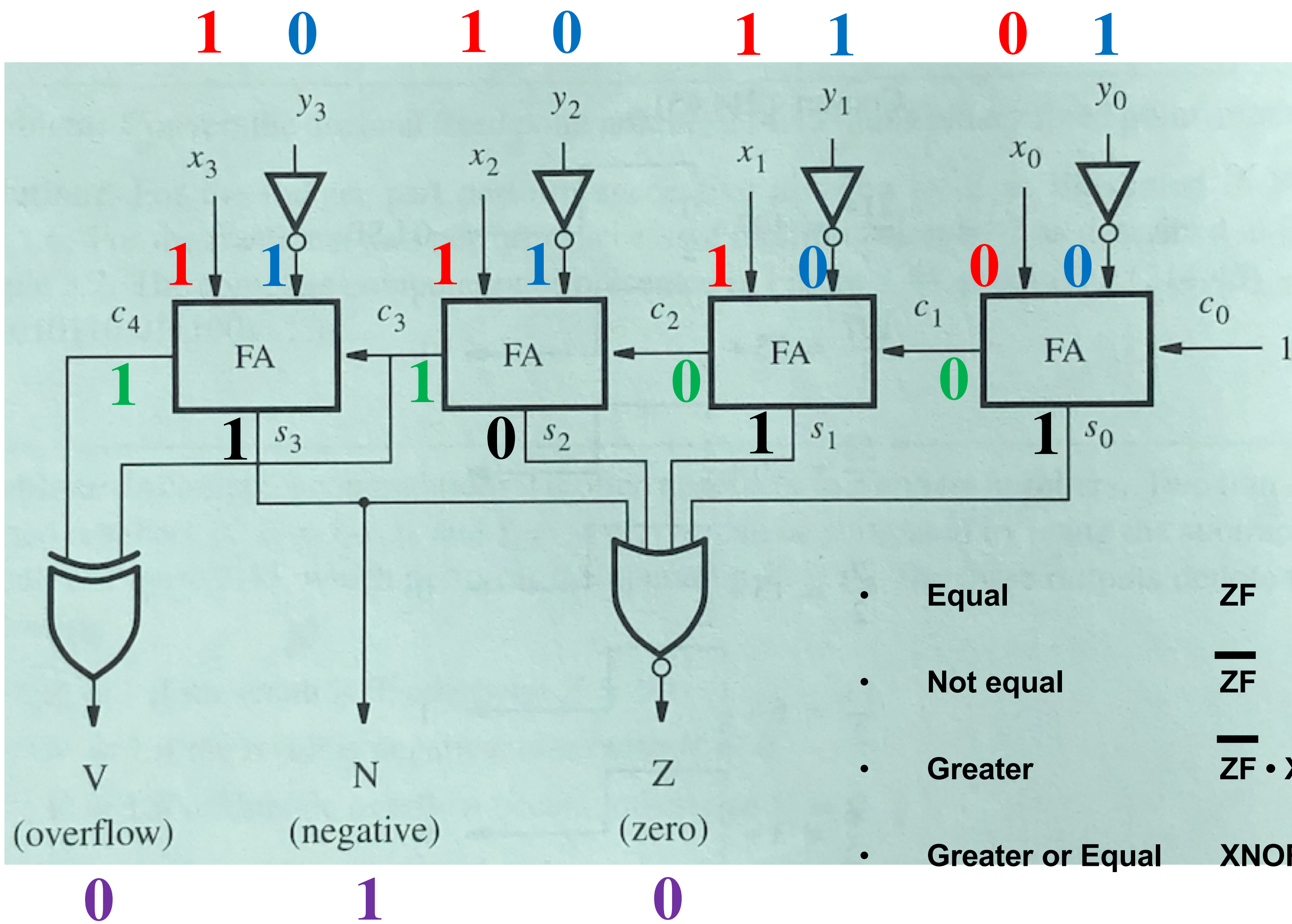
- Equal 0
- Not equal $\overline{0}$
- Greater $\overline{0}$ • XNOR(0, 0)
- Greater or Equal XNOR(0, 0)
- Less XOR(0, 0)
- Less or Equal 0 + XOR(0, 0)

Compare 6 with 5: (+6) - (+5)



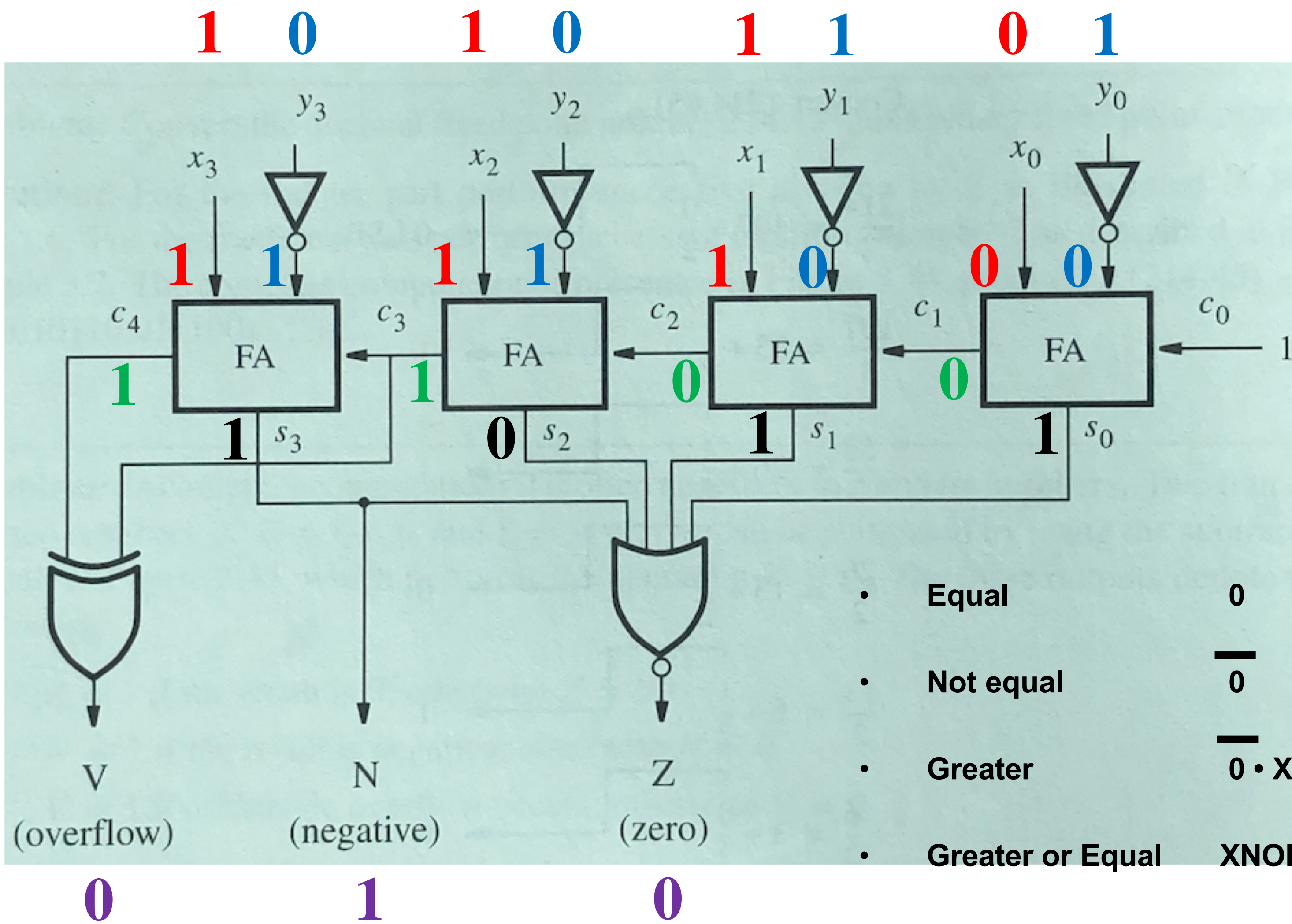
- Equal 0
- Not equal 1
- Greater 1
- Greater or Equal 1
- Less 0
- Less or Equal 0

Compare negative 2 with 3: (-2) - (+3)



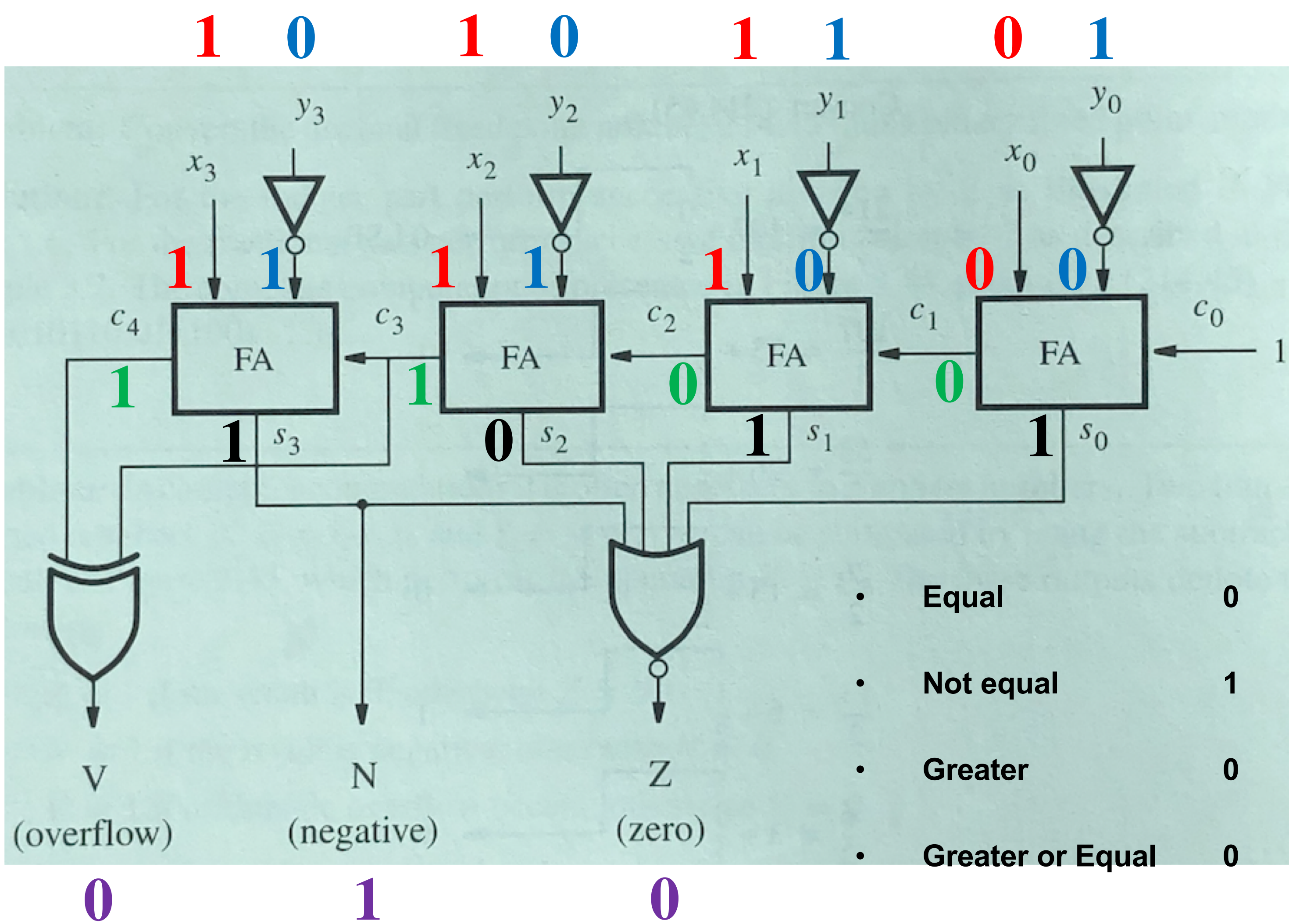
- Equal — ZF
- Not equal — $\overline{ZF}$
- Greater — $\overline{ZF}$ • XNOR(NF, OF)
- Greater or Equal — XNOR(NF, OF)
- Less — XOR(NF, OF)
- Less or Equal — ZF + XOR(NF, OF)

Compare negative 2 with 3: (-2) - (+3)



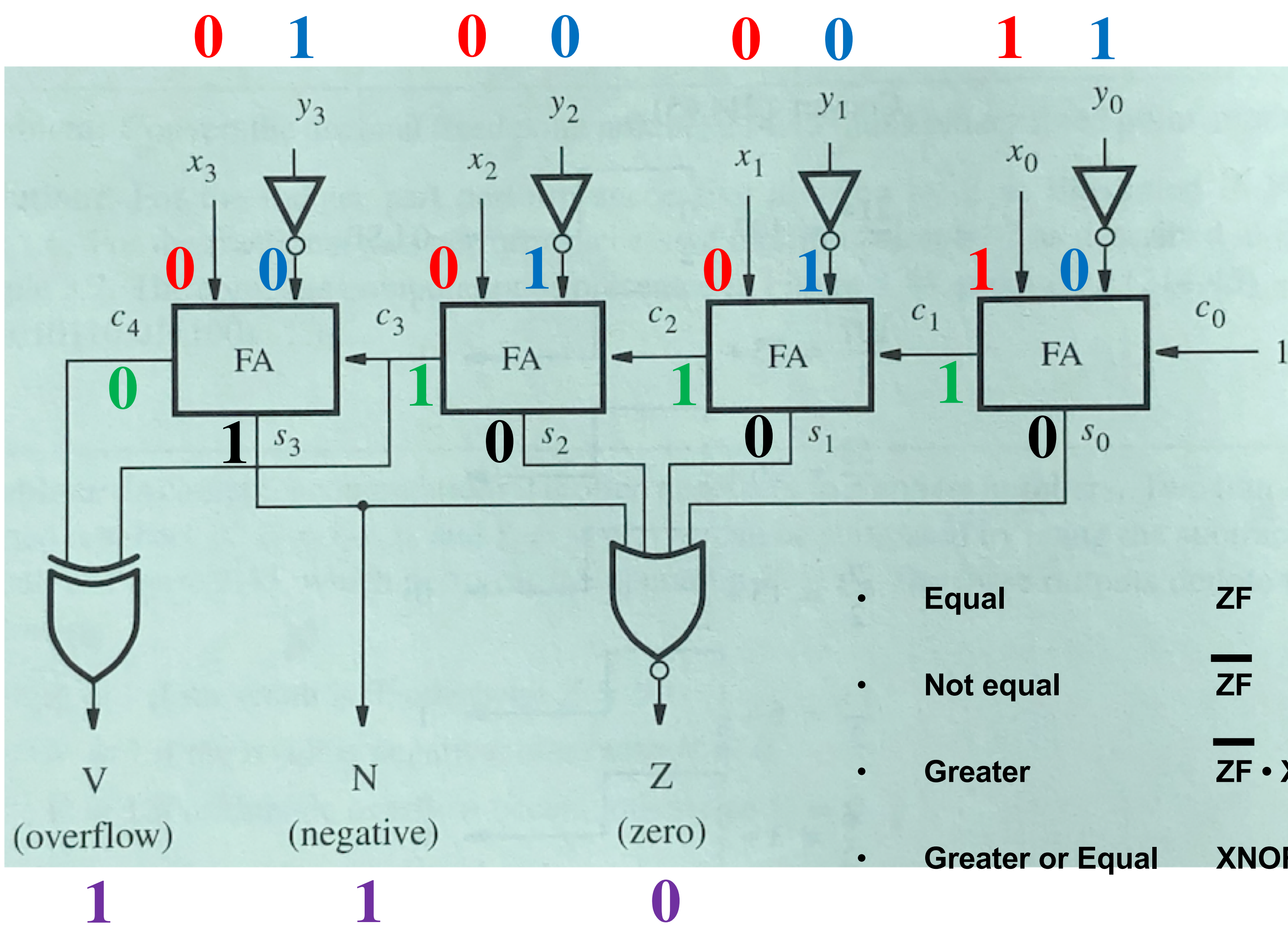
- Equal 0
- Not equal $\overline{0}$
- Greater $\overline{0}$ • XNOR(1, 0)
- Greater or Equal XNOR(1, 0)
- Less XOR(1, 0)
- Less or Equal 0 + XOR(1, 0)

Compare negative 2 with 3: (-2) - (+3)



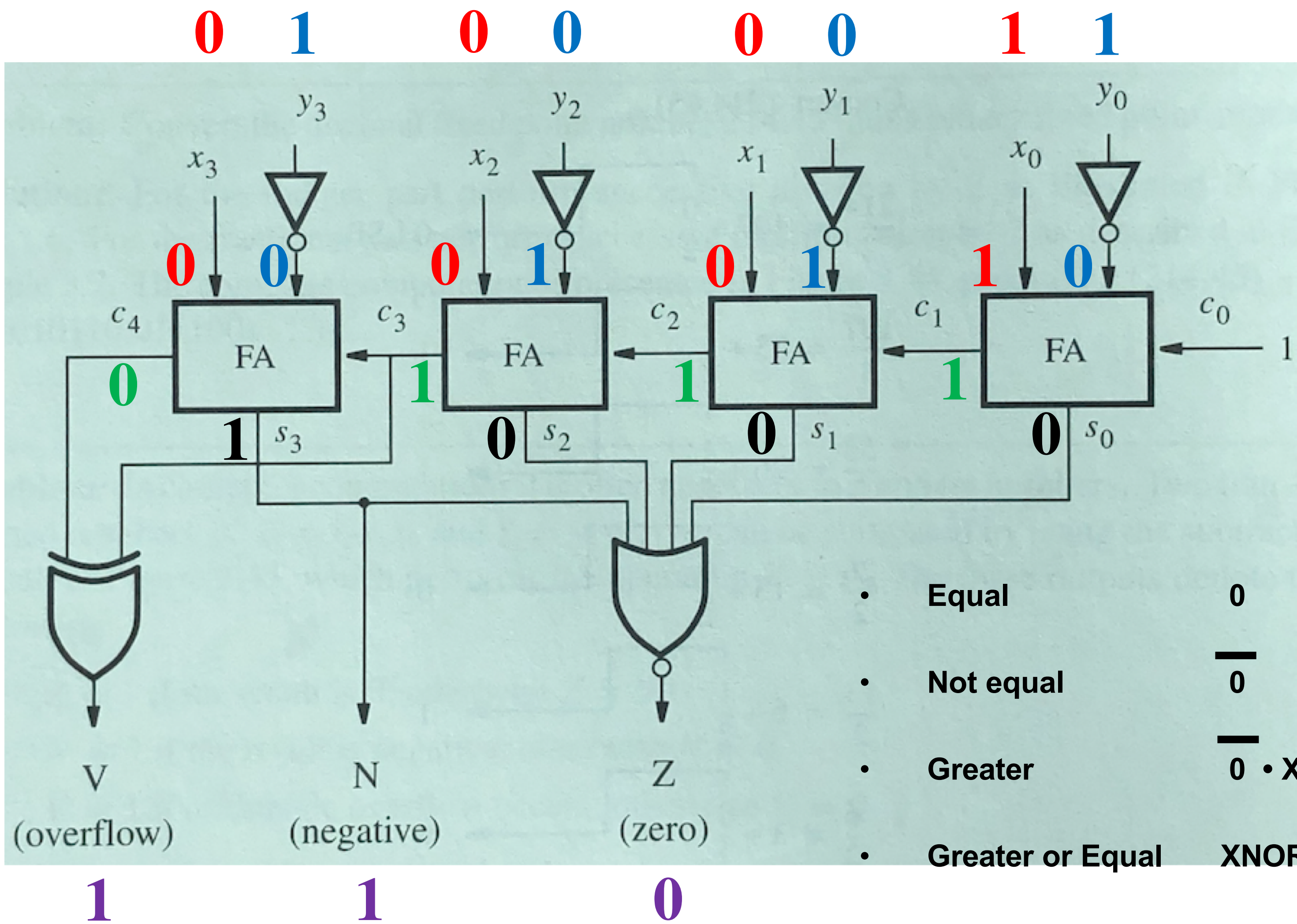
- Equal 0
- Not equal 1
- Greater 0
- Greater or Equal 0
- Less 1
- Less or Equal 1

Compare 1 with negative 7: (+1) - (-7)



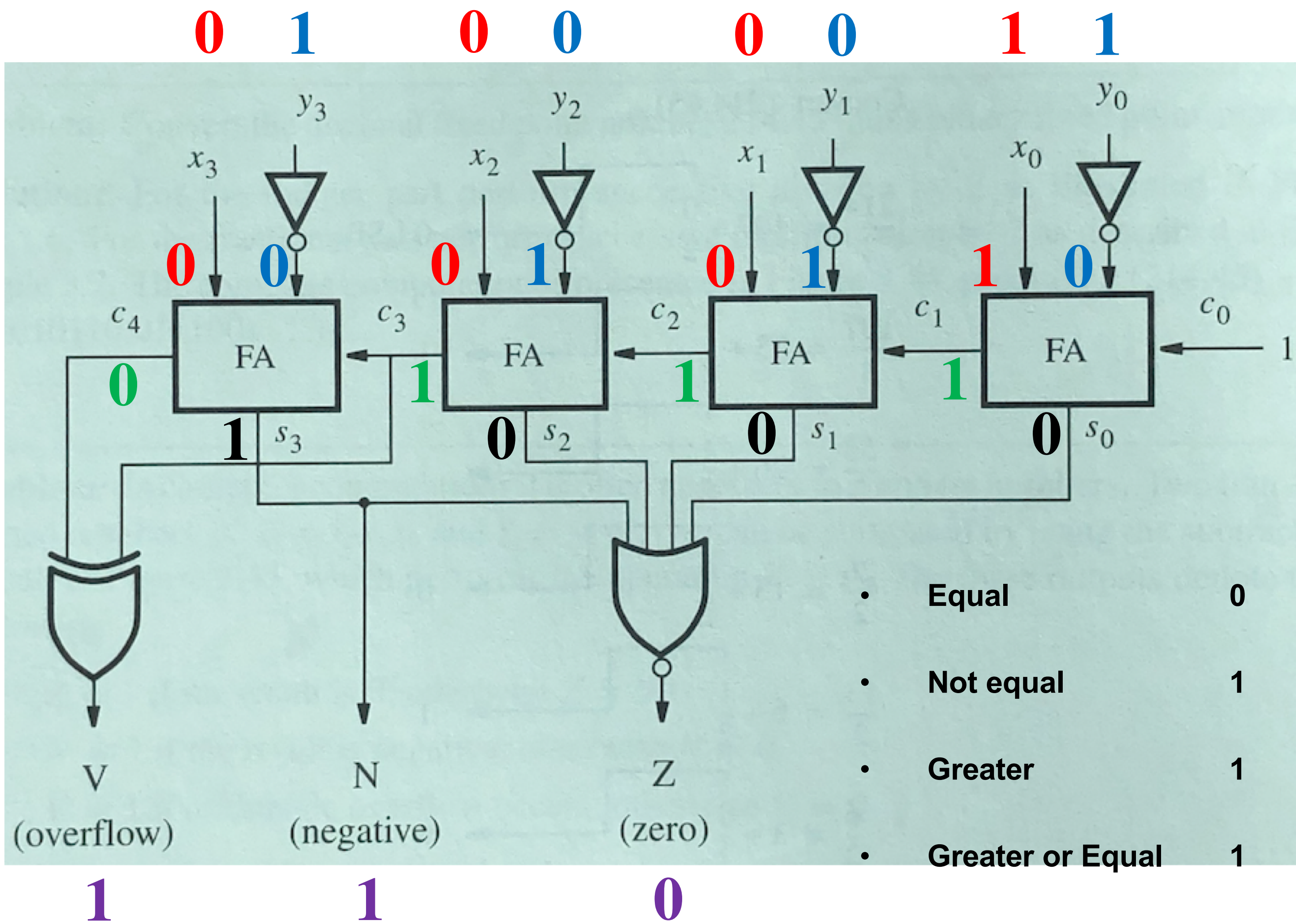
- Equal — ZF
- Not equal — $\overline{ZF}$
- Greater — $\overline{ZF}$ • XNOR(NF, OF)
- Greater or Equal — XNOR(NF, OF)
- Less — XOR(NF, OF)
- Less or Equal — ZF + XOR(NF, OF)

Compare 1 with negative 7: (+1) - (-7)



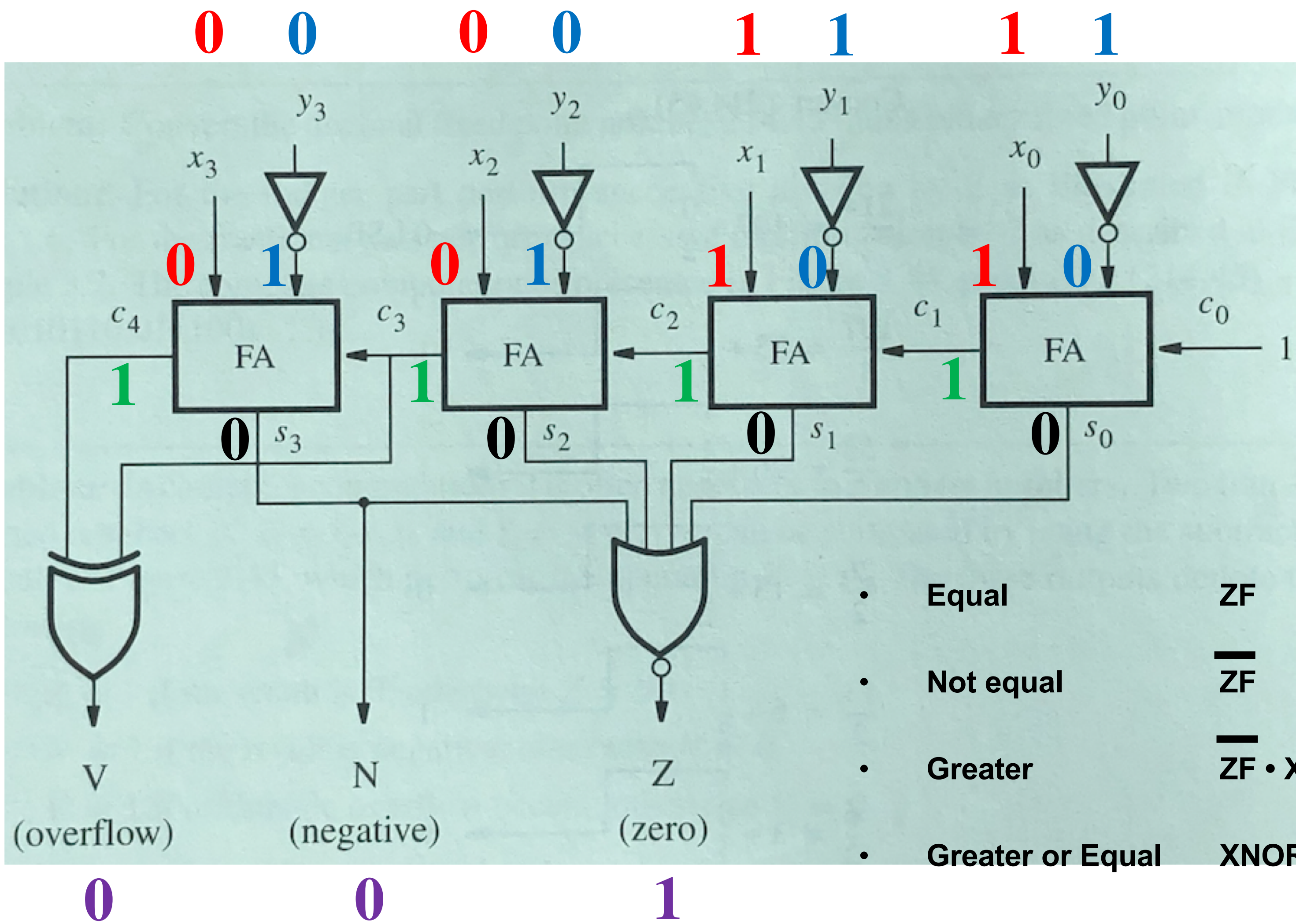
- Equal 0
- Not equal $\overline{0}$
- Greater $\overline{0}$ • XNOR(1, 1)
- Greater or Equal XNOR(1, 1)
- Less XOR(1, 1)
- Less or Equal 0 + XOR(1, 1)

Compare 1 with negative 7: (+1) - (-7)



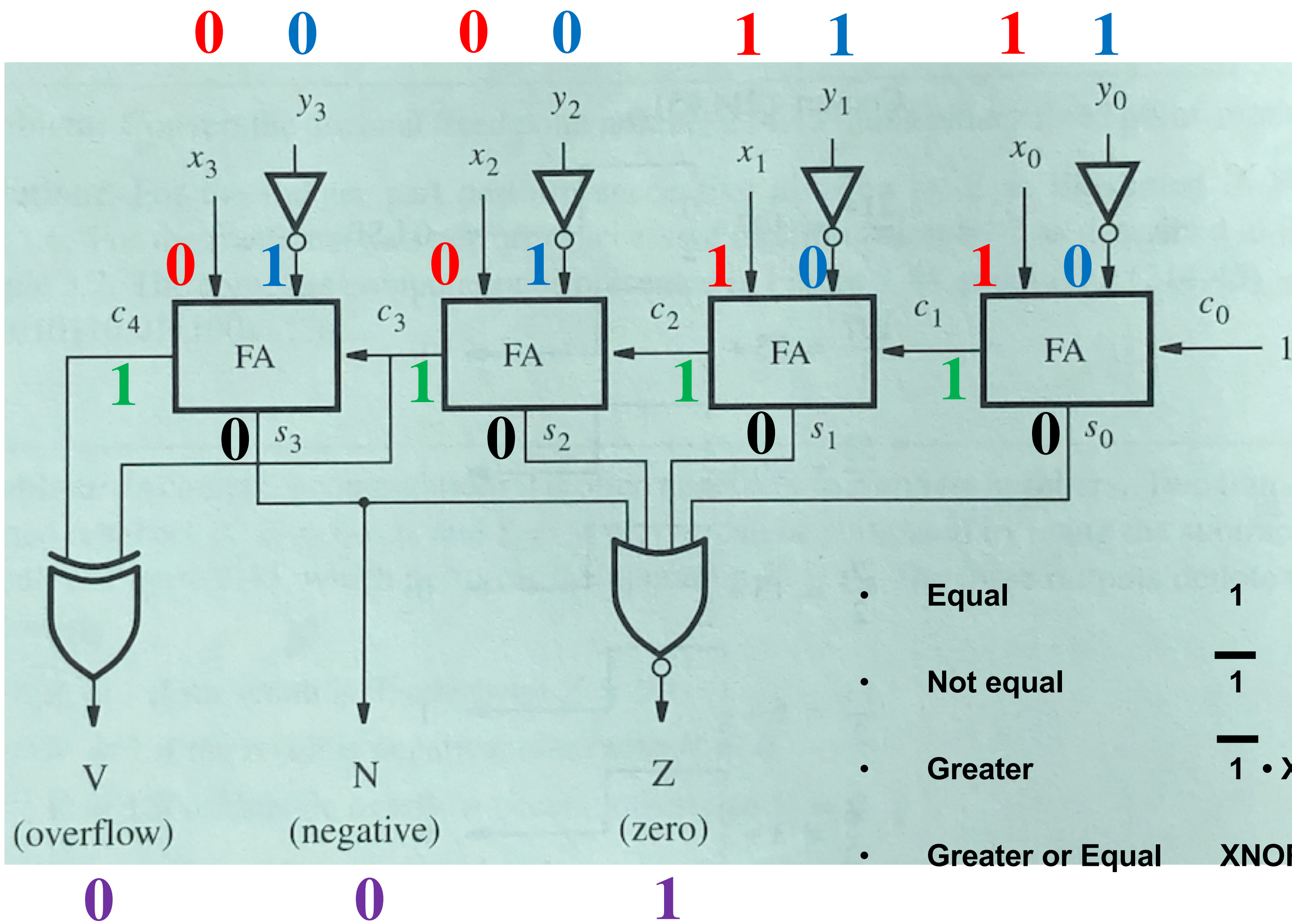
Equal	0
Not equal	1
Greater	1
Greater or Equal	1
Less	0
Less or Equal	0

Compare 3 with 3: (+3) - (+3)



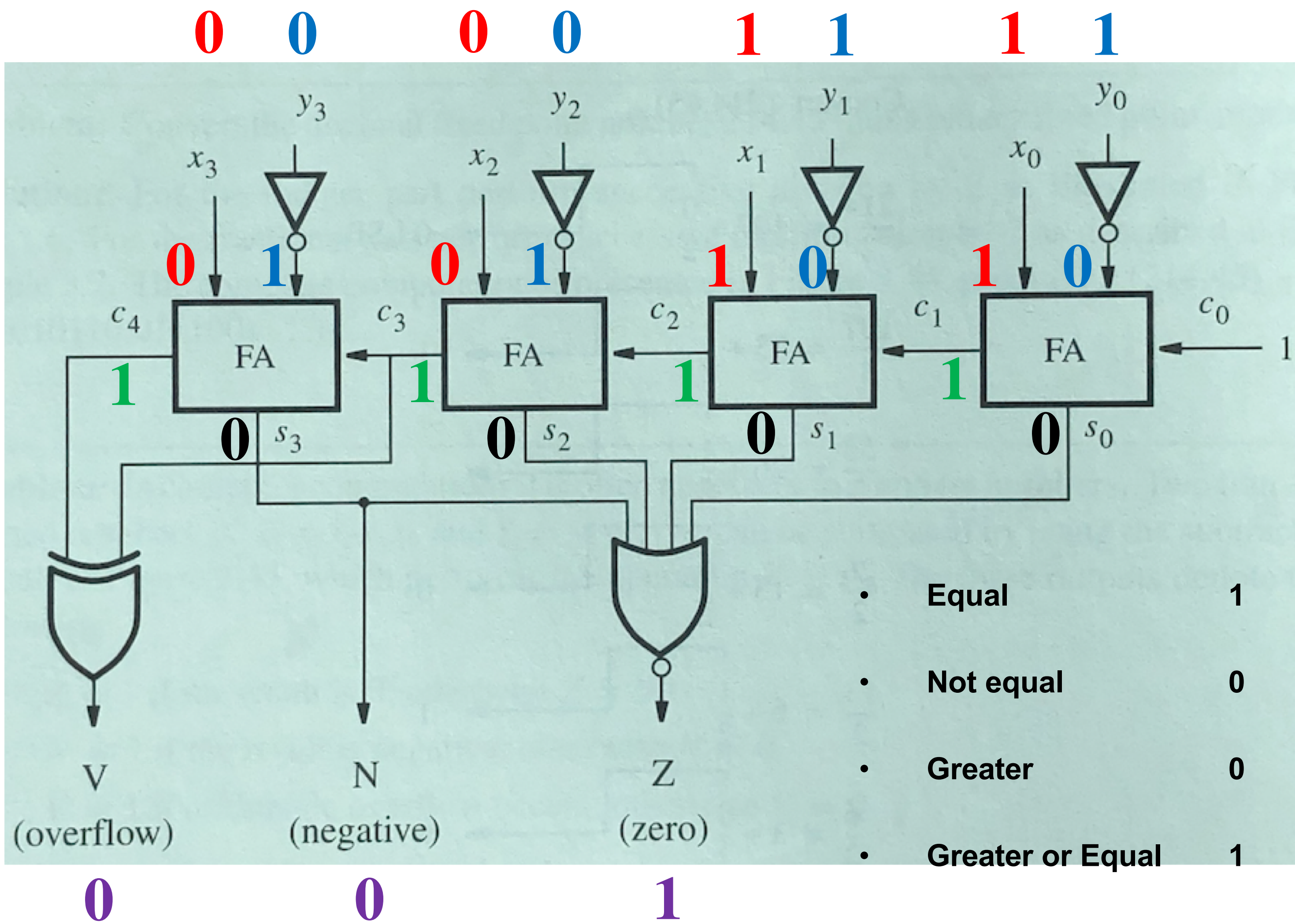
- Equal — ZF
- Not equal — $\overline{\text{ZF}}$
- Greater — $\overline{\text{ZF}}$ • XNOR(NF, OF)
- Greater or Equal — XNOR(NF, OF)
- Less — XOR(NF, OF)
- Less or Equal — ZF + XOR(NF, OF)

Compare 3 with 3: (+3) - (+3)



- Equal 1
- Not equal $\overline{1}$
- Greater $\overline{1}$ • XNOR(0, 0)
- Greater or Equal XNOR(0, 0)
- Less XOR(0, 0)
- Less or Equal 1 + XOR(0, 0)

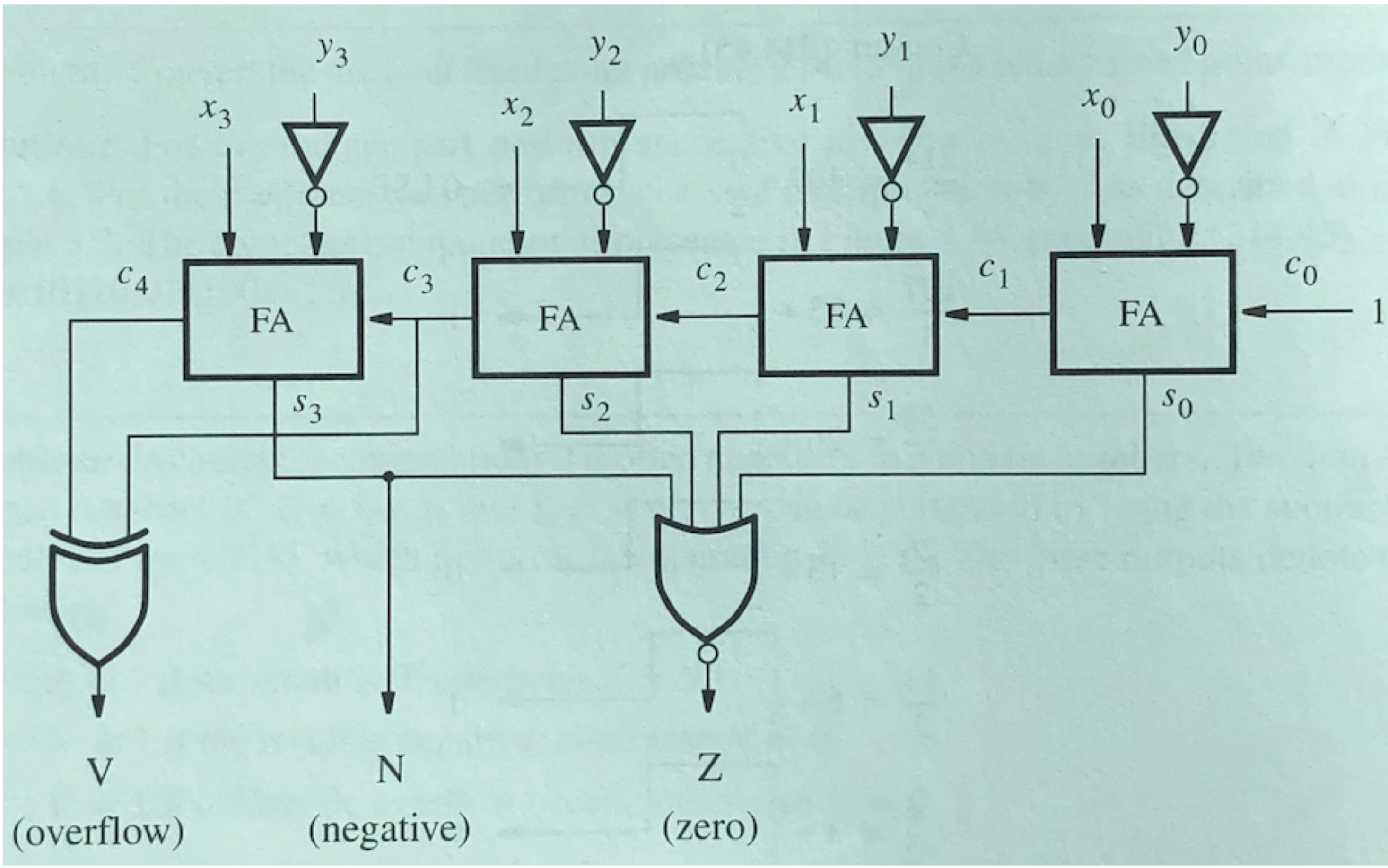
Compare 3 with 3: (+3) - (+3)



- Equal 1
- Not equal 0
- Greater 0
- Greater or Equal 1
- Less 0
- Less or Equal 1

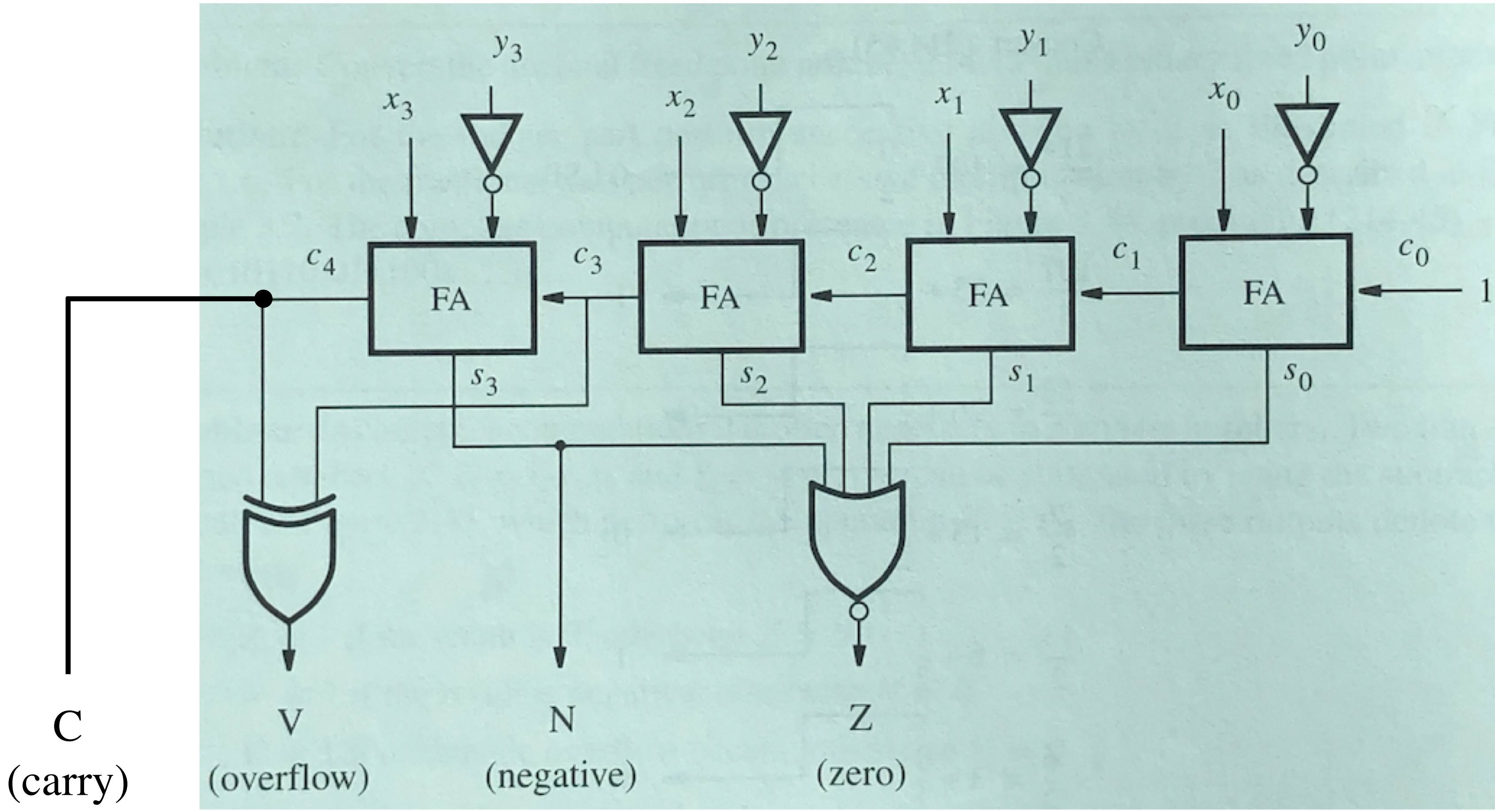
Comparison of Unsigned Numbers

A four-bit comparator circuit

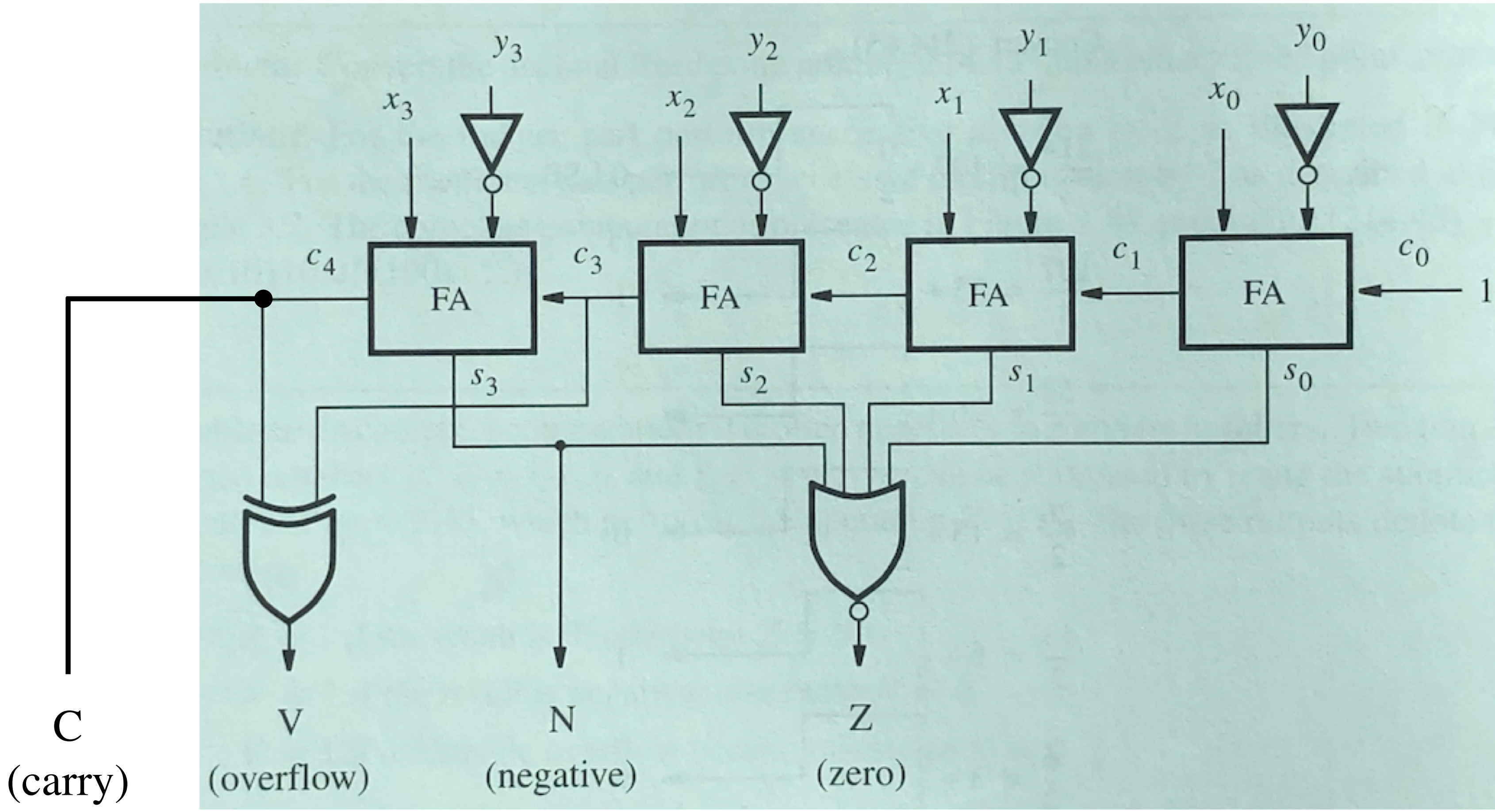


[Figure 3.45 from the textbook]

A four-bit comparator circuit



A four-bit comparator circuit



CF OF NF ZF

alternative names
for the flags

Comparison of Unsigned Numbers

- Equal
- Not equal
- Greater
- Greater or equal
- Less
- Less or Equal

Comparison of Unsigned Numbers

- **Equal**
- **Not equal**
- **Greater / Above**
- **Greater or Equal / Above or Equal**
- **Less / Below**
- **Less or Equal / Below or Equal**

Comparison of Unsigned Numbers

• Equal	ZF = 1
• Not equal	ZF = 0
• Greater	ZF = 0 and CF = 1
• Greater or Equal	CF = 1
• Less	CF = 0
• Less or Equal	ZF = 1 or CF = 0

Comparison of Unsigned Numbers

• Equal	ZF
• Not equal	$\overline{ZF}$
• Greater	$\overline{ZF} \cdot CF$
• Greater or Equal	CF
• Less	$\overline{CF}$
• Less or Equal	$ZF + \overline{CF}$

Comparison of Unsigned Numbers

Equal	ZF
Not equal	$\overline{ZF}$
Above	$\overline{ZF} \cdot CF$
Above or Equal	CF
Below	$\overline{CF}$
Below or Equal	$ZF + \overline{CF}$

Example Problems from Chapter 4

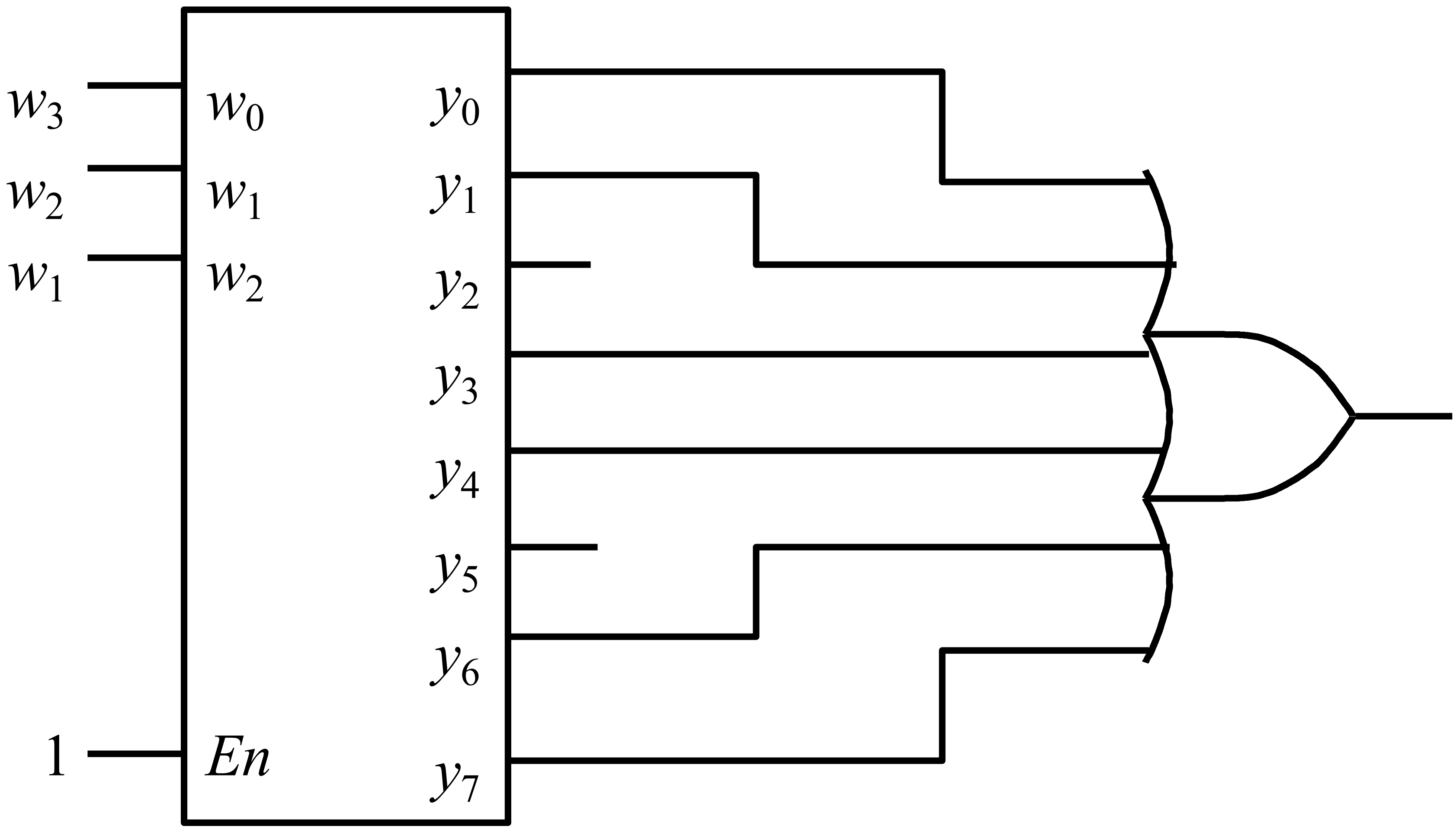
Example 1: SOP vs Decoders

Implement the function

$$f(w_1, w_2, w_3) = \Sigma\, m(0, 1, 3, 4, 6, 7)$$

by using a 3-to-8 binary decoder and one OR gate.

Solution Circuit



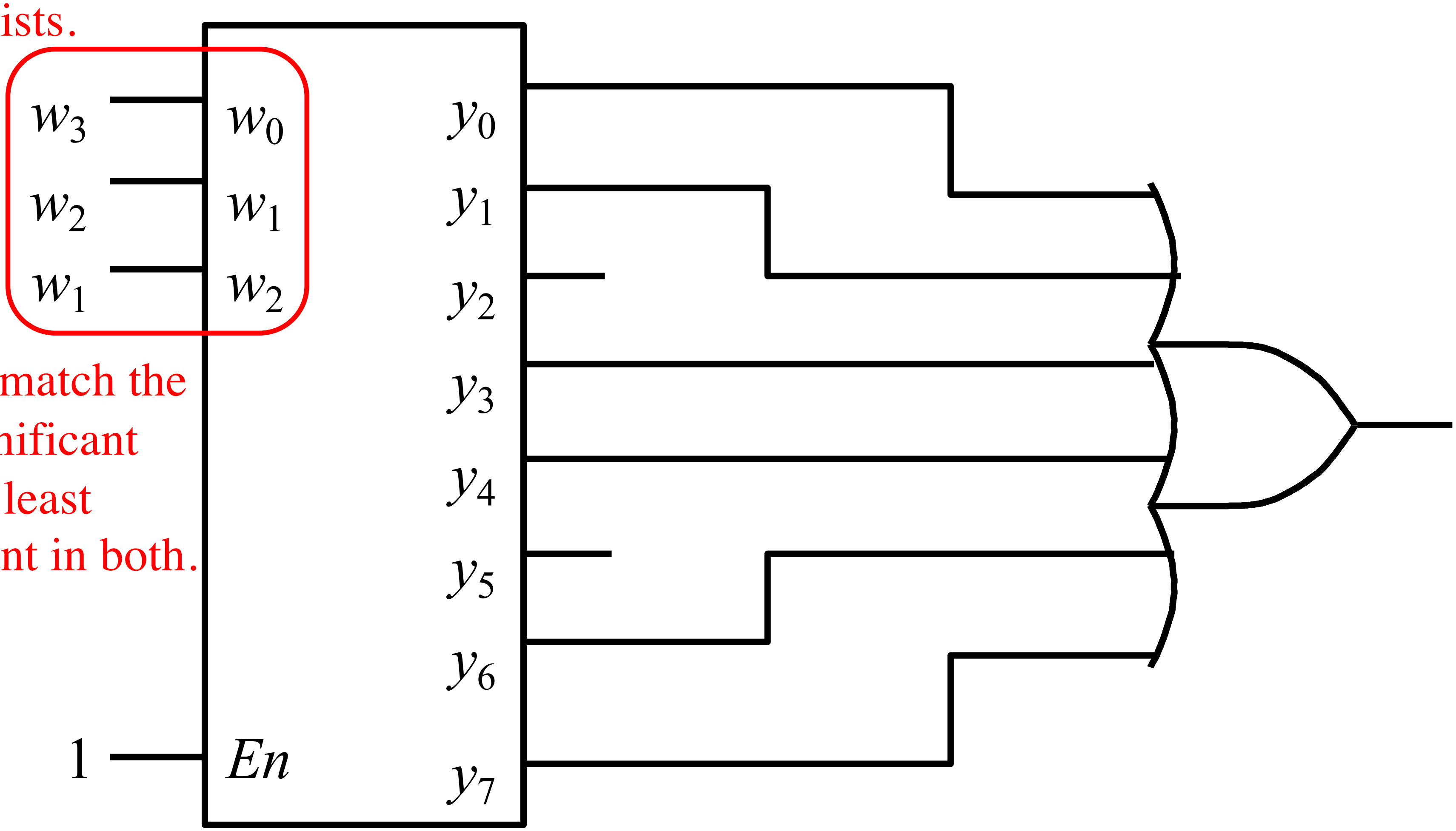
$$f(w_1, w_2, w_3) = \Sigma\, m(0, 1, 3, 4, 6, 7)$$

[Figure 4.44 from the textbook]

Solution Circuit

Notice this swap of variables in the two lists.

Need to match the least significant with the least significant in both.



$$f(w_1, w_2, w_3) = \Sigma\, m(0, 1, 3, 4, 6, 7)$$

[Figure 4.44 from the textbook]

Example 2: Implement an 8-to-3 binary encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

[Figure 4.45 from the textbook]

Example 2: Implement an 8-to-3 binary encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$y_0 = w_1 + w_3 + w_5 + w_7$$
$$y_1 = w_2 + w_3 + w_6 + w_7$$
$$y_2 = w_4 + w_5 + w_6 + w_7$$

[Figure 4.45 from the textbook]

Example 2: Implement an 8-to-3 binary encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$y_0 = \boxed{w_1 + w_3 + w_5 + w_7}$$
$$y_1 = w_2 + w_3 + w_6 + w_7$$
$$y_2 = w_4 + w_5 + w_6 + w_7$$

Example 2: Implement an 8-to-3 binary encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$y_0 = w_1 + w_3 + w_5 + w_7$$
$$y_1 = \boxed{w_2 + w_3 + w_6 + w_7}$$
$$y_2 = w_4 + w_5 + w_6 + w_7$$

Example 2: Implement an 8-to-3 binary encoder

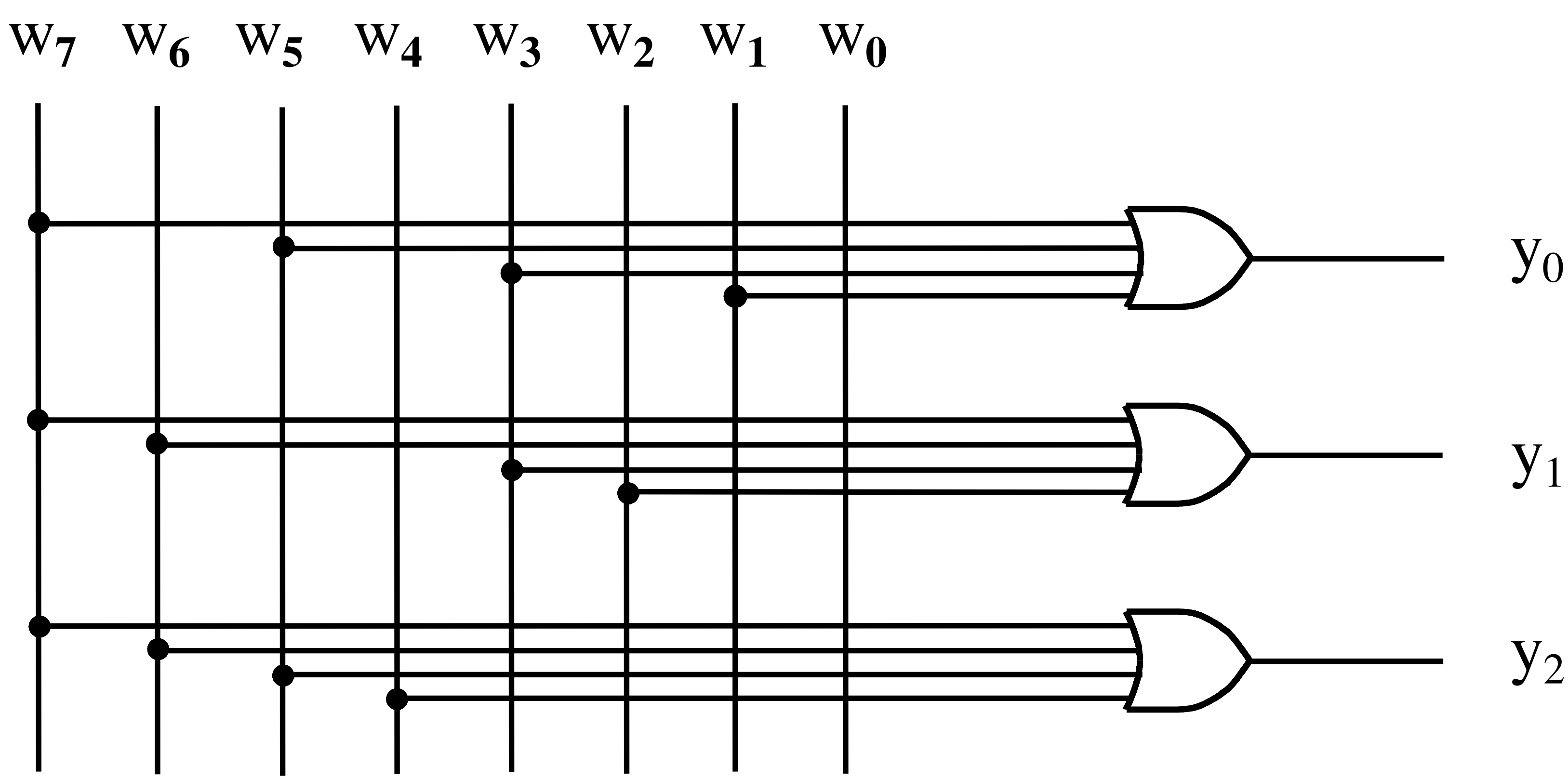
w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$y_0 = w_1 + w_3 + w_5 + w_7$$

$$y_1 = w_2 + w_3 + w_6 + w_7$$

$$y_2 = \boxed{w_4 + w_5 + w_6 + w_7}$$

Circuit for the 8-to-3 binary encoder



$$y_0 = w_1 + w_3 + w_5 + w_7$$
$$y_1 = w_2 + w_3 + w_6 + w_7$$
$$y_2 = w_4 + w_5 + w_6 + w_7$$

Example 3: Implement an 8-to-3 priority encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Example 3: Implement an 8-to-3 priority encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

Example 3: Implement an 8-to-3 priority encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0	z
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	x	0	0	1	1
0	0	0	0	0	1	x	x	0	1	0	1
0	0	0	0	1	x	x	x	0	1	1	1
0	0	0	1	x	x	x	x	1	0	0	1
0	0	1	x	x	x	x	x	1	0	1	1
0	1	x	x	x	x	x	x	1	1	0	1
1	x	x	x	x	x	x	x	1	1	1	1
0	0	0	0	0	0	0	0	d	d	d	0

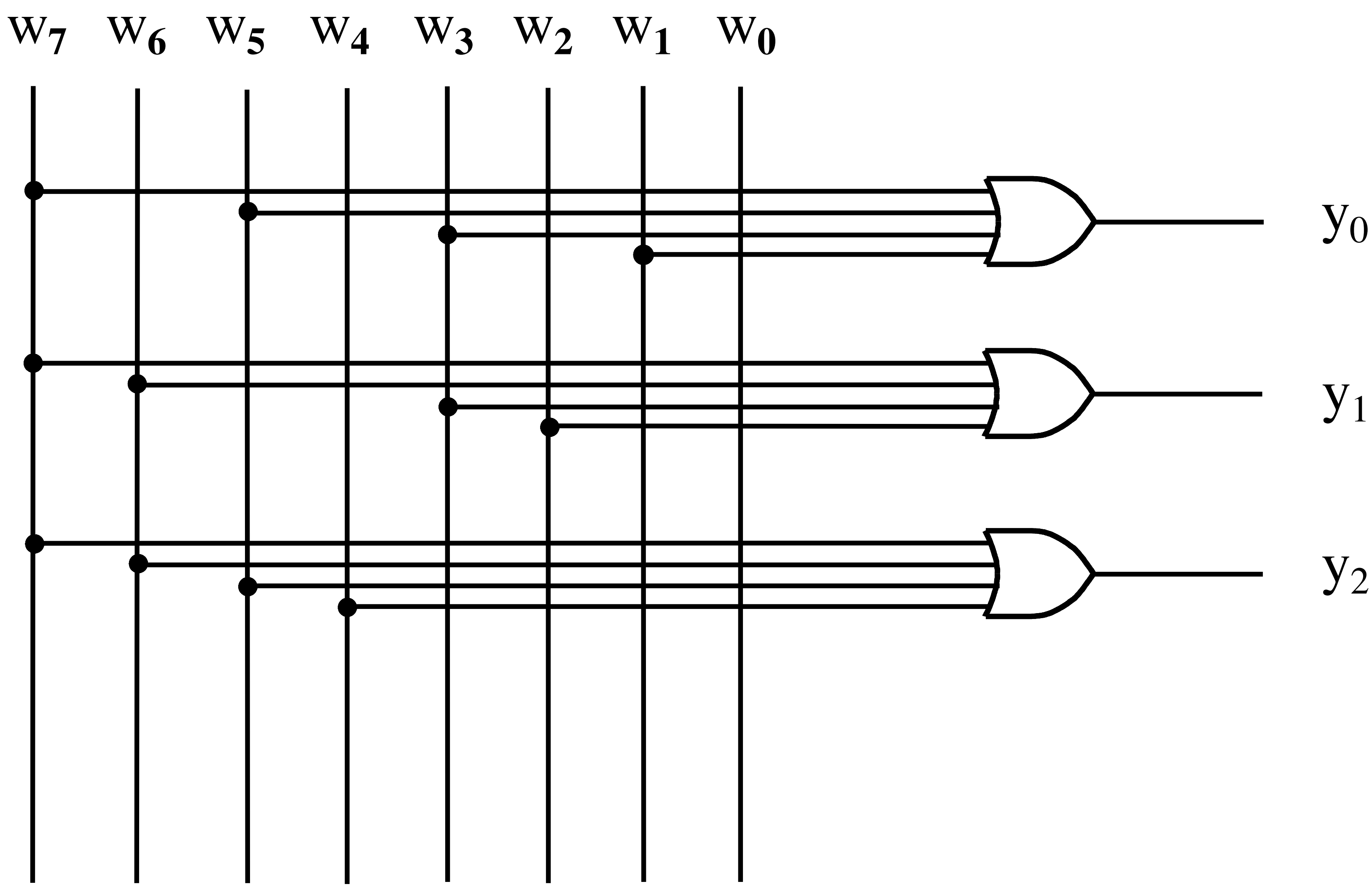
Example 3: Implement an 8-to-3 priority encoder

w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0	z
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	x	0	0	1	1
0	0	0	0	0	1	x	x	0	1	0	1
0	0	0	0	1	x	x	x	0	1	1	1
0	0	0	1	x	x	x	x	1	0	0	1
0	0	1	x	x	x	x	x	1	0	1	1
0	1	x	x	x	x	x	x	1	1	0	1
1	x	x	x	x	x	x	x	1	1	1	1
0	0	0	0	0	0	0	0	d	d	d	0

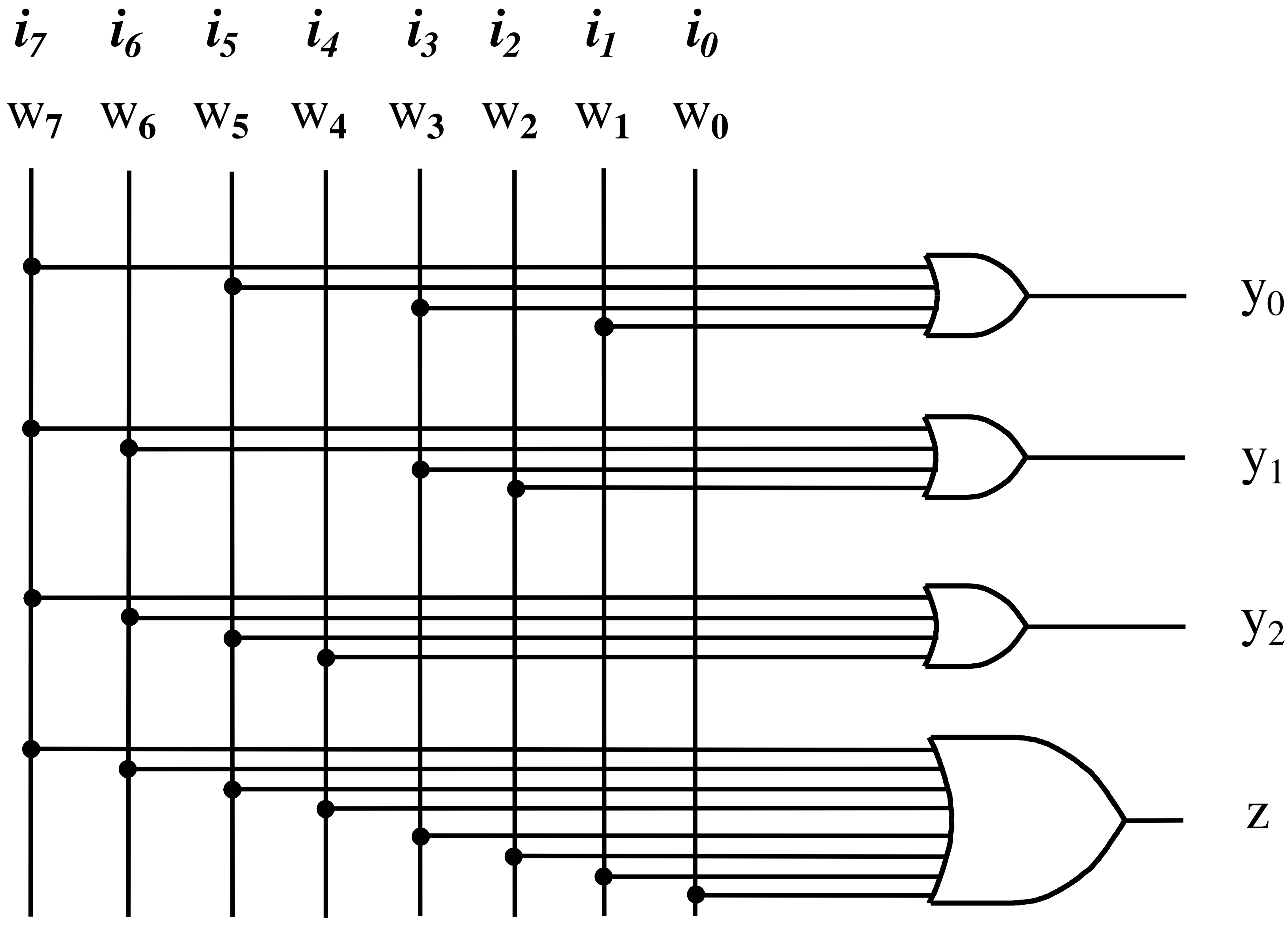
Example 3: Implement an 8-to-3 priority encoder

	w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0	y_2	y_1	y_0	z
$i_0 = \overline{w_7}\,\overline{w_6}\,\overline{w_5}\,\overline{w_4}\,\overline{w_3}\,\overline{w_2}\,\overline{w_1}\,w_0$	0	0	0	0	0	0	0	1	0	0	0	1
$i_1 = \overline{w_7}\,\overline{w_6}\,\overline{w_5}\,\overline{w_4}\,\overline{w_3}\,\overline{w_2}\,w_1$	0	0	0	0	0	0	1	x	0	0	1	1
$i_2 = \overline{w_7}\,\overline{w_6}\,\overline{w_5}\,\overline{w_4}\,\overline{w_3}\,w_2$	0	0	0	0	0	1	x	x	0	1	0	1
$i_3 = \overline{w_7}\,\overline{w_6}\,\overline{w_5}\,\overline{w_4}\,w_3$	0	0	0	0	1	x	x	x	0	1	1	1
$i_4 = \overline{w_7}\,\overline{w_6}\,\overline{w_5}\,w_4$	0	0	0	1	x	x	x	x	1	0	0	1
$i_5 = \overline{w_7}\,\overline{w_6}\,w_5$	0	0	1	x	x	x	x	x	1	0	1	1
$i_6 = \overline{w_7}\,w_6$	0	1	x	x	x	x	x	x	1	1	0	1
$i_7 = w_7$	1	x	x	x	x	x	x	x	1	1	1	1
$z = i_0+i_1+i_2+i_3+i_4+i_5+i_6+i_7$	0	0	0	0	0	0	0	0	d	d	d	0

Circuit for the 8-to-3 binary encoder



Circuit for the 8-to-3 priority encoder



Example 4:Circuit implementation using a multiplexer

Implement the function

$$f(w_1, w_2, w_3, w_4, w_5) = \overline{w}_1\overline{w}_2\overline{w}_4\overline{w}_5 + w_1w_2 + w_1w_3 + w_1w_4 + w_3w_4w_5$$

using a 4-to-1 multiplexer

Some Boolean Algebra Leads To

$$\overline{w_1}\,\overline{w_2}\,\overline{w_4}\,\overline{w_5} + w_1w_2 + w_1w_3 + w_1w_4 + w_3w_4w_5$$

$$\overline{w_1}\,\overline{w_4}\,(\overline{w_5}\,\overline{w_2}) + w_4\,(w_3w_5) + w_1\,(w_2 + w_3) + w_1w_4\,(1)$$

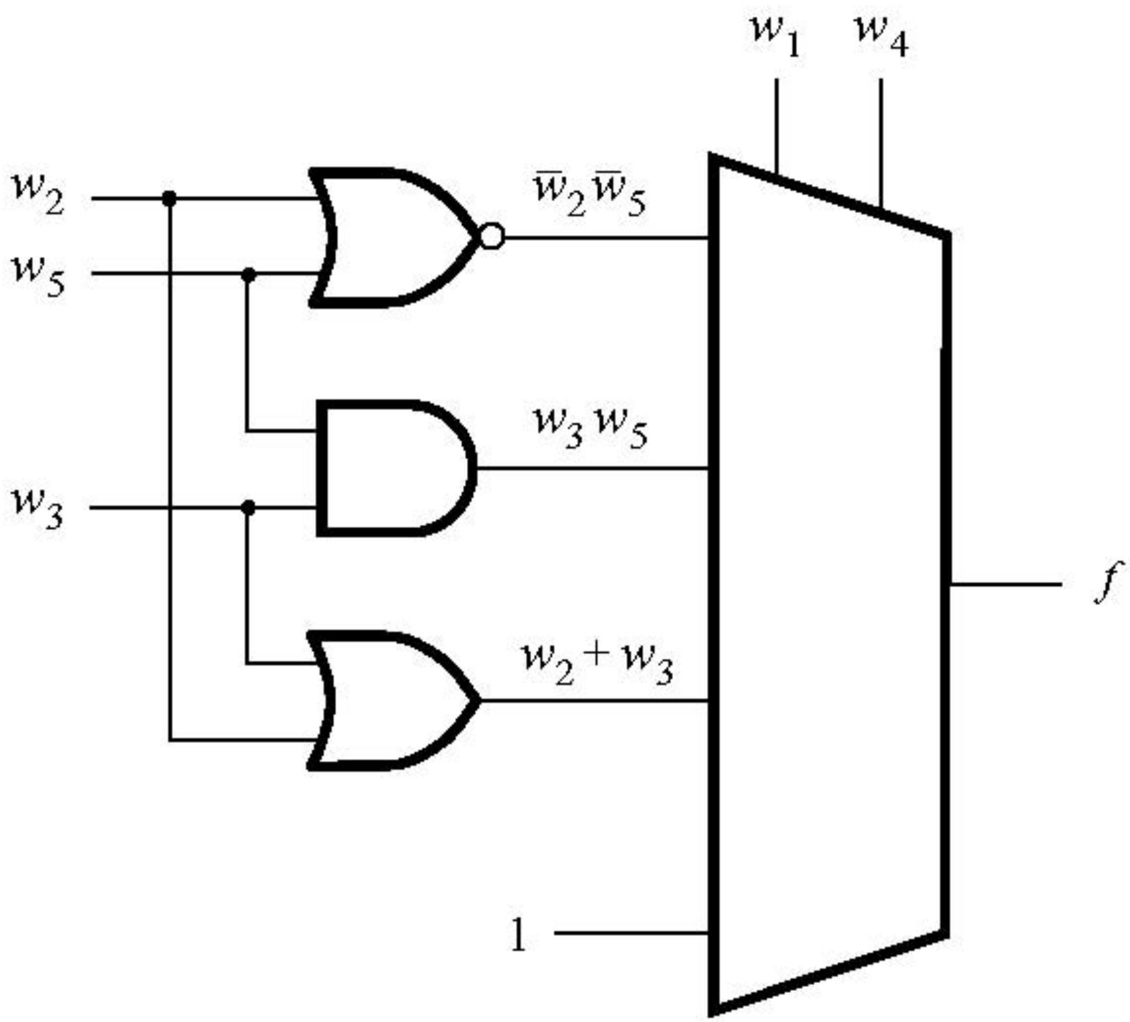
$$\overline{w_1}\,\overline{w_4}\,(\overline{w_5}\,\overline{w_2}) + (\,\overline{w_1}+w_1)w_4\,(w_3w_5) + w_1(\,\overline{w_4}+w_4)\,(w_2 + w_3) + w_1w_4\,(1)$$

$$\overline{w_1}\,\overline{w_4}\,(\overline{w_5}\,\overline{w_2}) + \overline{w_1}w_4\,(w_3w_5) + w_1\overline{w_4}\,(w_2 + w_3) + w_1w_4\,(\,w_3w_5 + (w_2+w_3) + 1)$$

$$\overline{w_1}\,\overline{w_4}\,(\overline{w_5}\,\overline{w_2}) + \overline{w_1}w_4\,(w_3w_5) + w_1\overline{w_4}\,(w_2 + w_3) + w_1w_4\,(1)$$

Note that the split is by w_1 and w_4, not w_1 and w_2

Solution Circuit

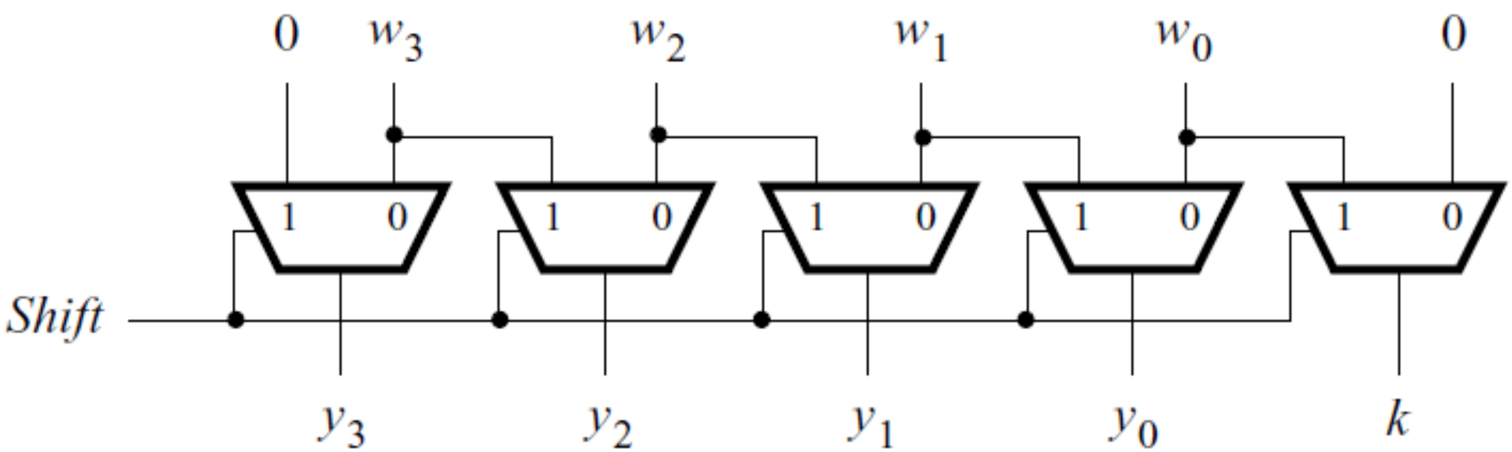


$$\overline{w}_1\overline{w}_4\,(\overline{w}_5\,\overline{w}_2) + \overline{w}_1 w_4\,(w_3 w_5) + w_1\overline{w}_4\,(w_2 + w_3) + w_1 w_4\,(1)$$

[Figure 4.46 from the textbook]

Some Final Things from Chapter 4

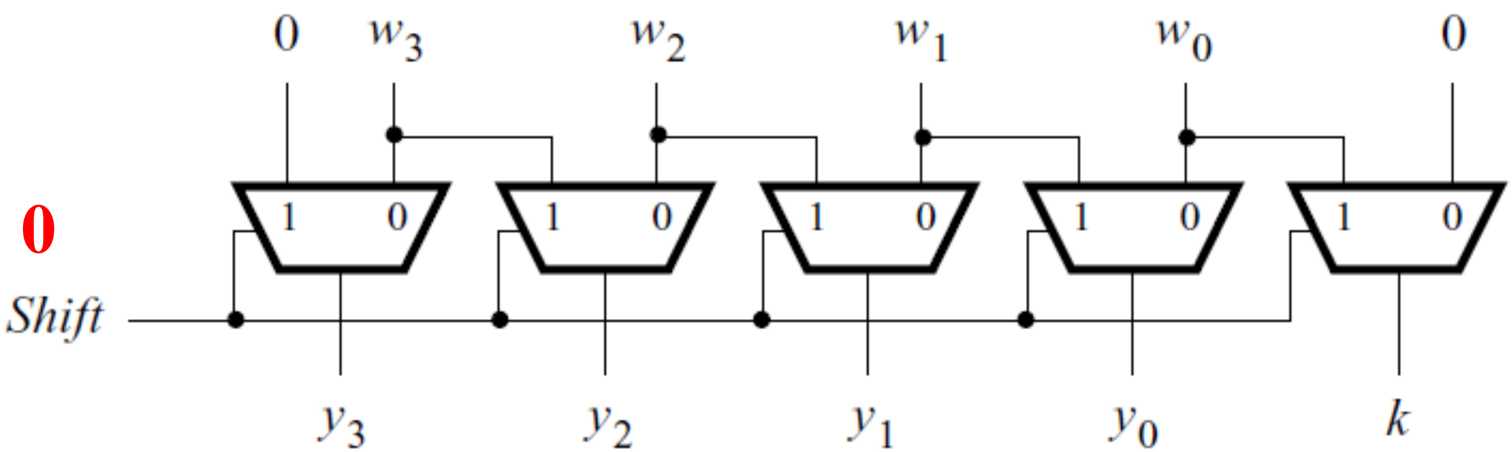
A shifter circuit



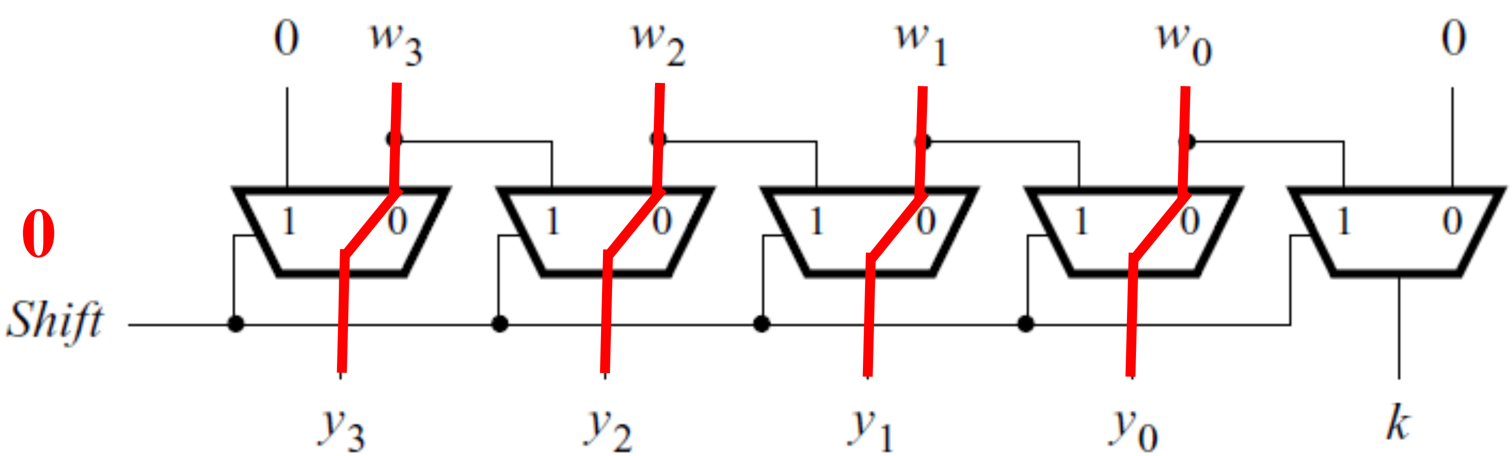
[Figure 4.50 from the textbook]

A shifter circuit

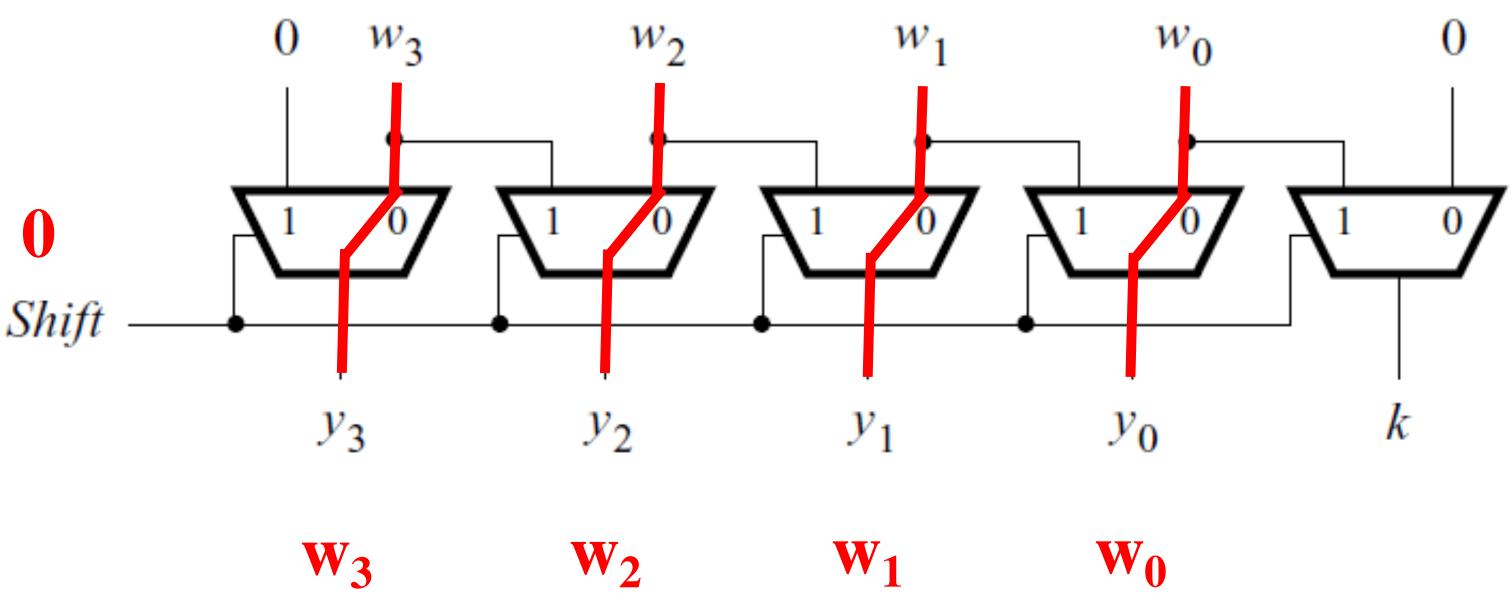
0



A shifter circuit

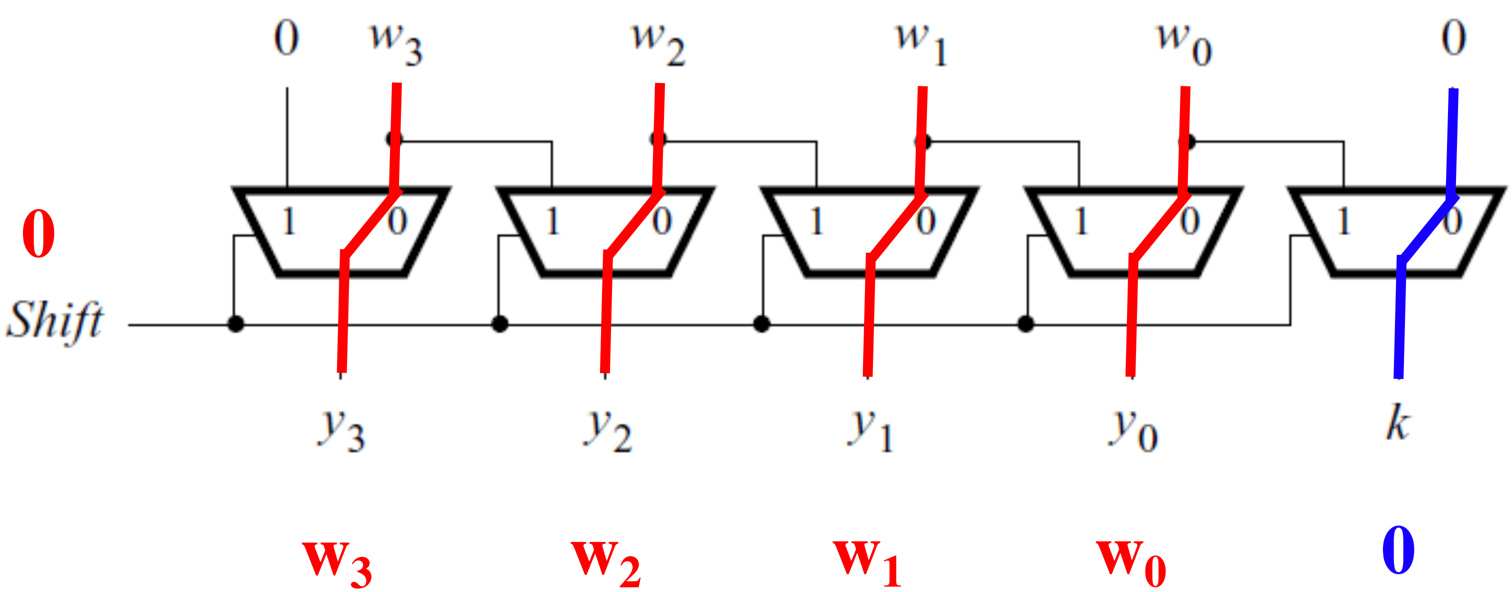


A shifter circuit



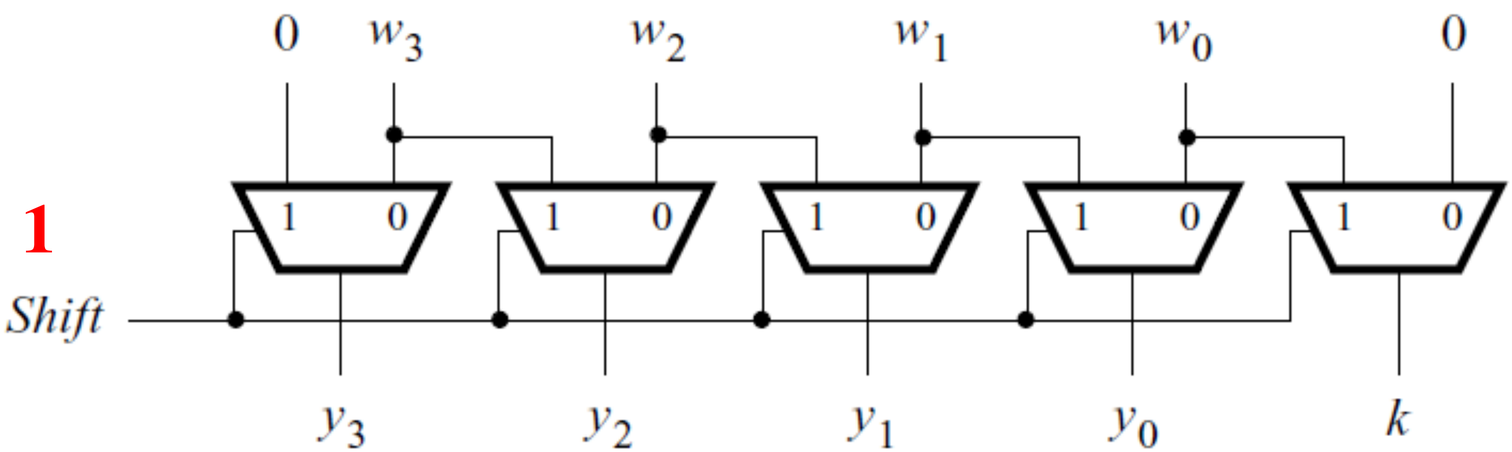
No shift in this case.

A shifter circuit

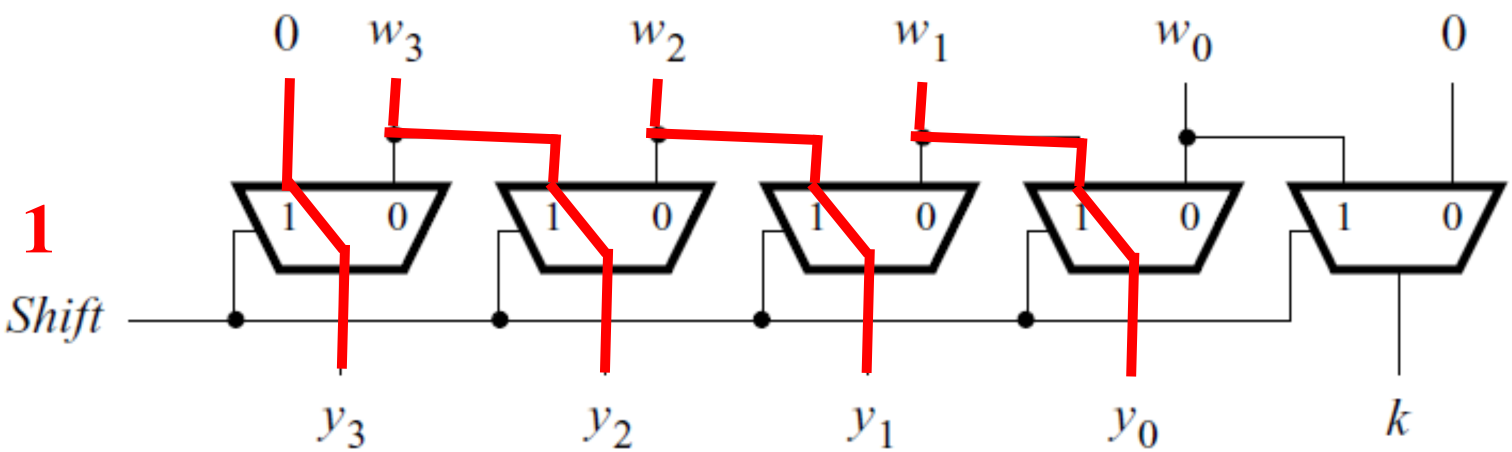


No shift in this case.

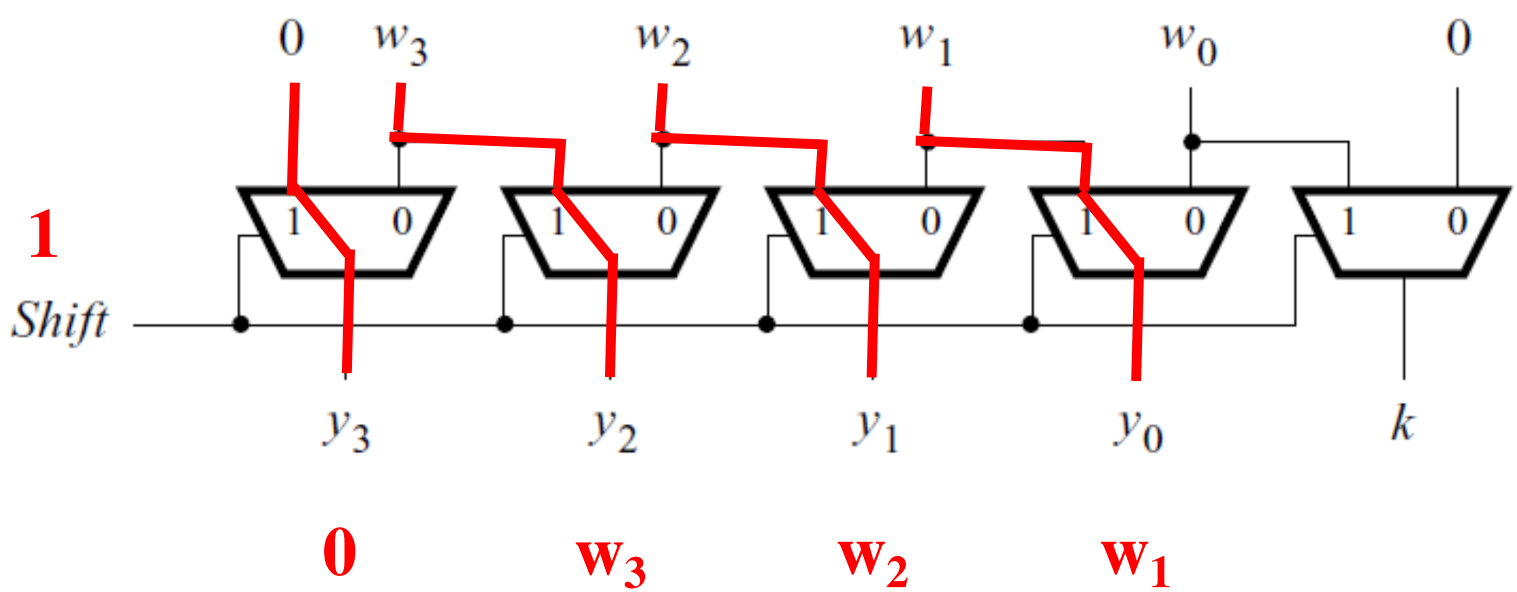
A shifter circuit



A shifter circuit

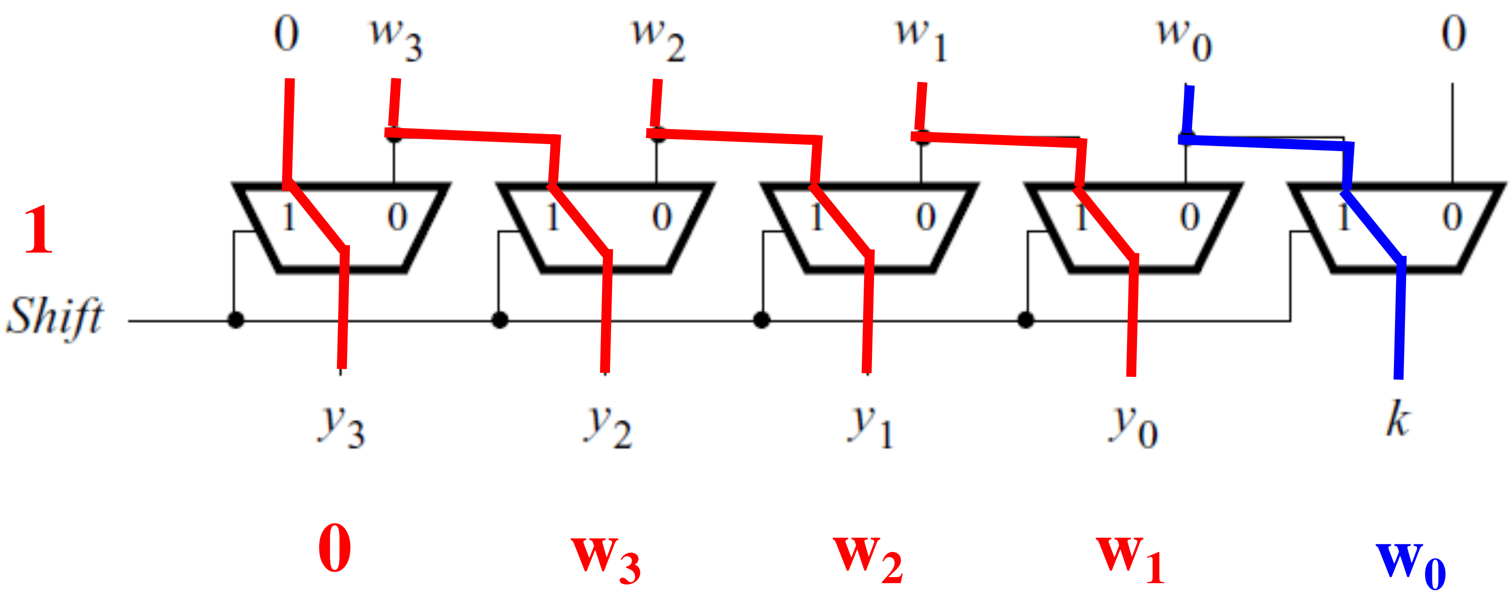


A shifter circuit



Shift to the right by 1 bit

A shifter circuit

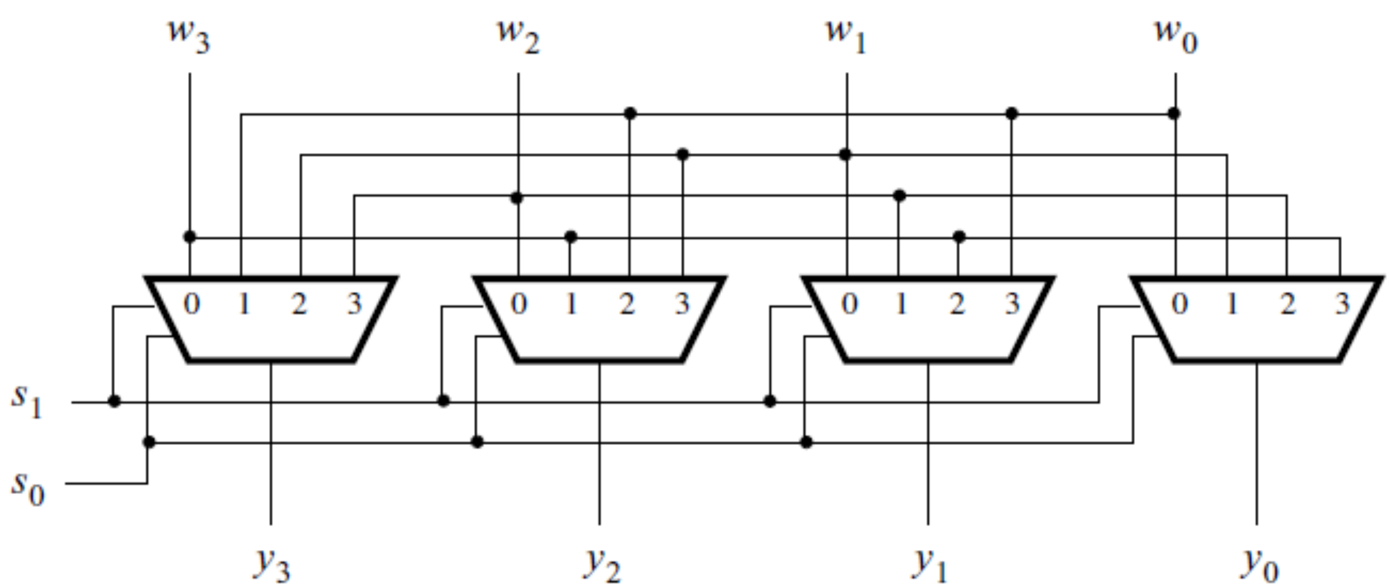


Shift to the right by 1 bit

A barrel shifter circuit

s_1	s_0	y_3	y_2	y_1	y_0
0	0	w_3	w_2	w_1	w_0
0	1	w_0	w_3	w_2	w_1
1	0	w_1	w_0	w_3	w_2
1	1	w_2	w_1	w_0	w_3

(a) Truth table



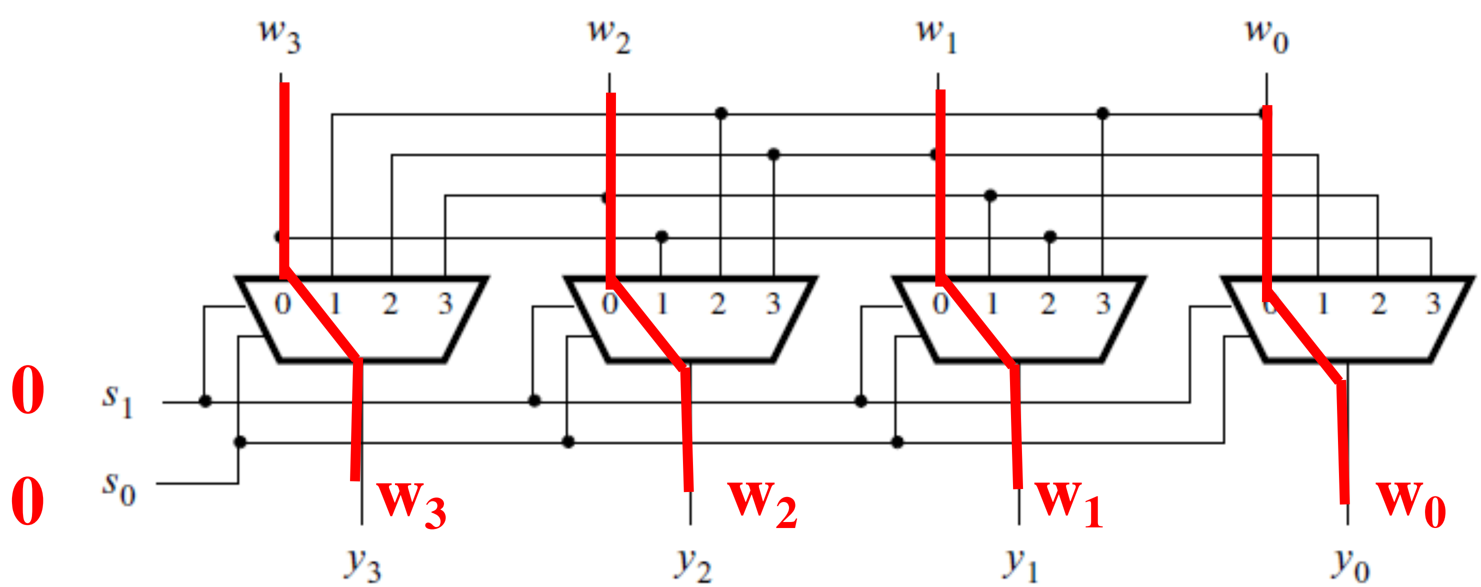
(b) Circuit

[Figure 4.51 from the textbook]

A barrel shifter circuit

s_1	s_0	y_3	y_2	y_1	y_0
0	0	w_3	w_2	w_1	w_0
0	1	w_0	w_3	w_2	w_1
1	0	w_1	w_0	w_3	w_2
1	1	w_2	w_1	w_0	w_3

(a) Truth table



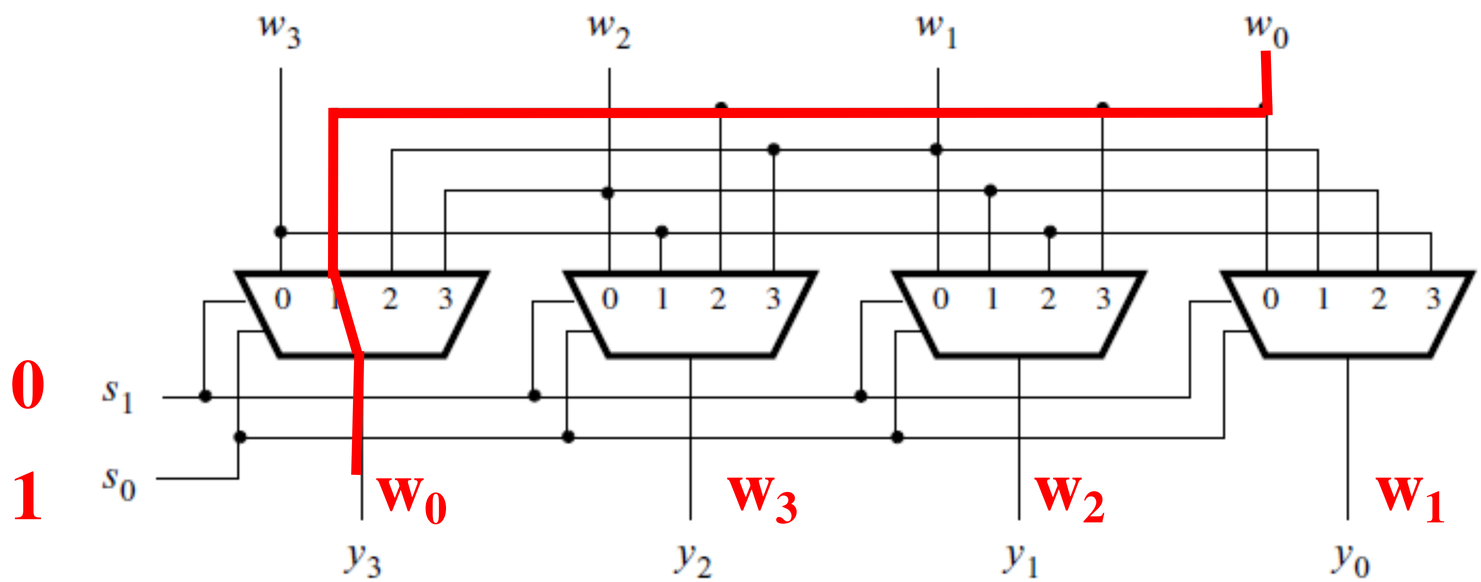
(b) Circuit

[Figure 4.51 from the textbook]

A barrel shifter circuit

s_1	s_0	y_3	y_2	y_1	y_0
0	0	w_3	w_2	w_1	w_0
0	1	w_0	w_3	w_2	w_1
1	0	w_1	w_0	w_3	w_2
1	1	w_2	w_1	w_0	w_3

(a) Truth table



(b) Circuit

[Figure 4.51 from the textbook]

Questions?

THE END