CprE 281 HW10
ELECTRICAL AND COMPUTER
ENGINEERING
IOWA STATE UNIVERSITY

Basic Design Steps, State-Assignment Problems, Moore & Mealy Machines
Assigned Date: Eleventh Week
Finish by Nov. 08, 2021

P1 (15 points): We want to design a circuit with input W and output Z, where Z will be equal 1 if, for the last three clock cycles, W has been 1.

  a. Draw a state diagram for a Moore Finite State Machine (FSM) that implements this circuit in four states, specified as follows:

RESET

| S-0 : 0 | | S-I : 0 | | S-II : 0 | | S-III : 1 |

  b. Complete a state table for the above state diagram with the state assignments as shown below for state variables D1 and D0.

	W=0	W=1	Z
S-0 : 00			
S-I : 01			
S-II : 10			
S-III : 11			

  c. Use K-maps to show that the output and next-state variables can be expressed as:

$$D_1^{new} = (w)(D_1 + D_0)$$
$$D_0^{new} = (w)(D_1 + \overline{D_0})$$
$$z = D_1 D_0$$

  d. Consider an alternative state assignment where the states were encoded as:
      S-0 = 00,   S-I = 01,   S-II = 11,   S-III = 10.
      Use K-maps to show that the output and next-state variables with this new encoding can be expressed as:

$$D_1^{new} = (w)(D_1 + D_0)$$
$$D_0^{new} = w\overline{D_1}$$
$$z = D_1 \overline{D_0}$$

  e. Draw the circuit for this FSM (developed in part d) using only DFFs, AND gates, and one OR gate (Do not use any NOT gates).

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P2 (15 points): Draw the state diagram for a Moore FSM that has a 1-bit input P and a 1-bit output Q. P will be either 1 or 0 on any particular clock cycle. Q=0 if P has been 1 for an even number of clock cycles; Q=1 if P has been 1 for an odd number of clock cycles.

a. Draw the state diagram for this Moore FSM.
b. Draw the state table for this FSM.
c. Draw a state assigned table for this FSM. The state should be the same as the output: Q.
d. Draw the truth table for this FSM's next-state variable.
e. Derive the expression for the next state variable and the output Q.
f. Draw the circuit for this FSM. If done properly, the circuit you create will implement a component that you have seen before. What component have you implemented?

P3. (20 points) Design a 4-bit register with both shift and parallel load features. The inputs of the register include a 2-bit control code X Y, a 4-bit input value I3 I2 I1 I0, and a clock signal. The outputs of the register are the 4 bits Q3 Q2 Q1 Q0 corresponding to the value stored in the register. You are allowed to use any number of D flip-flops, muxes of any size, decoders and encoders of any sizes, AND gates, OR gates, and NOT gates. (Notice that you do not need all of them.) The operations of the register are defined below:

X Y   Operation
0 0   Hold the current value stored (i.e., Q3 Q2 Q1 Q0 are not changed)
0 1   Shift right (i.e., new Q3=I3, new Q2=Q3, new Q1=Q2, new Q0=Q1)
1 0   Shift left (i.e., new Q3=Q2, new Q2=Q1, new Q1=Q0, new Q0=I0)
1 1   Load new date (i.e., new Q3=I3, new Q2=I2, new Q1=I1, new Q0=I0)

P4. (10 points) The circuit below looks like a counter. What is the sequence that this circuit counts-in?
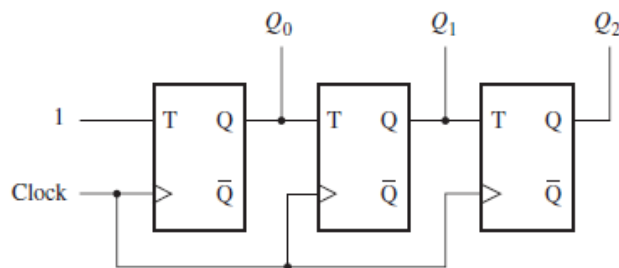
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P5. (15 points) Design a 4-bit asynchronous up/down-counter with Enable using T flip-flops and any combinational circuit devices. The direction of the counter is controlled by a 1-bit signal U. If U=1, the counter will count up. If U=0, the counter will count down. The counting can be enabled/disabled by a 1-bit signal E. If E=1, the counter will count whenever there is up-going clock edge. If E=0, the counter will keep the same value stored.

P6. (15 points) Design a shifter circuit which can shift a four-bit input vector, W = w3w2w1w0, one bit-position to the right when the control signal Right is equal to 1, and one bit-position to the left when the control signal Left is equal to 1.
When Right = Left = 0, the output of the circuit should be the same as the input vector. Assume that the condition Right = Left = 1 will never occur.

P7.* (10 points) Design a register file with four 2-bit registers that has two write ports and two read ports. Describe your design in 5-6 sentences. Then draw the circuit diagram. Please use different colors for the wires to make it easy to trace them.

Hint 1: There are two input buses (each 2-bit wide) that provide the input data. One bus for each write port. And two output buses (again, each is 2-bit wide).

Hint 2: Each write port is controlled with a 2-to-4 decoder with enable. The two inputs are the write address. The enable input acts as write enable.

Hint 3: If both write ports select the same register for writing, then the first write port takes precedence and only the data on its corresponding input bus will be written to that register.