Name and Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**PRELAB:**

**Q1.** Consider the Verilog code in section 3.0. Briefly explain how the **always @** structure works.

**Q2**. Write the Verilog code for ***lab4step1***. Use the example code given in Section 3.0 and make the necessary changes.

**Q3**. Read Section 4.0 and fill in the Truth Table for ***lab4step2***.

|  |  |
| --- | --- |
| **Inputs** | **Outputs** |
| **M** | **T** | **H** | **P** | **E** | **F** | **AC** |
| 0 | 0 | 0 | 0 |  |  |  |
| 0 | 0 | 0 | 1 |  |  |  |
| 0 | 0 | 1 | 0 |  |  |  |
| 0 | 0 | 1 | 1 |  |  |  |
| 0 | 1 | 0 | 0 |  |  |  |
| 0 | 1 | 0 | 1 |  |  |  |
| 0 | 1 | 1 | 0 |  |  |  |
| 0 | 1 | 1 | 1 |  |  |  |
| 1 | 0 | 0 | 0 |  |  |  |
| 1 | 0 | 0 | 1 |  |  |  |
| 1 | 0 | 1 | 0 |  |  |  |
| 1 | 0 | 1 | 1 |  |  |  |
| 1 | 1 | 0 | 0 |  |  |  |
| 1 | 1 | 0 | 1 |  |  |  |
| 1 | 1 | 1 | 0 |  |  |  |
| 1 | 1 | 1 | 1 |  |  |  |

Pre-lab TA Initials: \_\_\_\_\_\_\_\_\_

**LAB:**

 **3.0** Use the hardware results to fill in the truth table for ***lab4step1.***

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Farmer** | **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

 ModelSim results demonstrate correct code. TA Initials: \_\_\_\_\_\_\_\_\_

**4.0**  Demonstrate ModelSim results for correct A/C code. TA Initials: \_\_\_\_\_\_\_\_\_