



CprE 281: Digital Logic

Instructor: Alexander Stoytchev

<http://www.ece.iastate.edu/~alexs/classes/>

Logic Gates

*CprE 281: Digital Logic
Iowa State University, Ames, IA
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Administrative Stuff

- **HW1 is out. It is due on Monday Aug 30 @ 4pm.**
- **Submit it as a PDF upload on Canvas before the deadline.**
- **You can write the solutions on paper and then scan the pages to make ****one**** PDF file.**
- **No late homeworks will be accepted.**
- **Please write clearly on the first page:**
 - your name
 - student ID
 - lab section number

Labs Next Week

- Please download and read the lab assignment for next week before you go to your lab section.
- https://www.ece.iastate.edu/~alexs/classes/2021_Fall_281/labs/Lab_01/
- You must **print and complete** the prelab **before** you go to the lab.
- The TAs will check your prelab answers at the **beginning of the recitation**. If you don't have it done you'll lose 20% of the lab grade for that lab.

CprE 281: Digital Logic

Fall 2021, 4:25 - 5:15 p.m. (Mondays, Wednesdays, and Fridays)

LeBaron Hall, Room 1210

Instructor: [Alexander Stoytchev](#)

- [Syllabus](#)
- [Class Schedule \(Tentative\)](#)
- [Lecture Notes](#) (also in [PDF](#))
- [Labs](#)
- [Recitations](#)

- [Extra Readings](#)

- [Verilog Stuff](#)
- [Verilog Reference](#)

- [i281 CPU](#)

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https://www.ece.iastate.edu/~alexs/classes/2021_Fall_281/labs/

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|  Lab_02/ | 27-Aug-2021 14:09 | - | |

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|  CPRE281_LAB01(Answer_Sheet).docx | 27-Aug-2021 14:02 | 26K | |
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|  CPRE281_LAB01.docx | 27-Aug-2021 14:04 | 1.9M | |
|  CPRE281_LAB01.pdf | 27-Aug-2021 14:04 | 1.4M | |
|  lab1.zip | 27-Aug-2021 13:56 | 5.4M | |







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|  lab1.zip | 27-Aug-2021 13:56 | 5.4M | |

Print this file,
complete the prelab,
and bring it with you
to the lab.

Index of /~alexs/classes/2021_Fall_281/labs/Lab_01

| <u>Name</u> | <u>Last modified</u> | <u>Size</u> | <u>Description</u> |
|--|----------------------|-------------|--------------------|
|  Parent Directory | | - | |
|  CPRE281_LAB01(Answer_Sheet).docx | 27-Aug-2021 14:02 | 26K | |
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|  CPRE281_LAB01.pdf | 27-Aug-2021 14:04 | 1.4M | |
|  lab1.zip | 27-Aug-2021 13:56 | 5.4M | |

This is the same,
but in PDF format.

Name and Student ID: _____ Lab Section: _____

Date: _____

PRELAB:

Q1. Fill in the Truth Table below for an AND gate:

| A | B | C |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Q2. What does the .bdf file extension stand for?

Q3. What is the name of the FPGA on the DE2-115 board?

TA Initials: _____

LAB:

2.0 Fill in the Truth Table for *lab1step1*:

| A | B | C |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Logic Expression: _____

This is the prelab
for lab #1.

Quartus Simulation TA Initials: _____ Questa ModelSim TA Initials: _____

4.0 Fill in the Truth Table for *lab1step2*:

| W | X | Y | Z |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

Logic Expression: _____

TA Initials: _____

4.0 Fill in the Truth Table for *lab1step3*:

| A | B | C | F |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

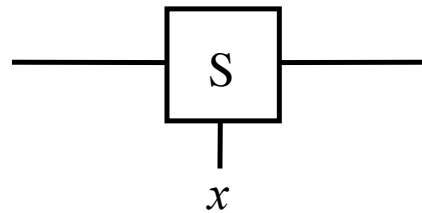
Logic Expression: _____

TA Initials: _____

A Binary Switch

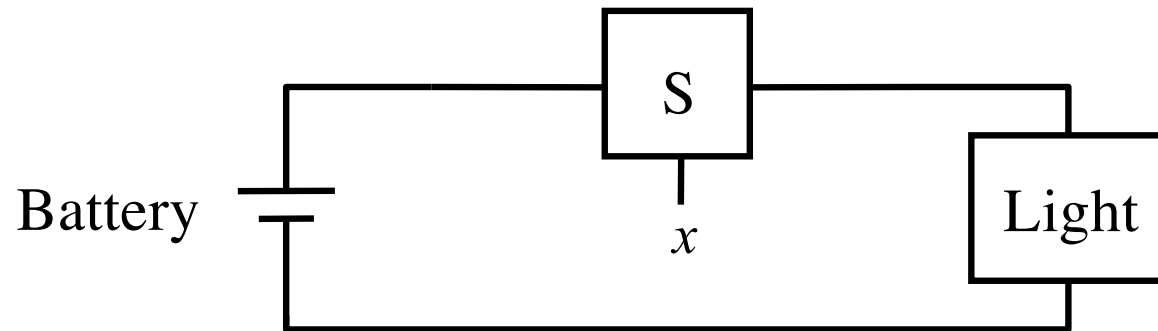


(a) Two states of a switch



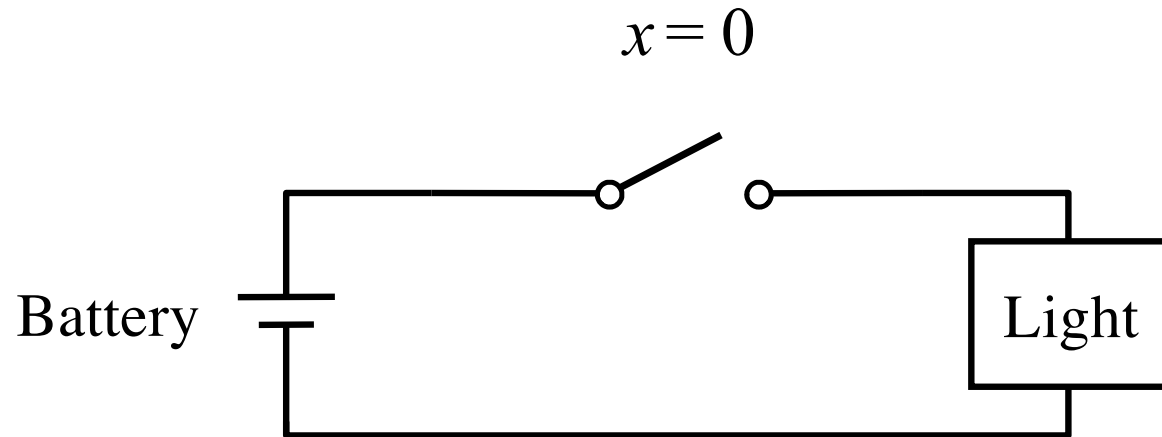
(b) Symbol for a switch

A Light Controlled by a Switch



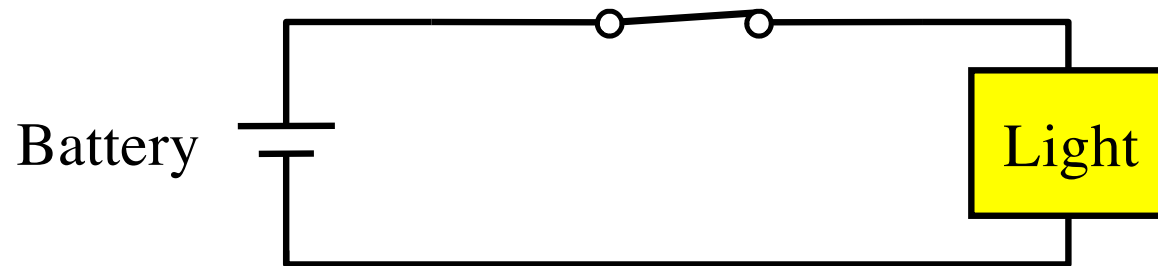
(a) Simple connection to a battery

A Light Controlled by a Switch

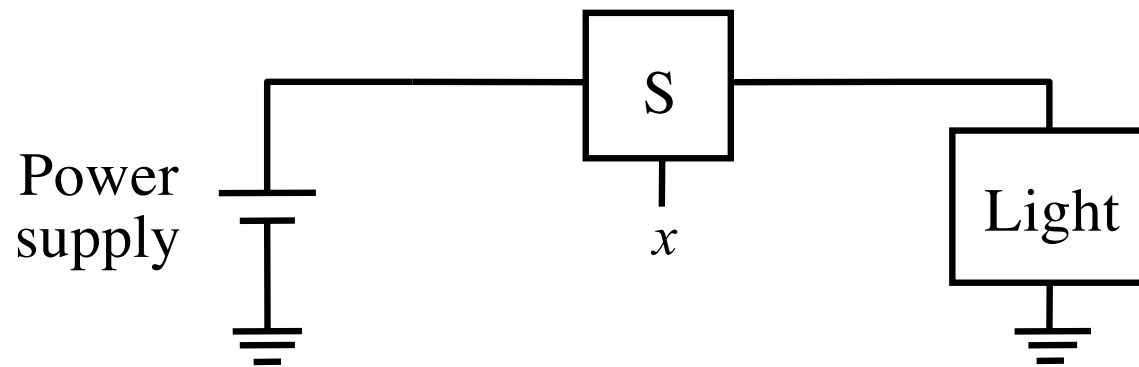


A Light Controlled by a Switch

$$x = 1$$

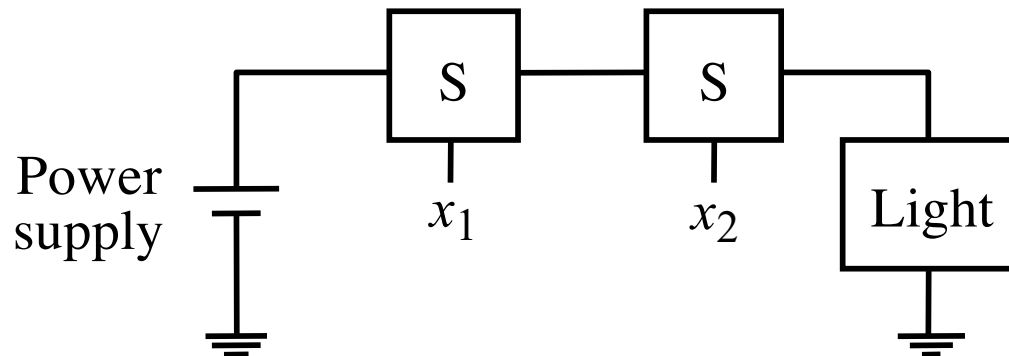


A Light Controlled by a Switch

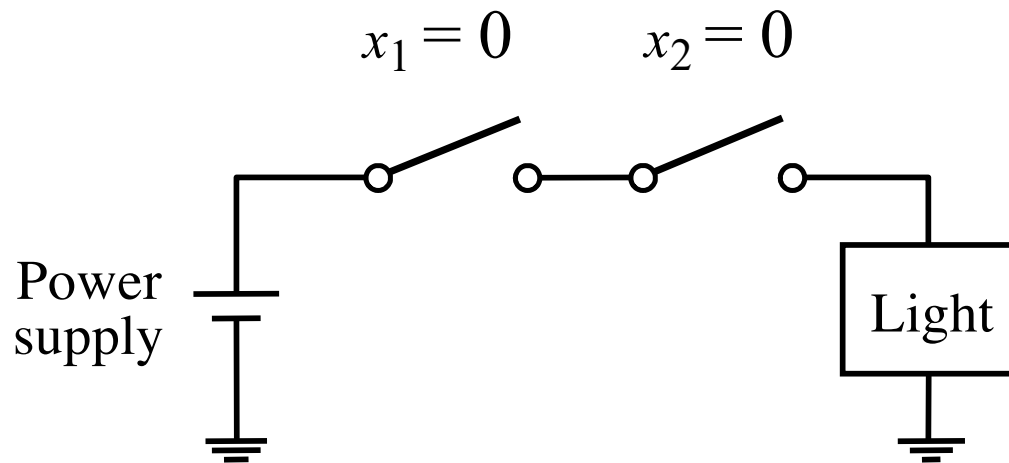


(b) Using a ground connection as the return path

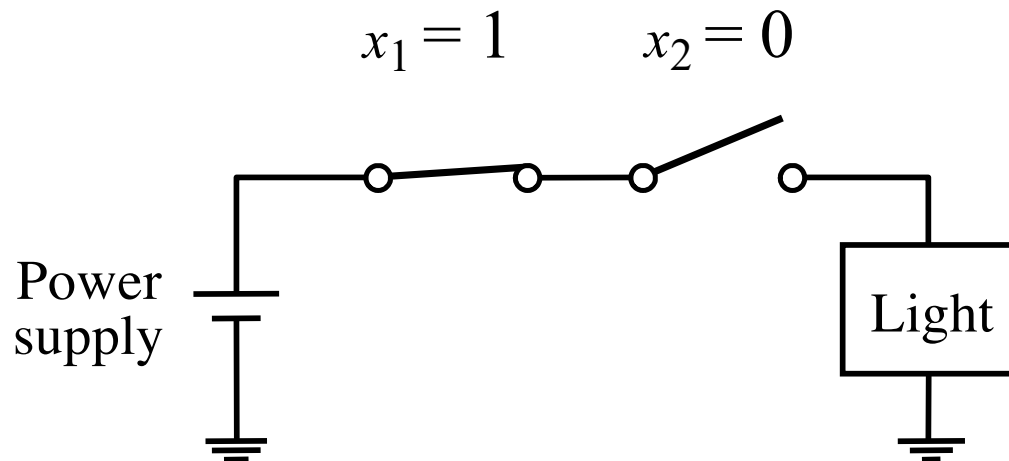
The Logical AND function (series connection of the switches)



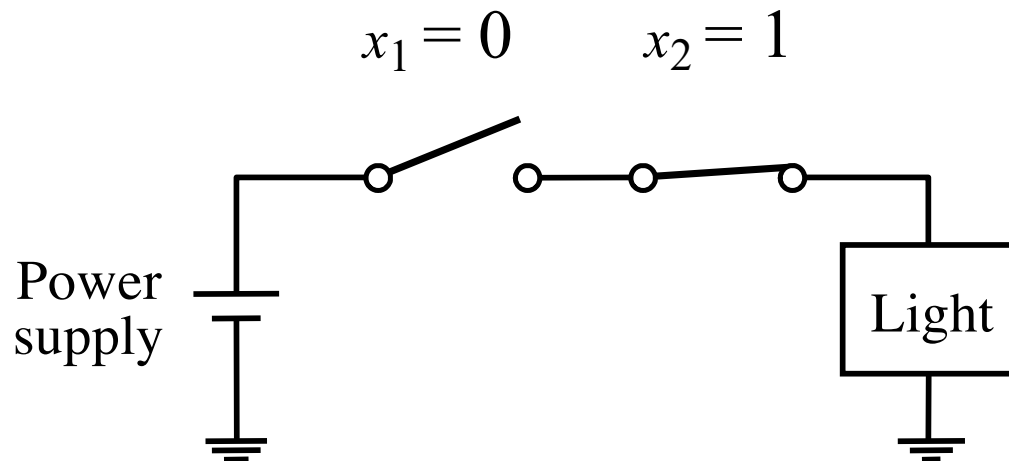
The Logical AND function (series connection of the switches)



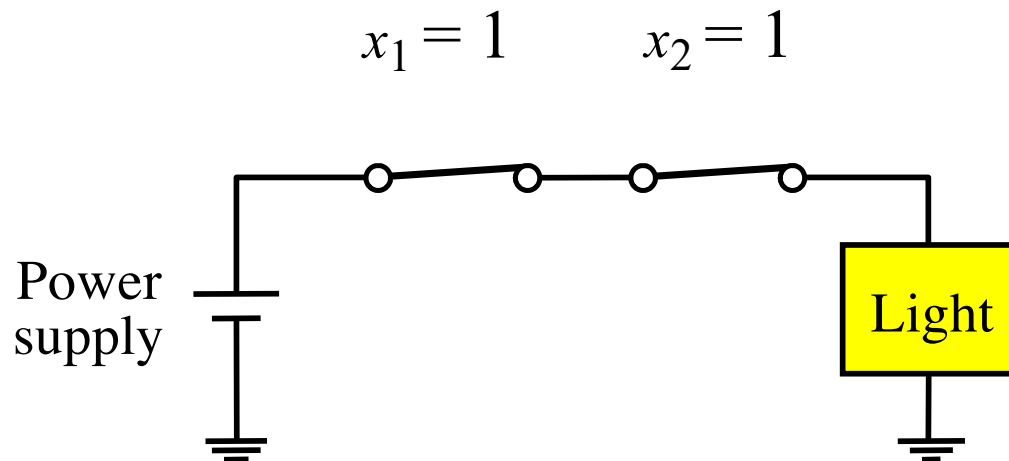
The Logical AND function (series connection of the switches)



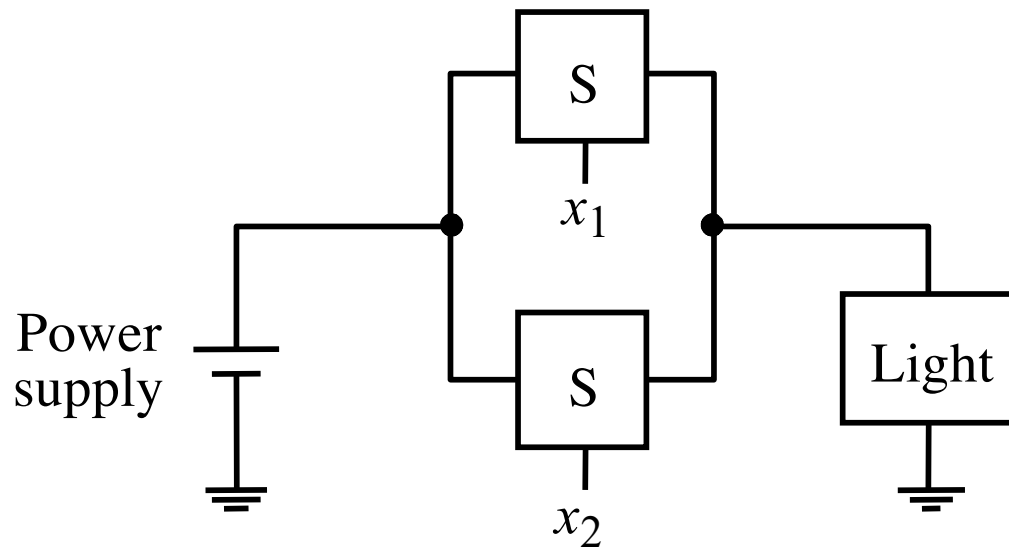
The Logical AND function (series connection of the switches)



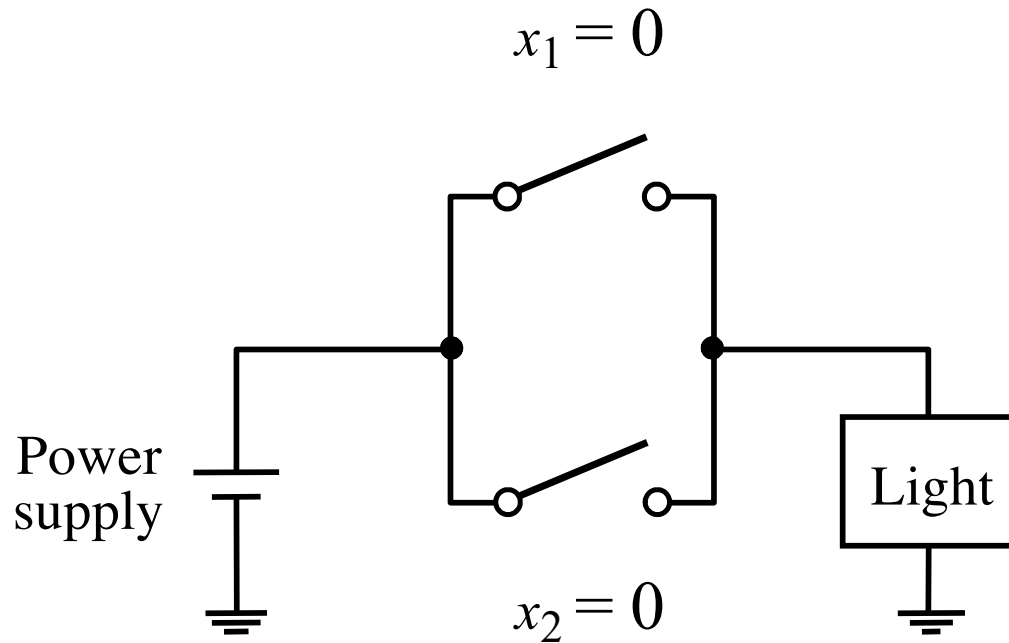
The Logical AND function (series connection of the switches)



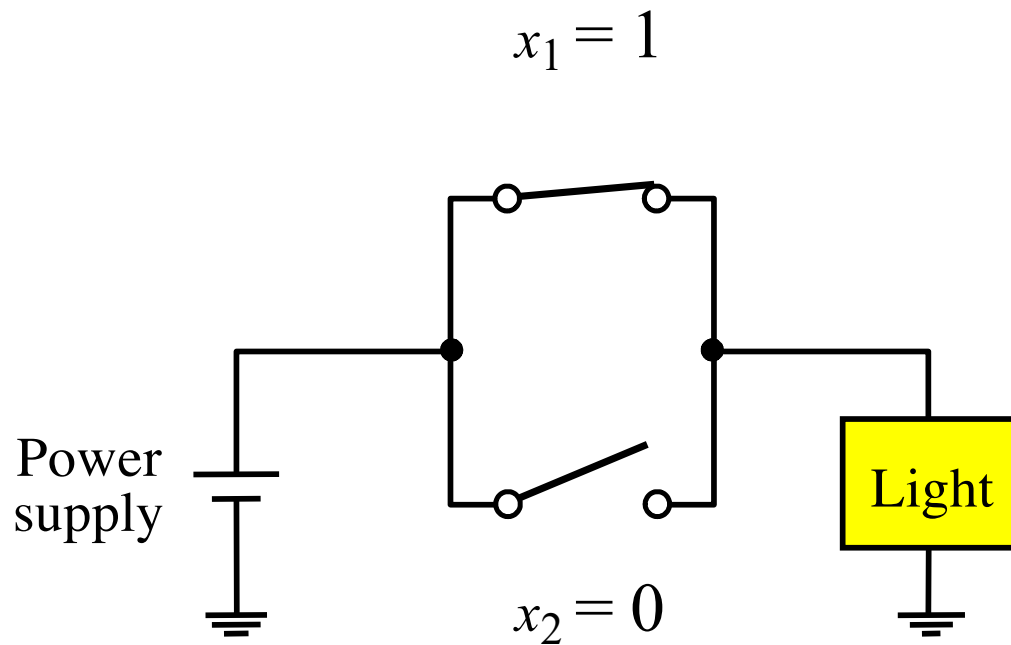
The Logical OR function (parallel connection of the switches)



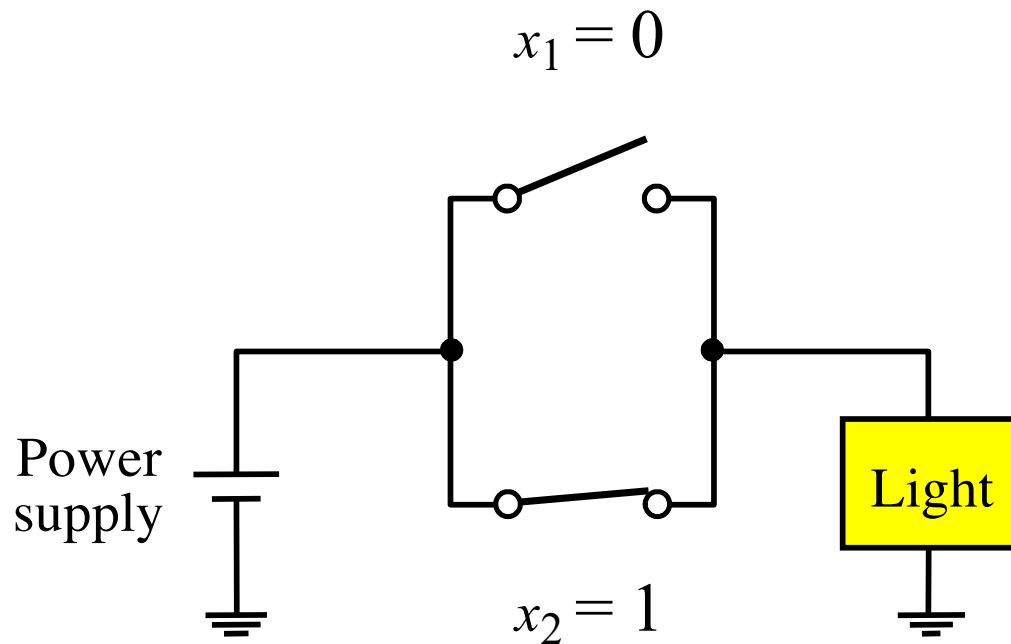
The Logical OR function (parallel connection of the switches)



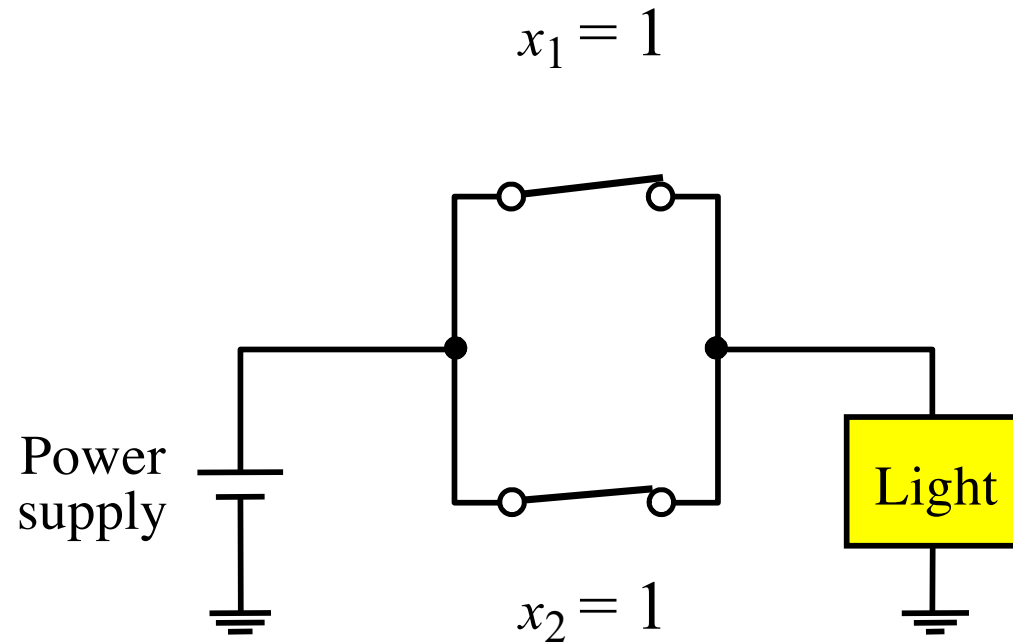
The Logical OR function (parallel connection of the switches)



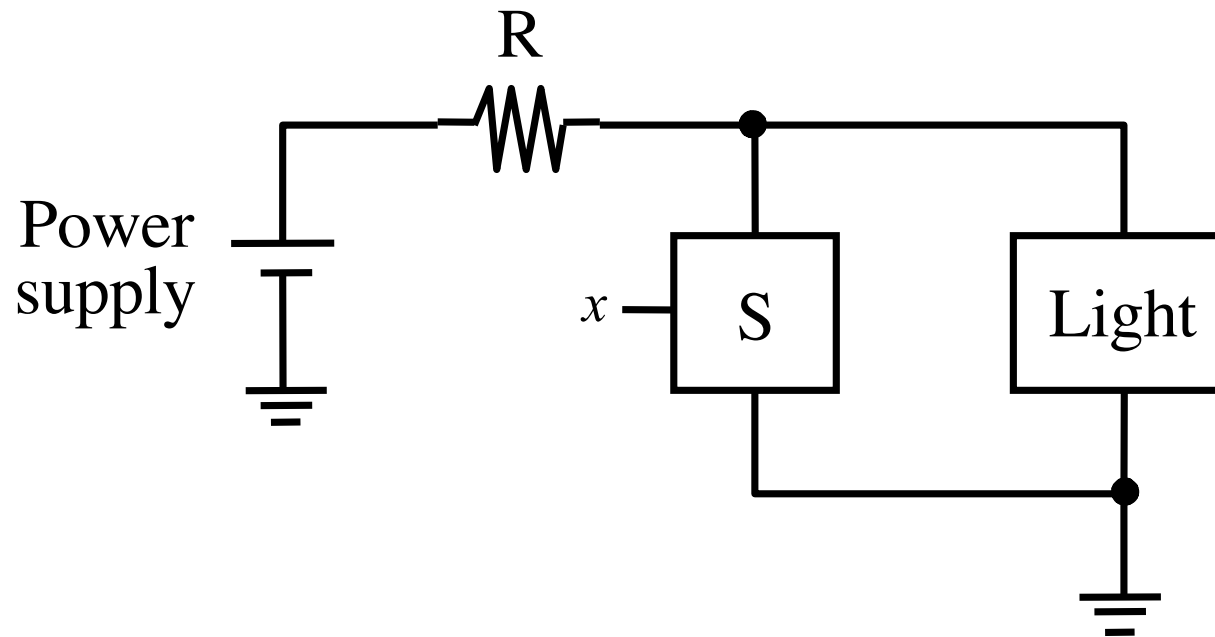
The Logical OR function (parallel connection of the switches)



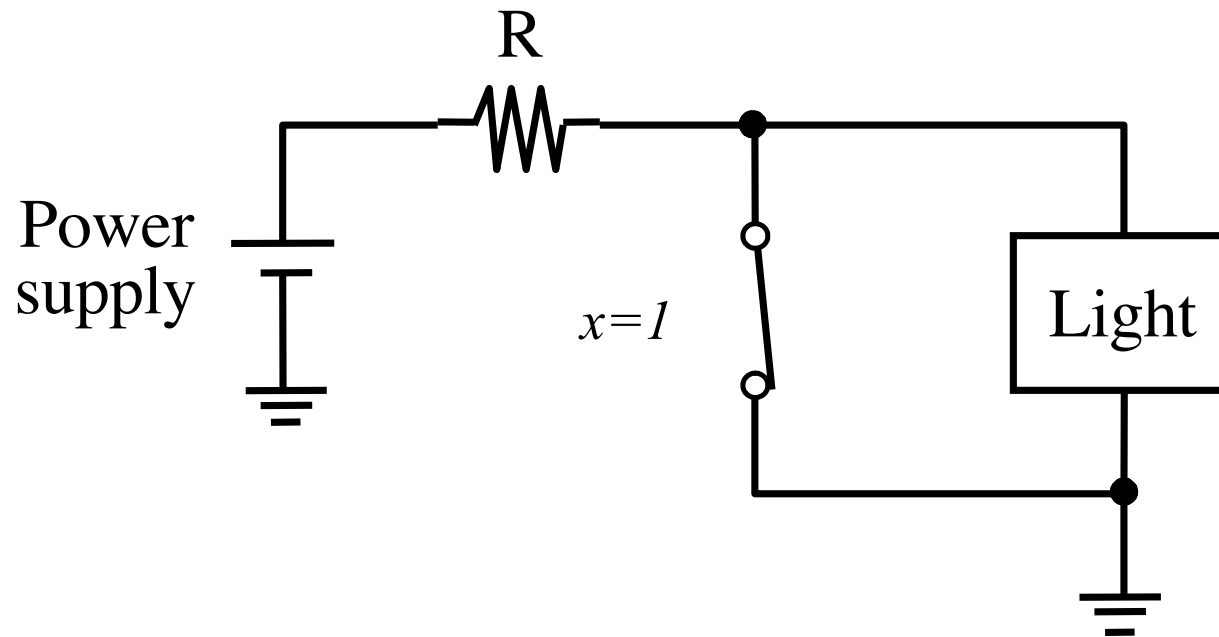
The Logical OR function (parallel connection of the switches)



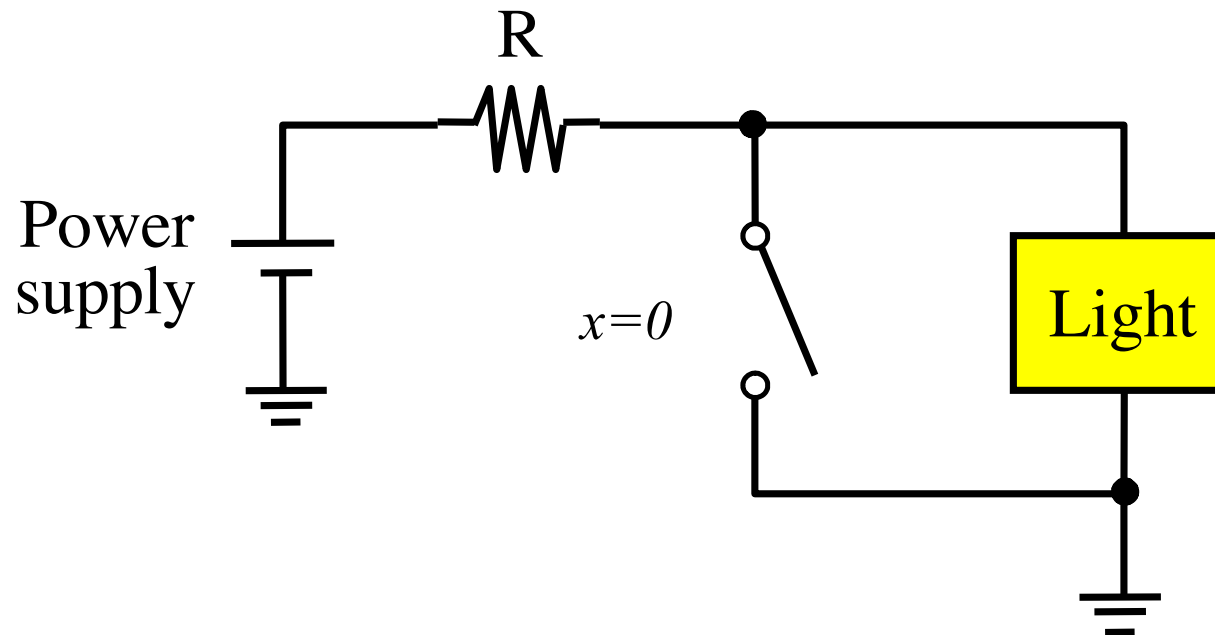
An Inverting Circuit



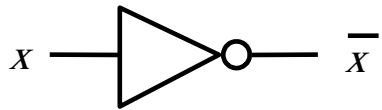
An Inverting Circuit



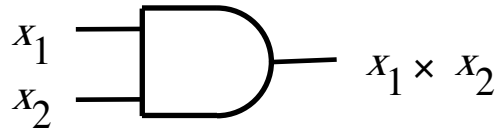
An Inverting Circuit



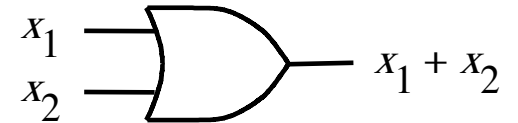
The Three Basic Logic Gates



NOT gate

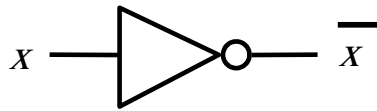


AND gate



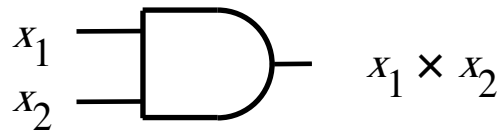
OR gate

Truth Table for NOT



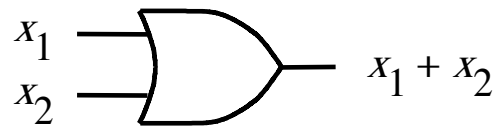
| x | \bar{x} |
|-----|-----------|
| 0 | 1 |
| 1 | 0 |

Truth Table for AND



| x_1 | x_2 | $x_1 \cdot x_2$ |
|-------|-------|-----------------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Truth Table for OR



| x_1 | x_2 | $x_1 + x_2$ |
|-------|-------|-------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

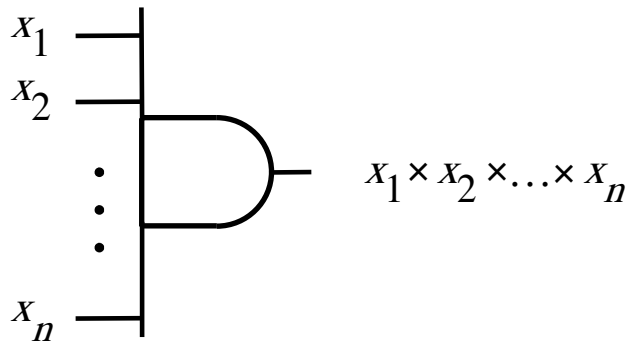
Truth Tables for AND and OR

| x_1 | x_2 | x_1 | x_2 | $x_1 + x_2$ |
|-------|-------|-------|-------|-------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

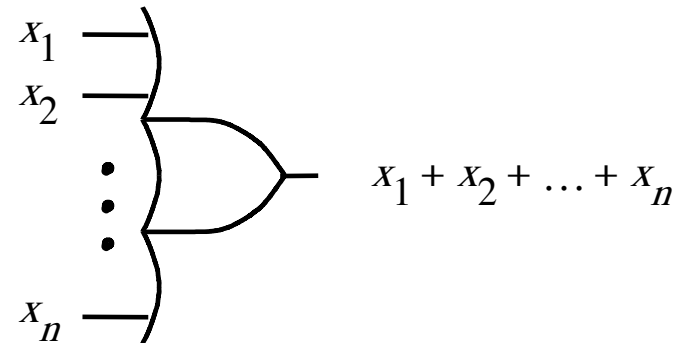
AND

OR

Logic Gates with n Inputs



AND gate

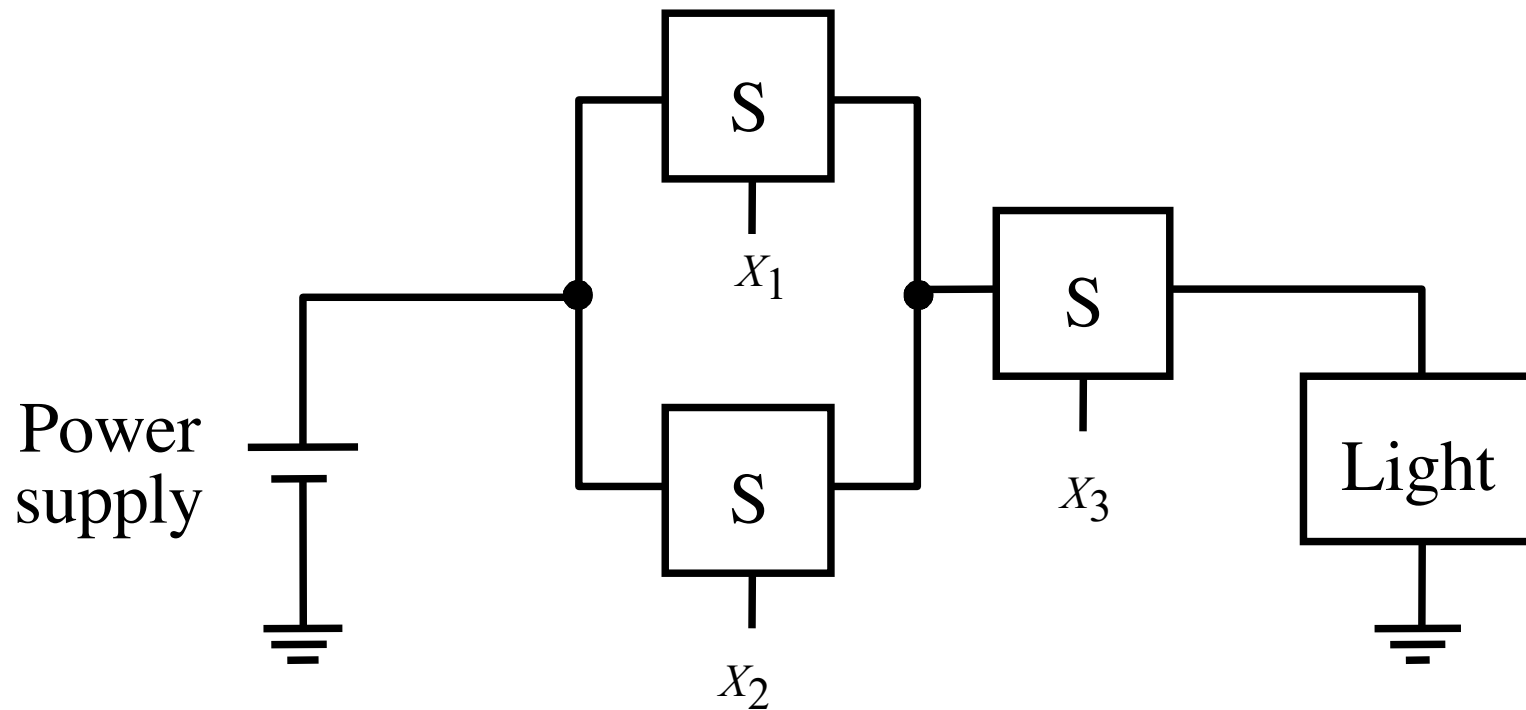


OR gate

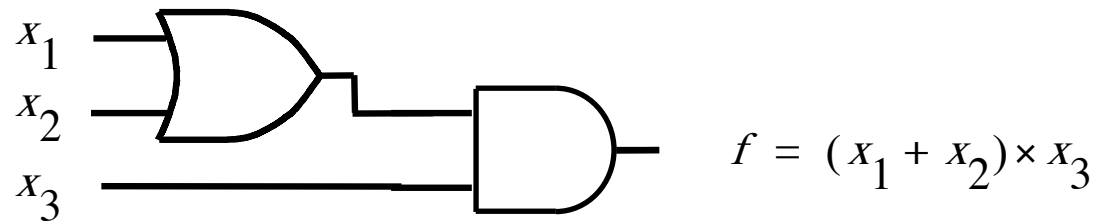
Truth Table for 3-input AND and OR

| x_1 | x_2 | x_3 | x_1 | x_2 | x_3 | $x_1 + x_2 + x_3$ |
|-------|-------|-------|-------|-------|-------|-------------------|
| 0 | 0 | 0 | | 0 | | 0 |
| 0 | 0 | 1 | | 0 | | 1 |
| 0 | 1 | 0 | | 0 | | 1 |
| 0 | 1 | 1 | | 0 | | 1 |
| 1 | 0 | 0 | | 0 | | 1 |
| 1 | 0 | 1 | | 0 | | 1 |
| 1 | 1 | 0 | | 0 | | 1 |
| 1 | 1 | 1 | | 1 | | 1 |

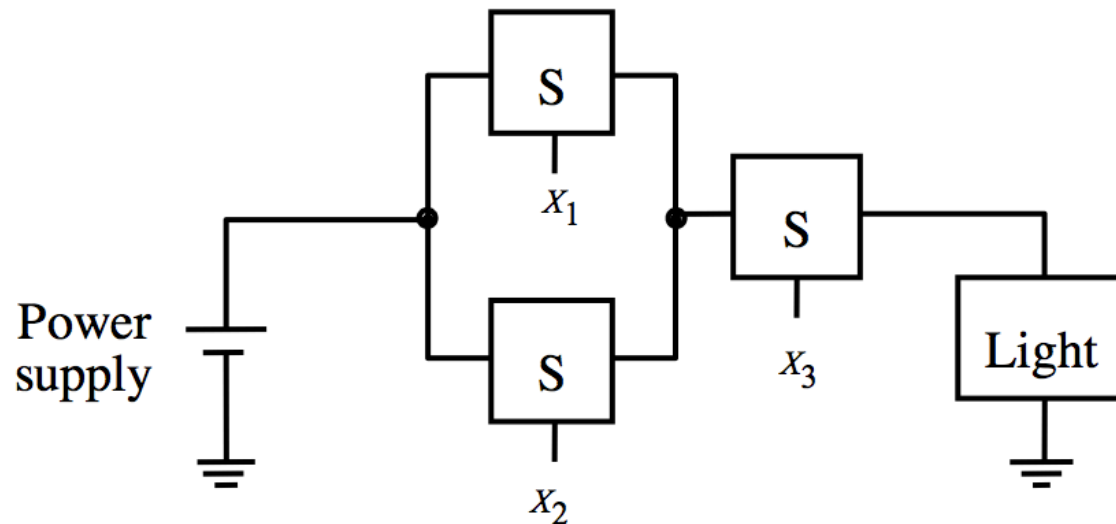
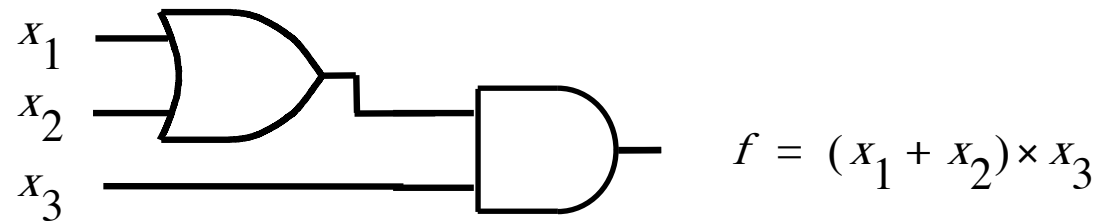
A series-parallel connection of the switches



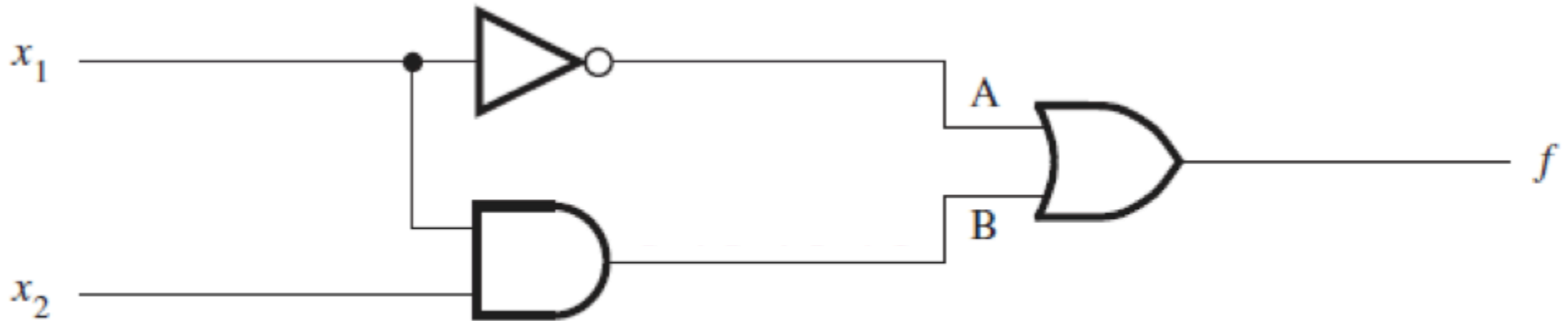
Example of a Logic Circuit Implemented with Logic Gates



Example of a Logic Circuit Implemented with Logic Gates

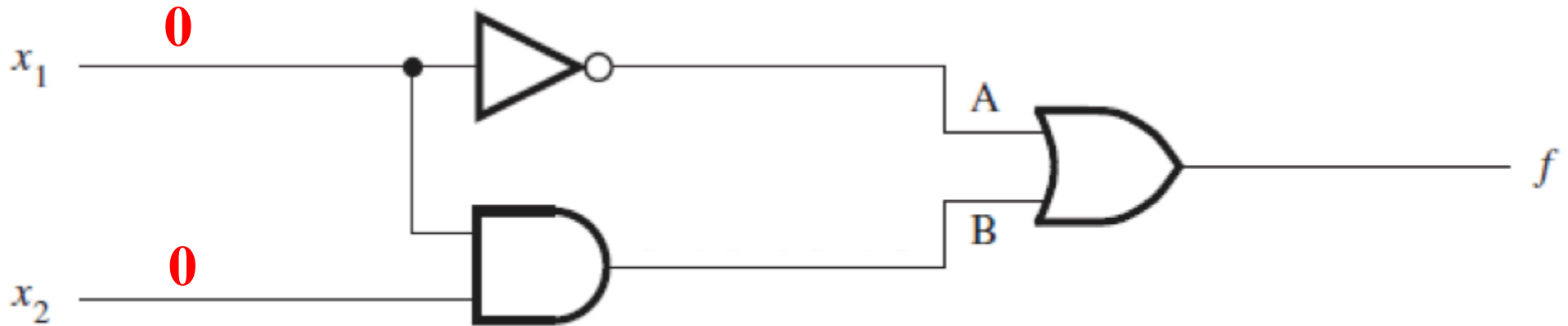


Circuit Analysis



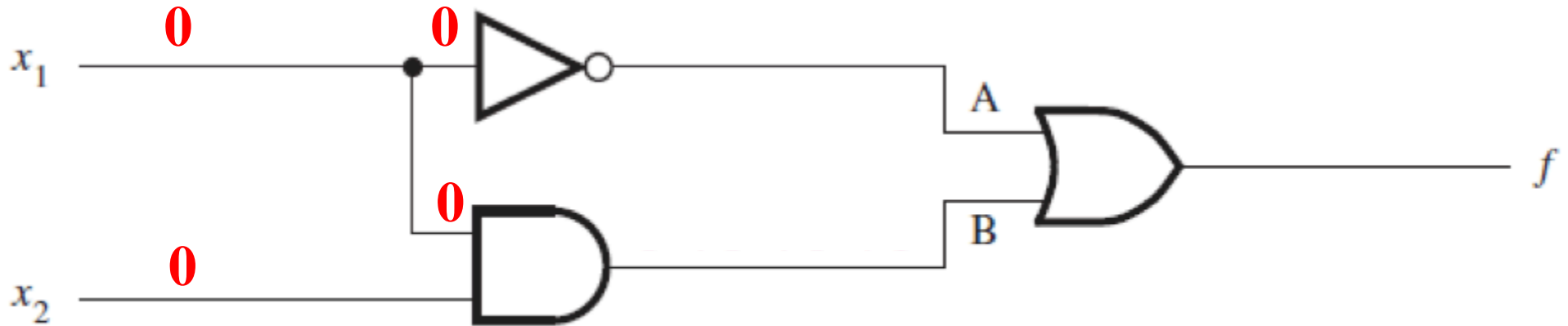
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



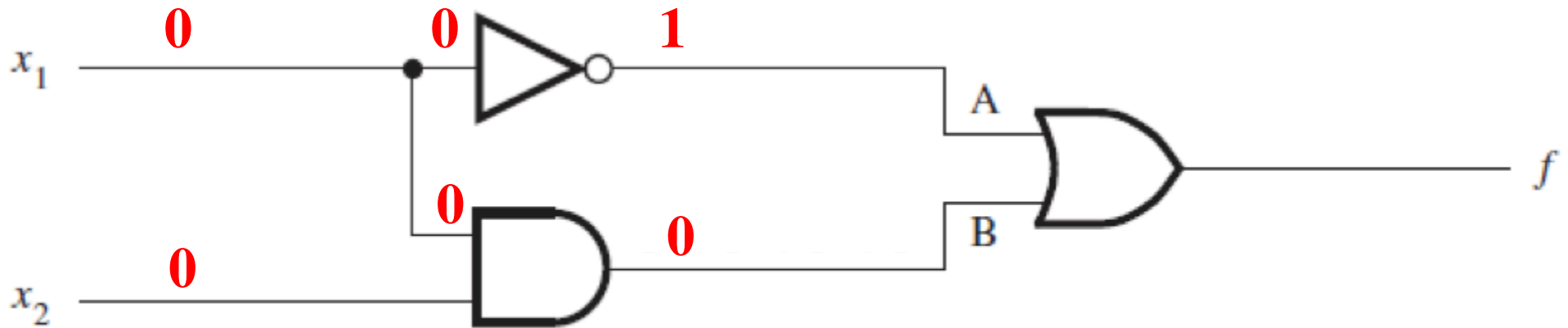
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



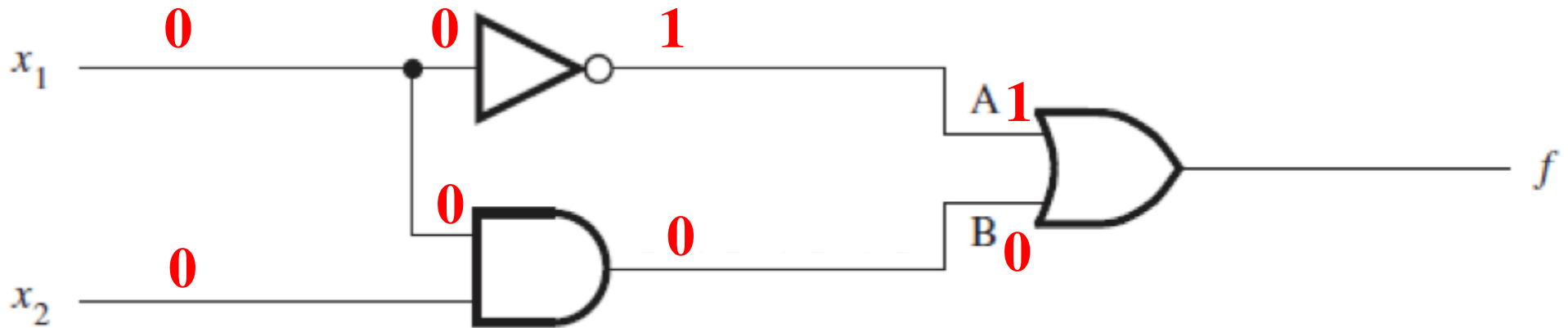
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



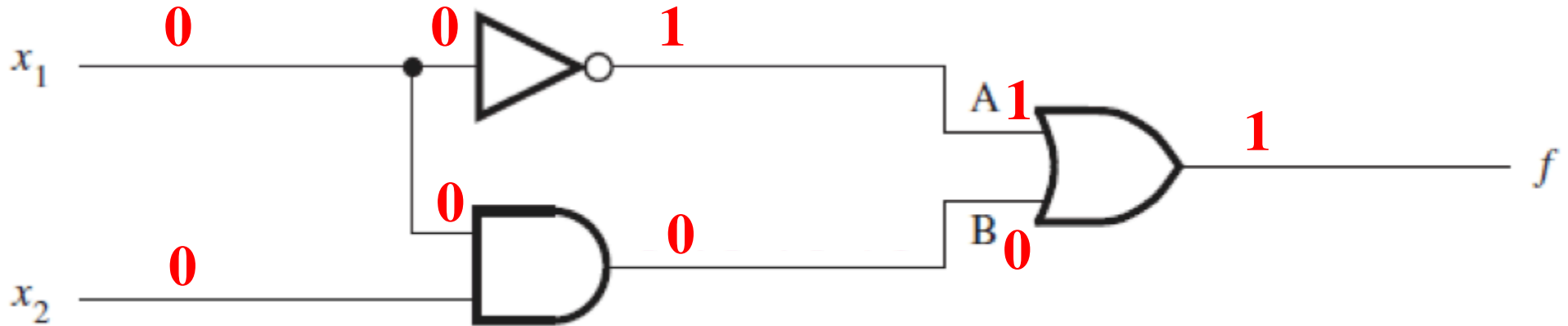
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



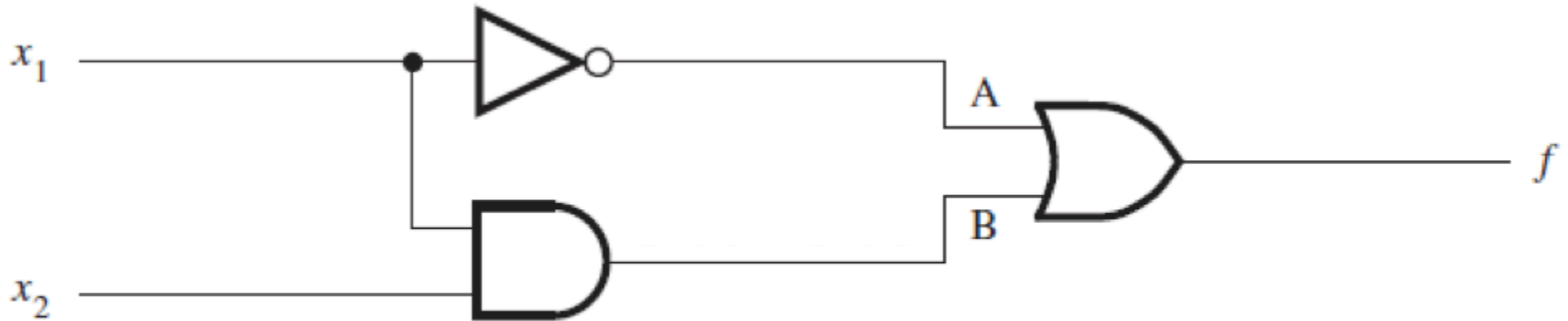
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



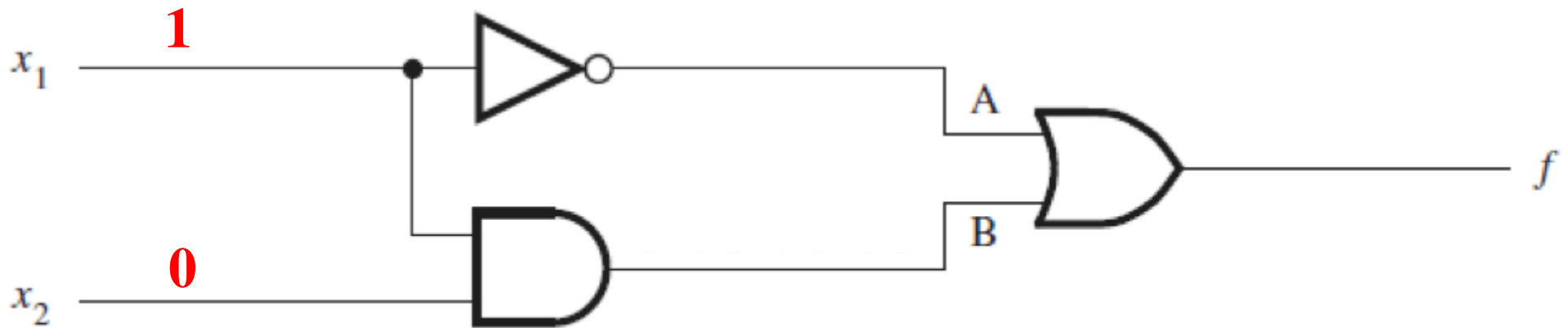
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



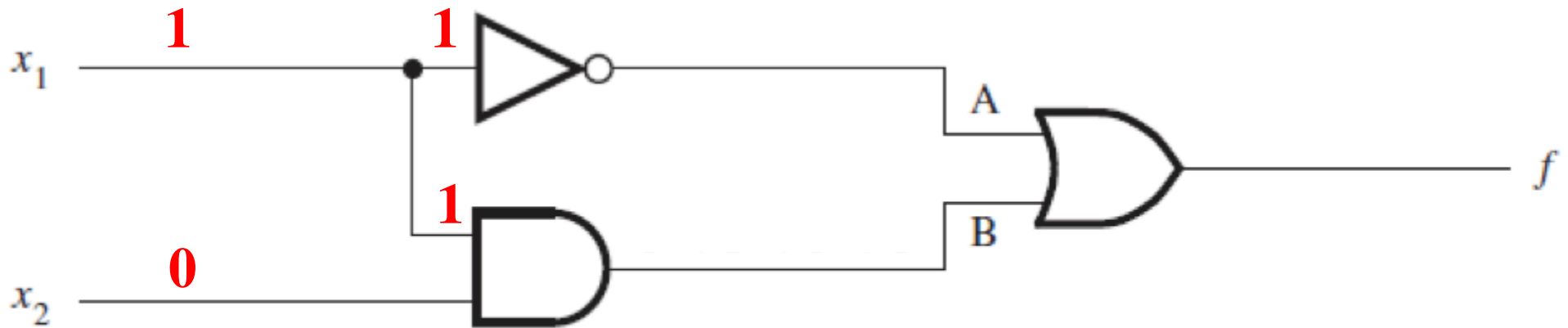
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



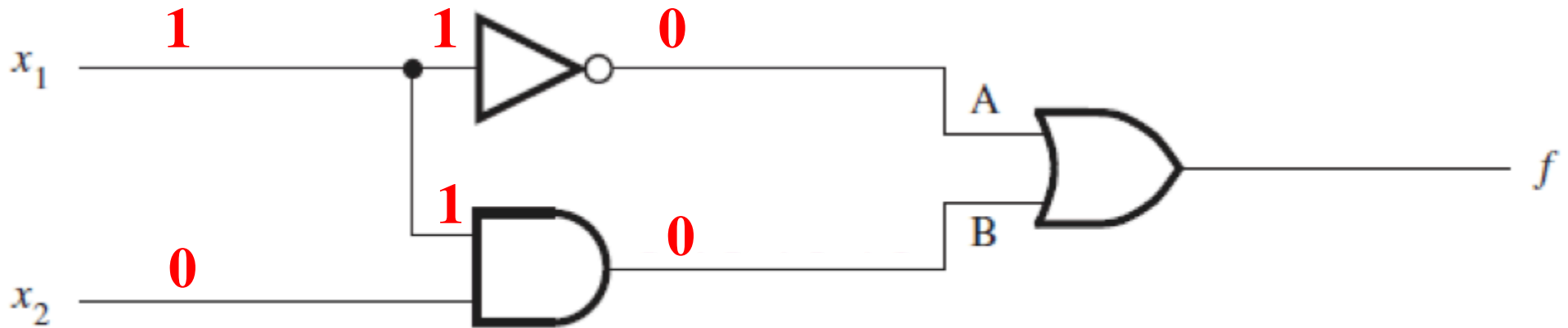
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



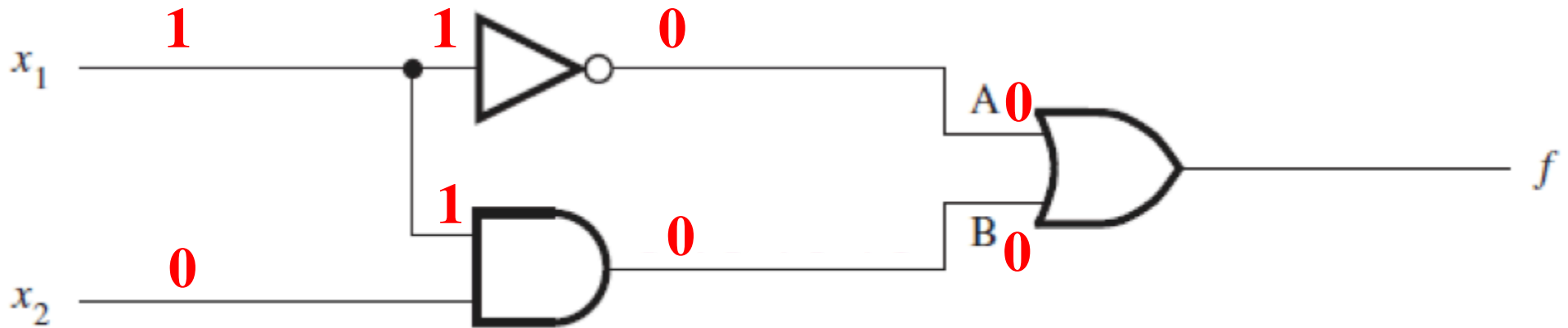
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



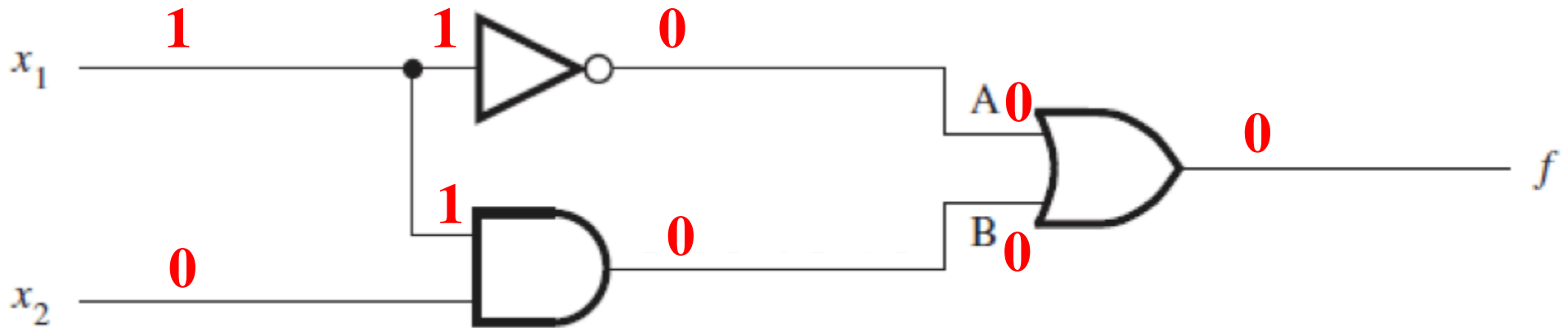
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



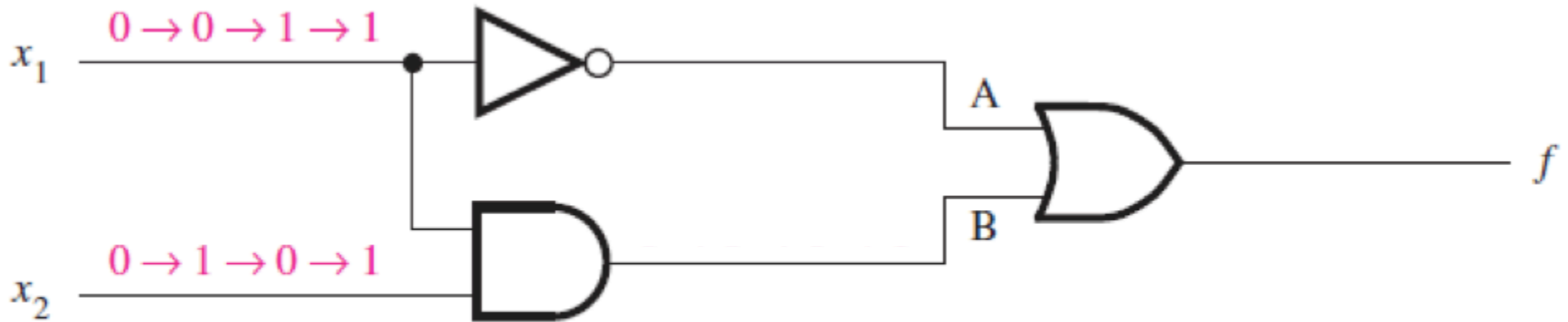
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis



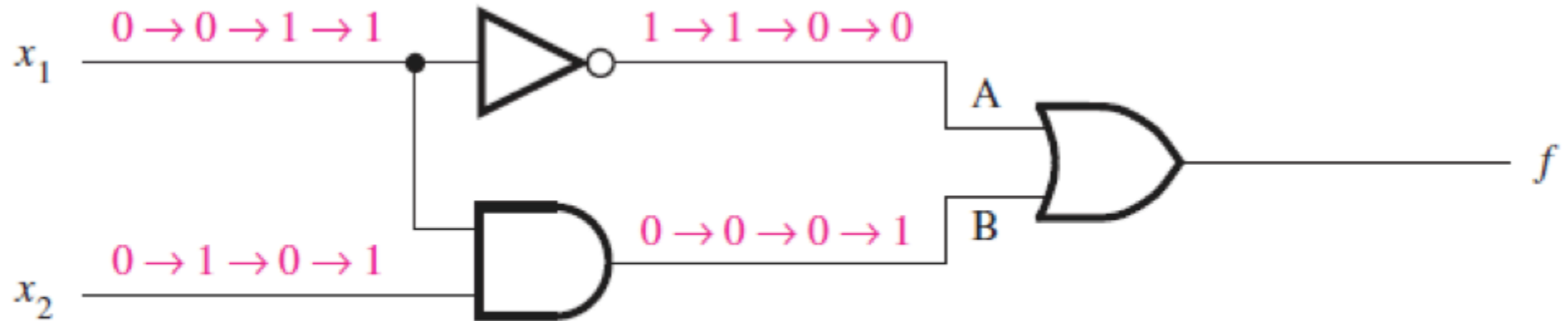
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis with Sequential Inputs



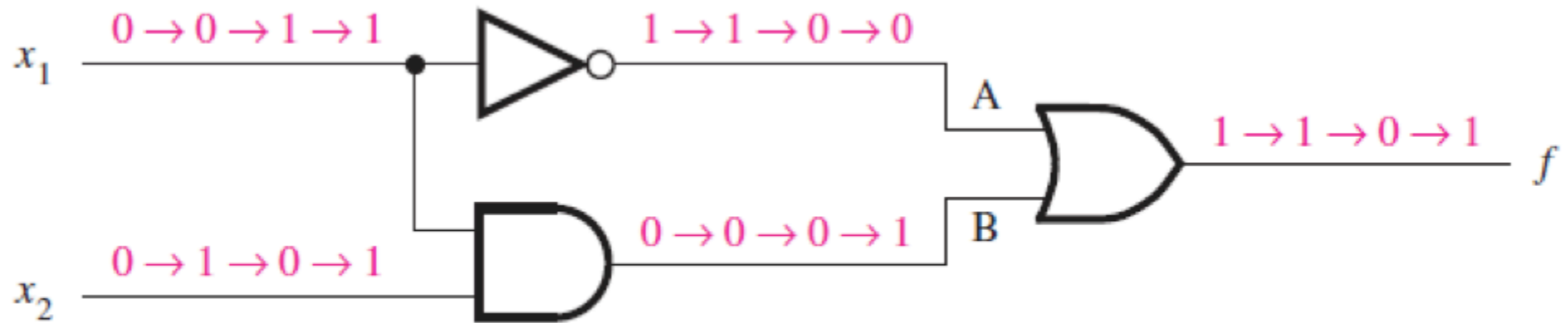
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis with Sequential Inputs



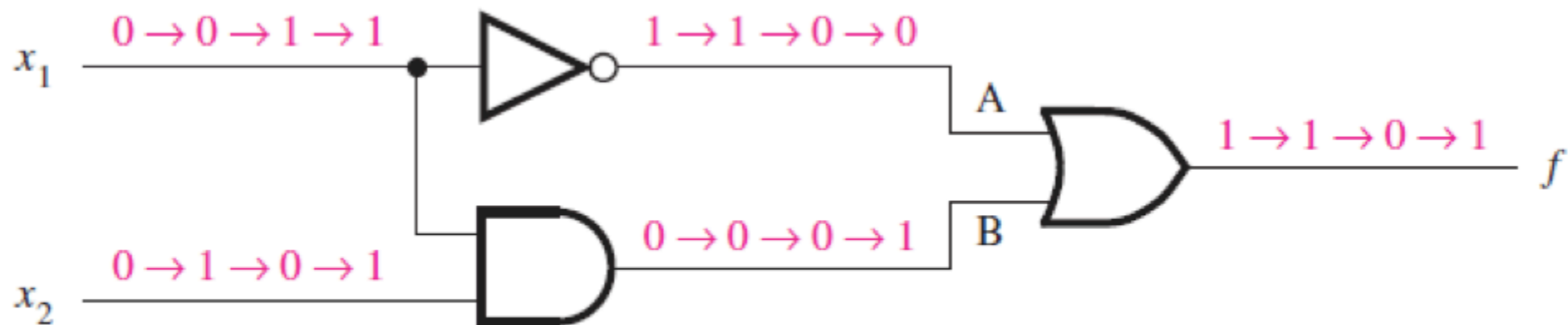
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Circuit Analysis with Sequential Inputs

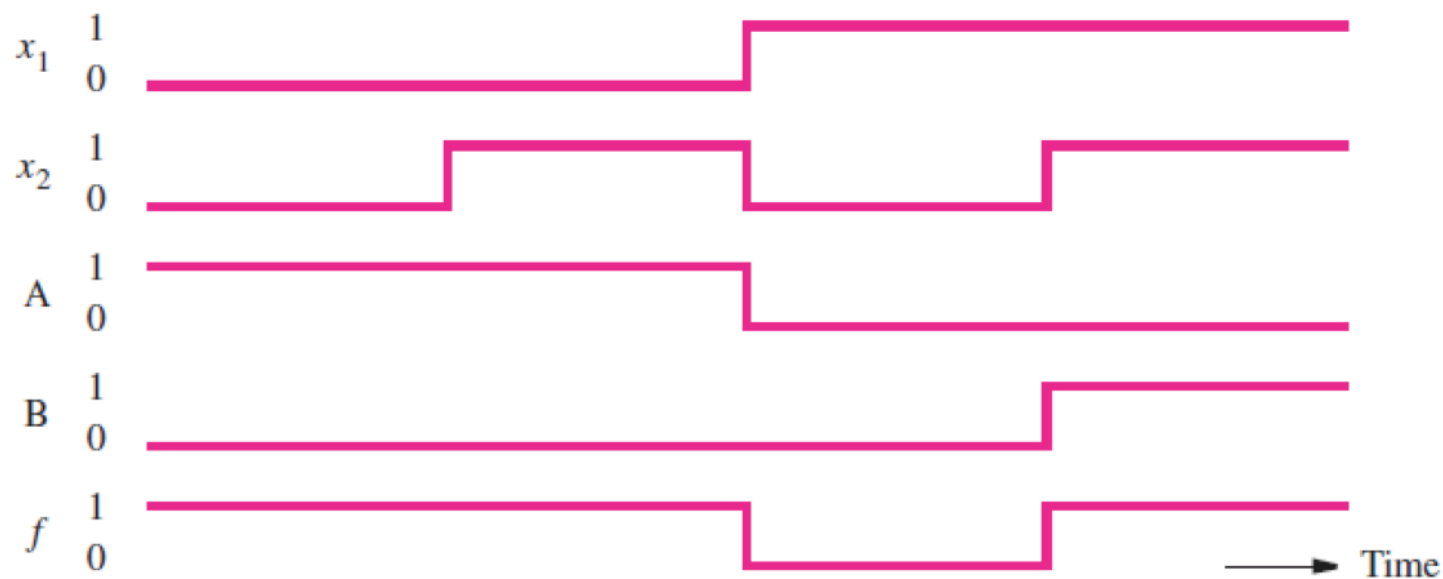


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

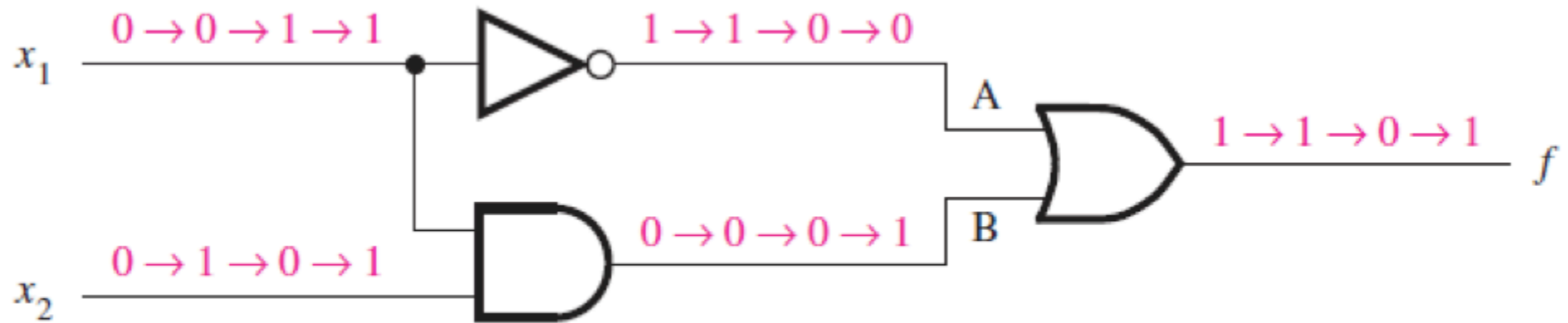
Circuit Analysis with Sequential Inputs



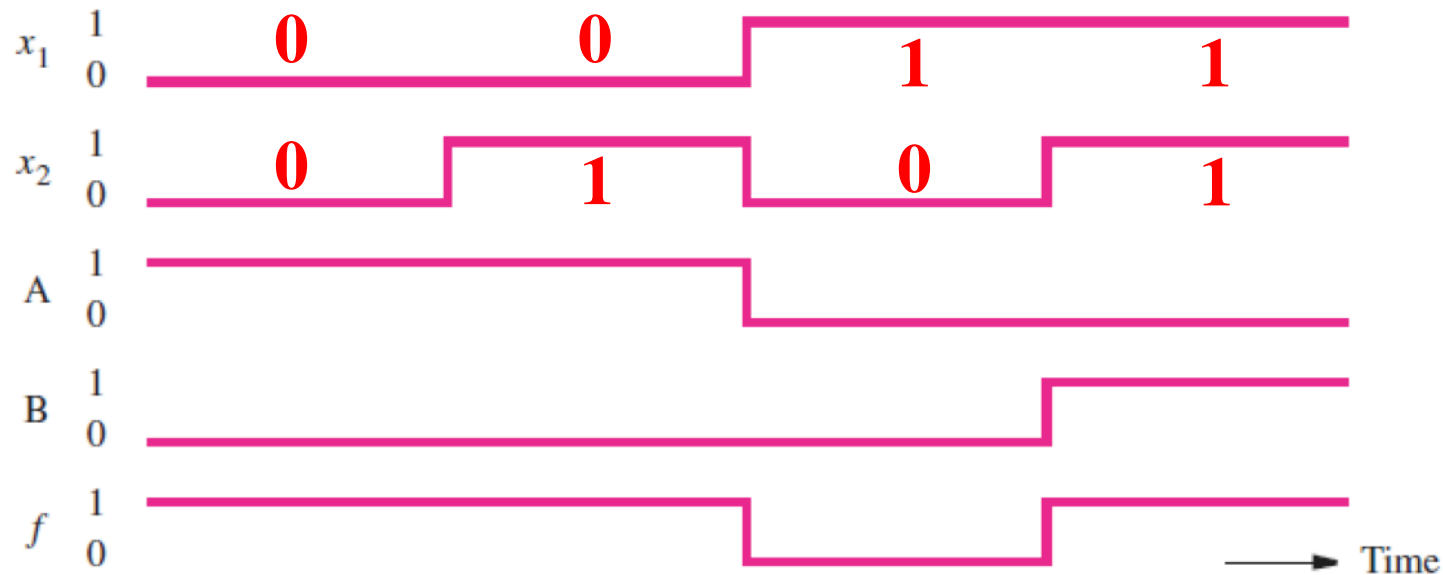
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



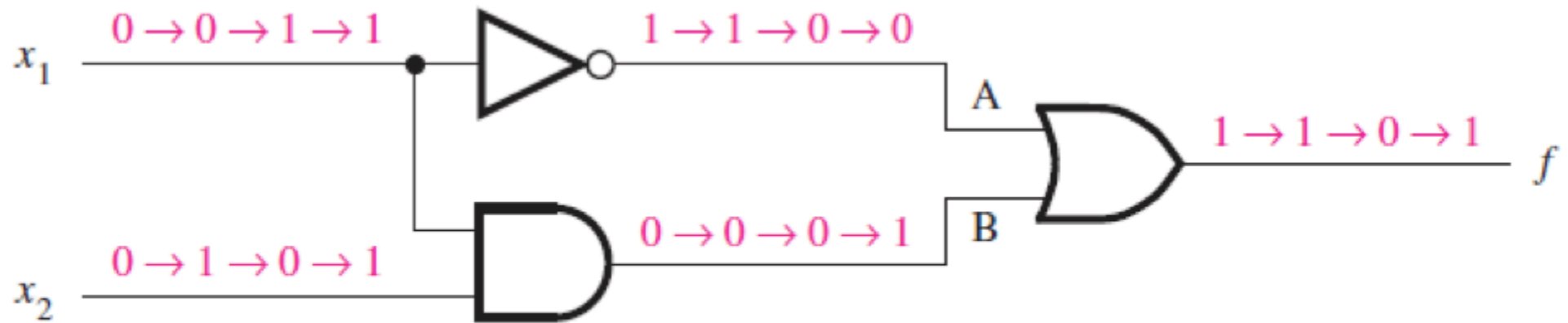
Circuit Analysis with Sequential Inputs



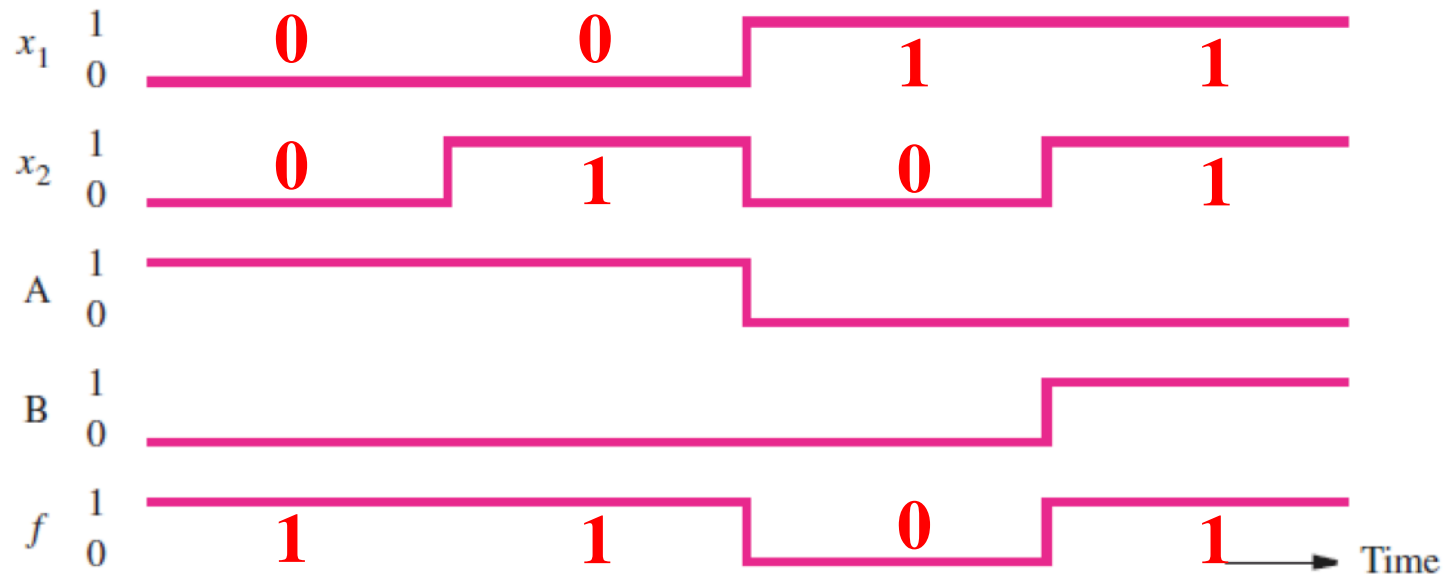
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



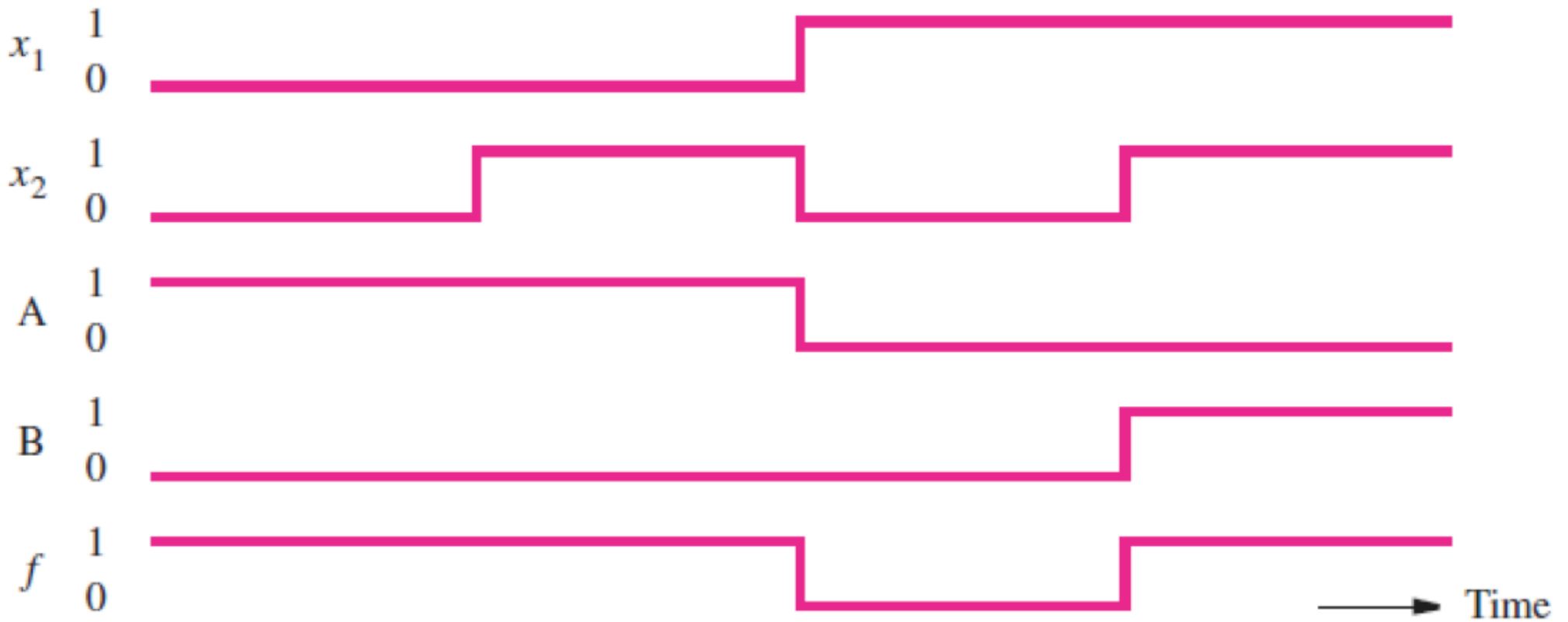
Circuit Analysis with Sequential Inputs



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



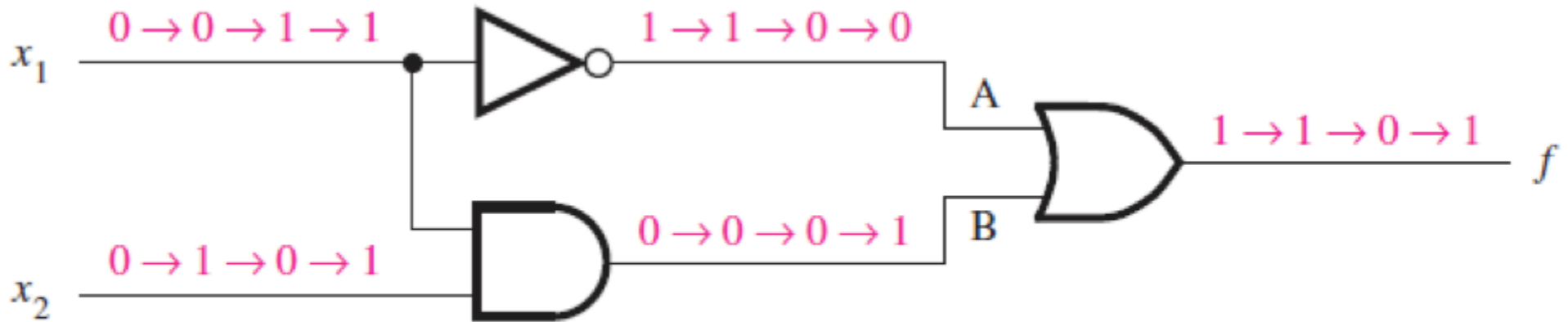
Timing Diagram



Truth Table for this Logic Circuit

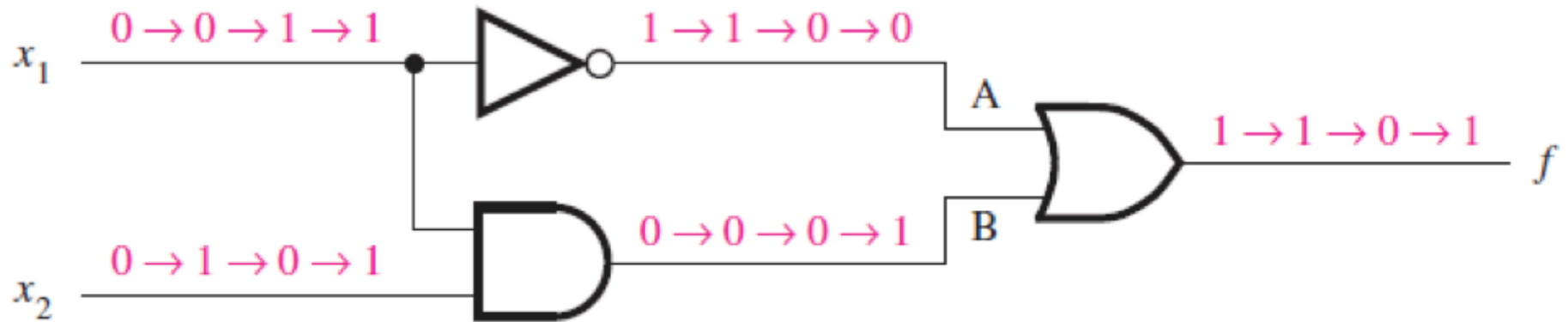
| x_1 | x_2 | $f(x_1, x_2)$ |
|-------|-------|---------------|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Truth Table for this Logic Circuit



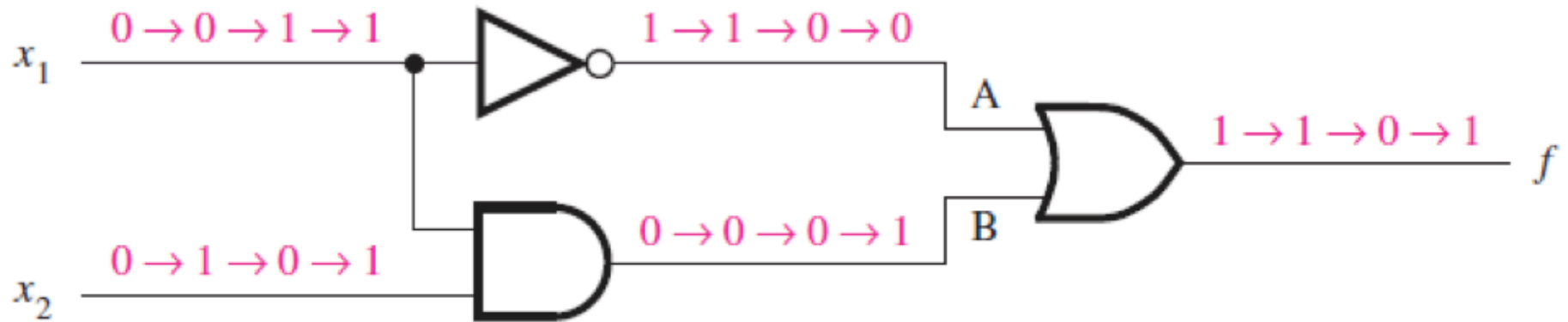
| x_1 | x_2 | $f(x_1, x_2)$ |
|-------|-------|---------------|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Functionally Equivalent Circuits

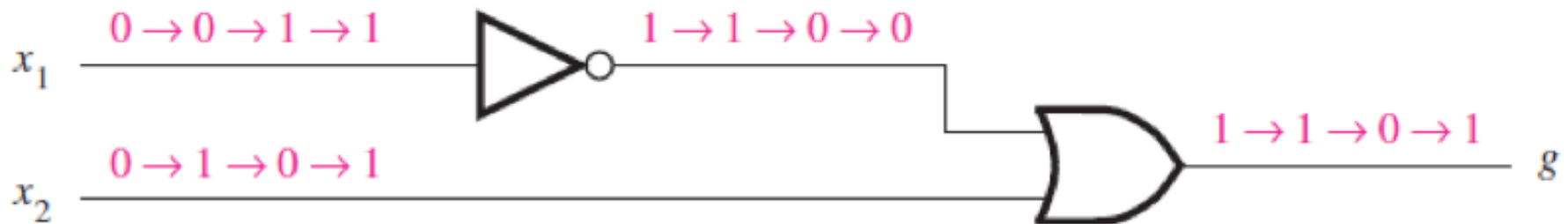


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

Functionally Equivalent Circuits

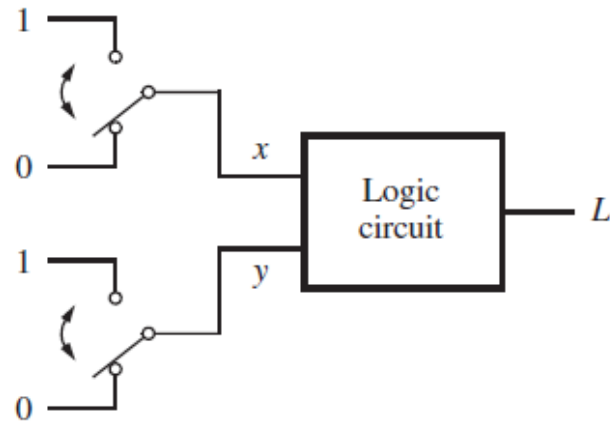


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



(d) Network that implements $g = \bar{x}_1 + x_2$

The XOR Logic Gate

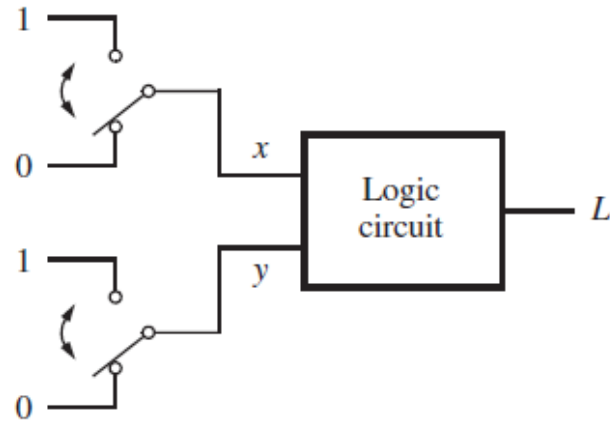


(a) Two switches that control a light

| x | y | L |
|-----|-----|-----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b) Truth table

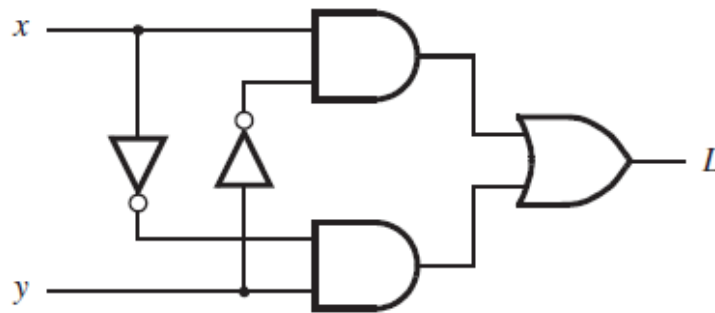
The XOR Logic Gate



(a) Two switches that control a light

| x | y | L |
|-----|-----|-----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b) Truth table

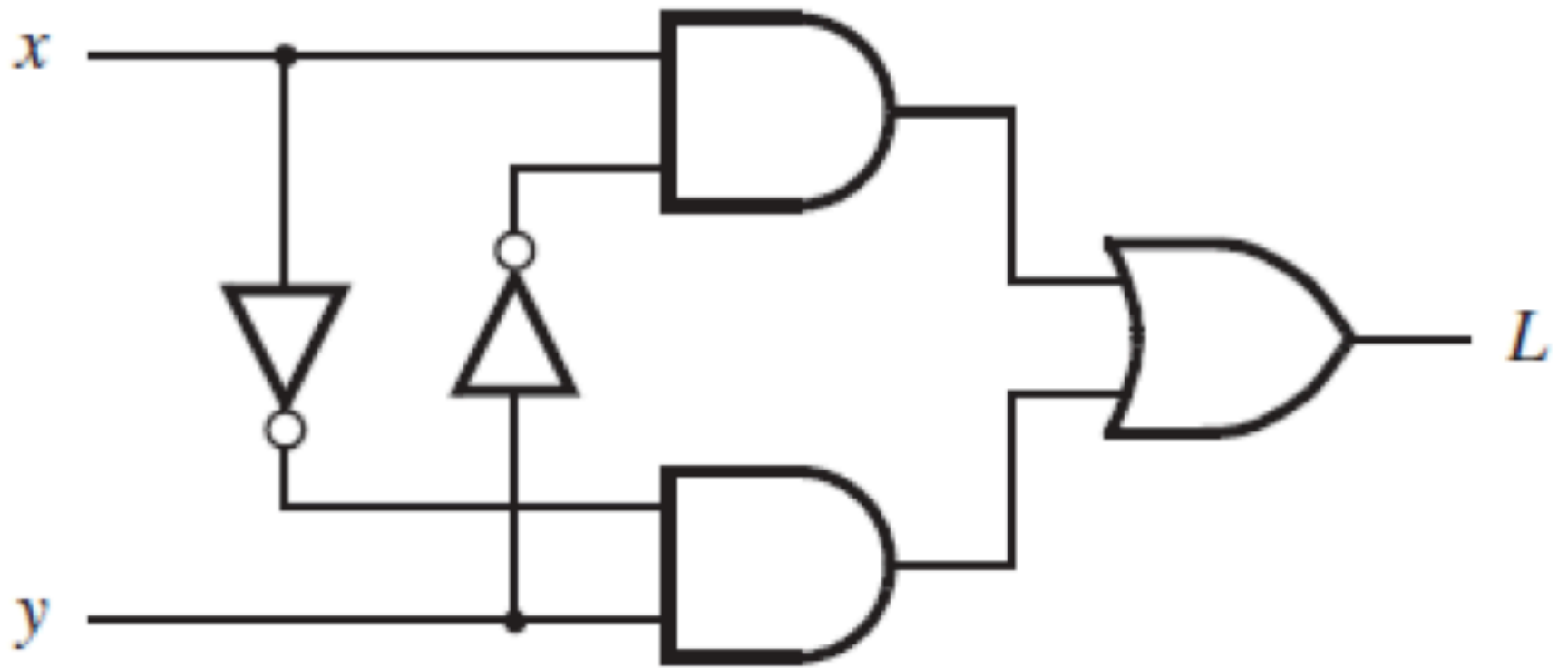


(c) Logic network



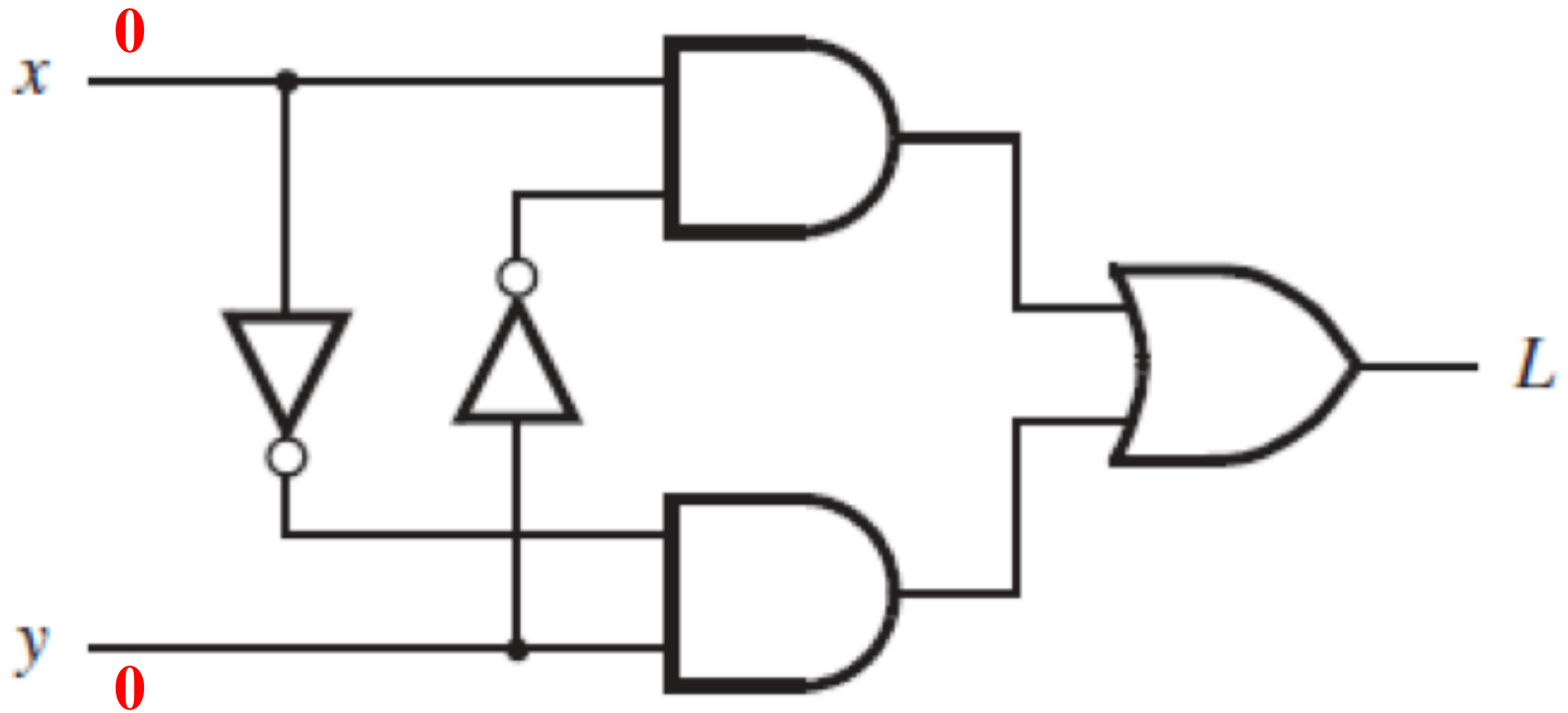
(d) XOR gate symbol

XOR Analysis

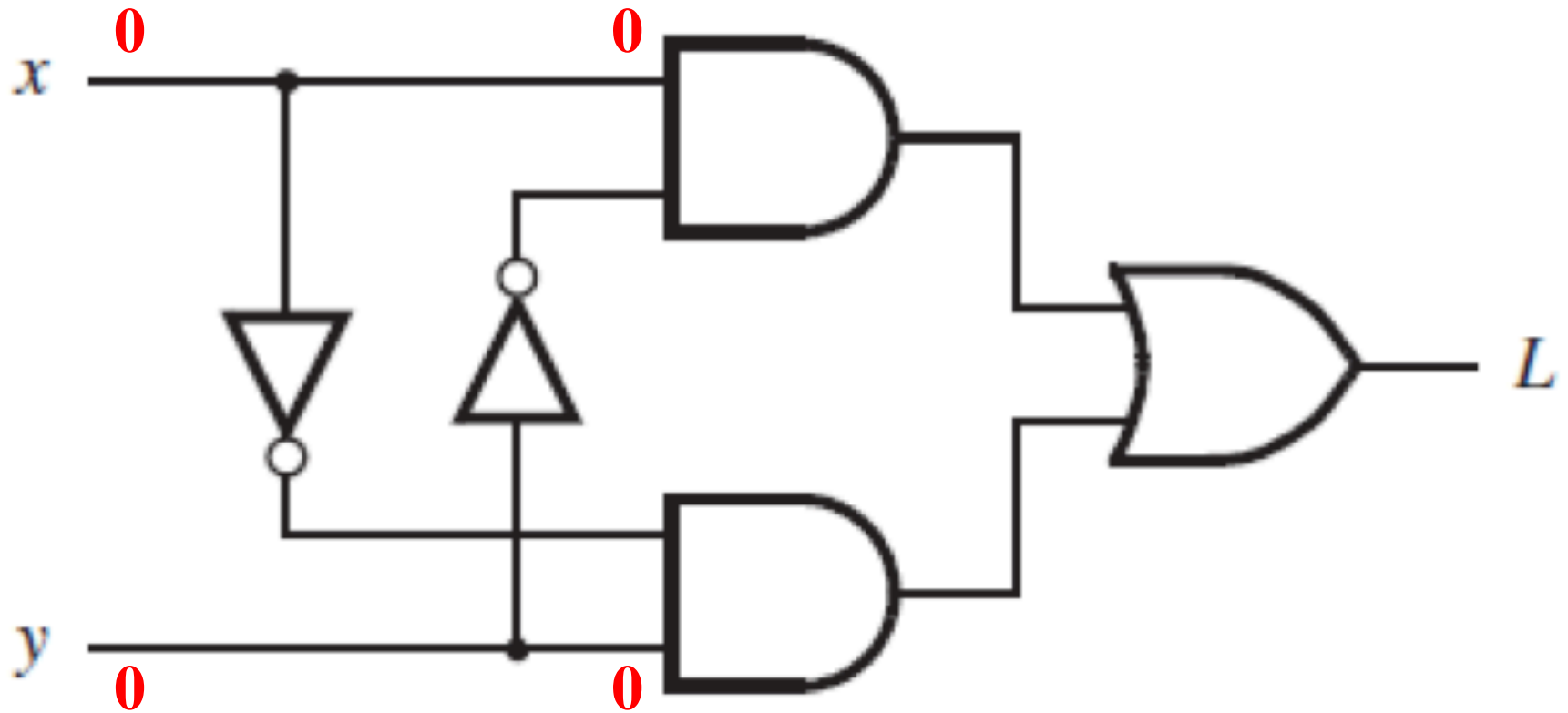


[Figure 2.11c from the textbook]

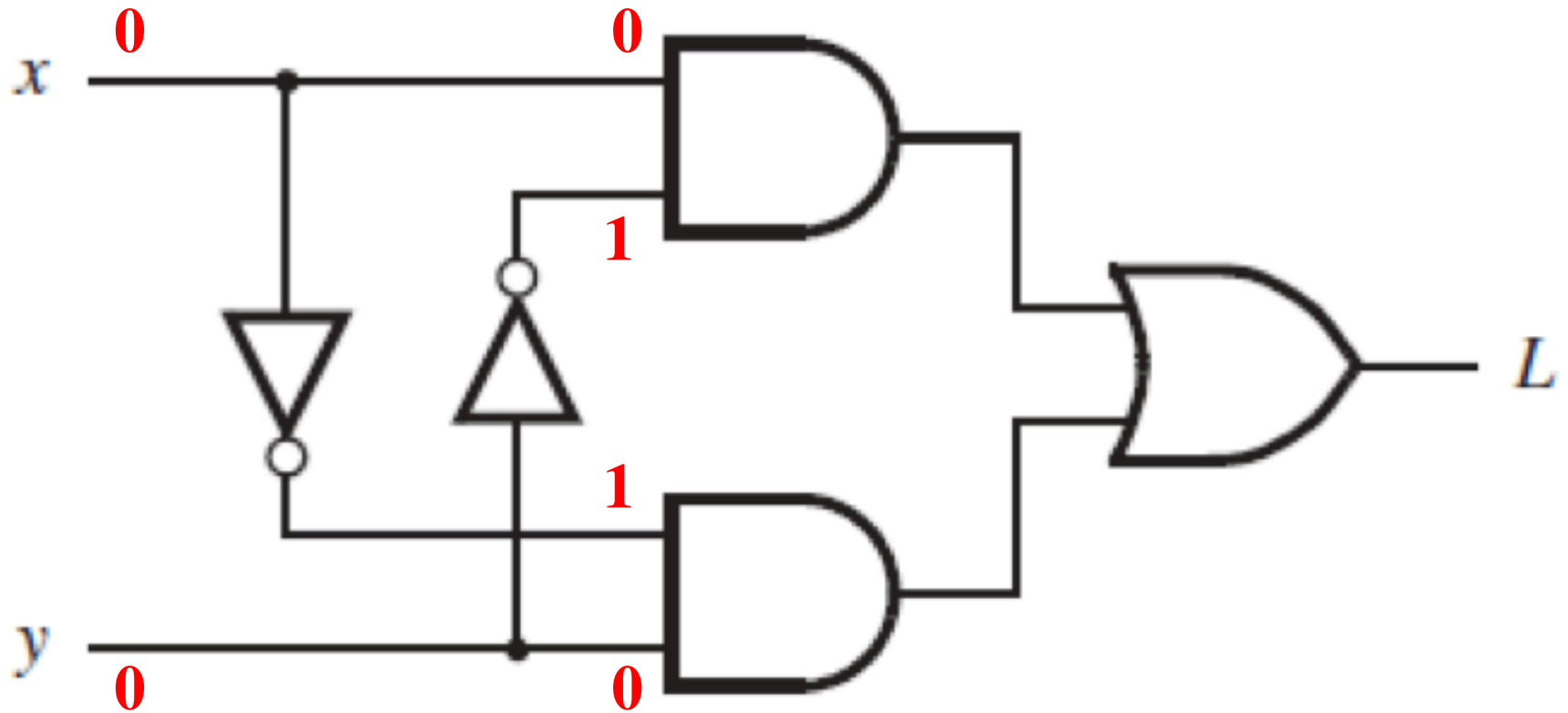
XOR Analysis (x=0, y=0)



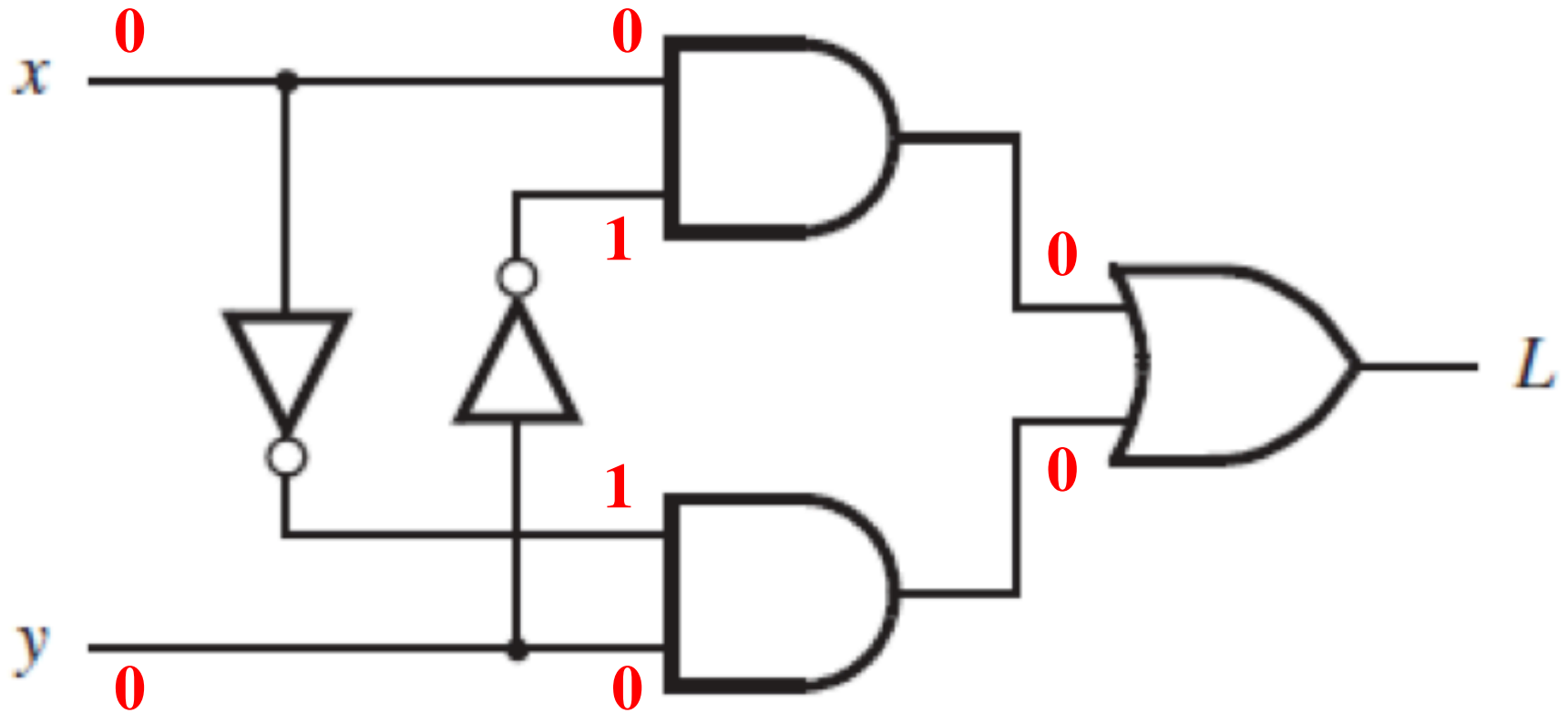
XOR Analysis (x=0, y=0)



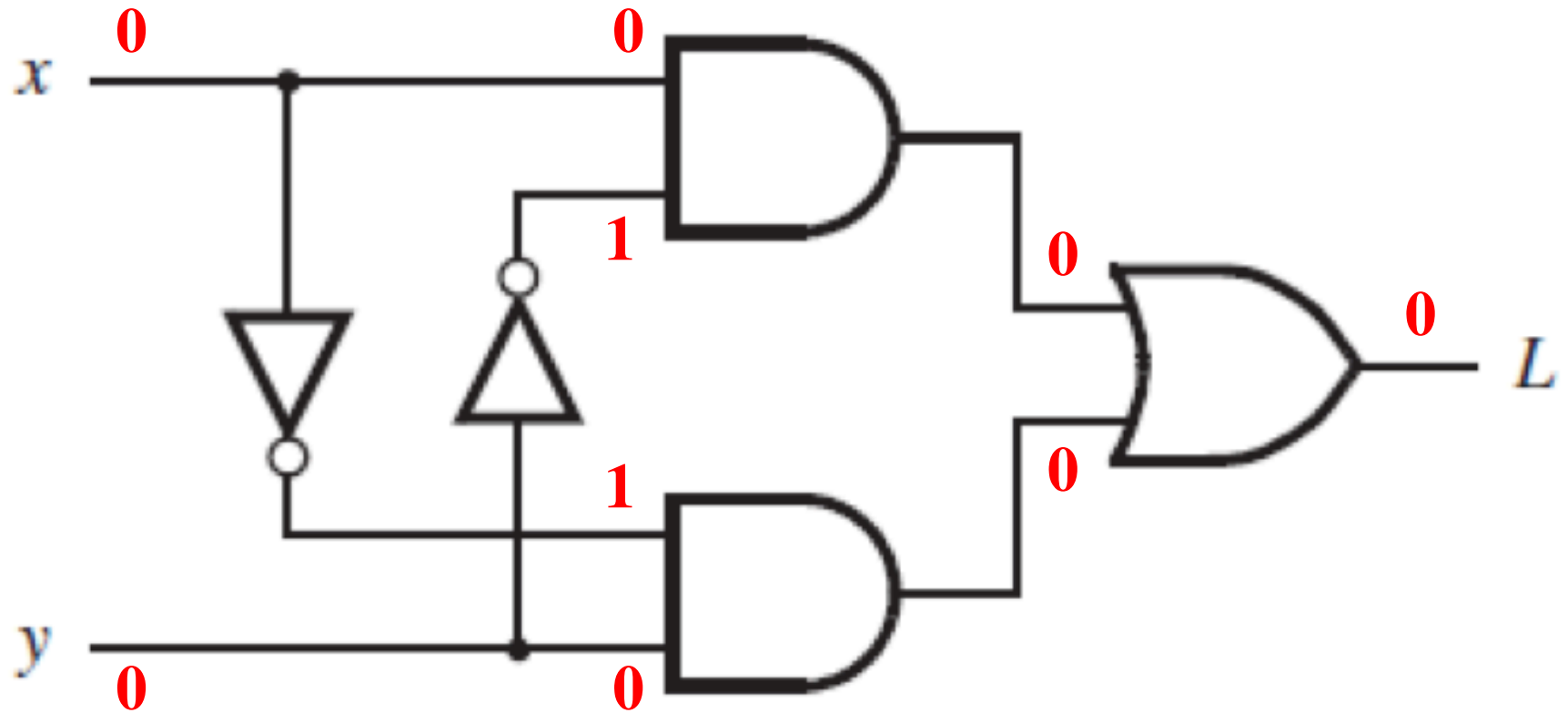
XOR Analysis (x=0, y=0)



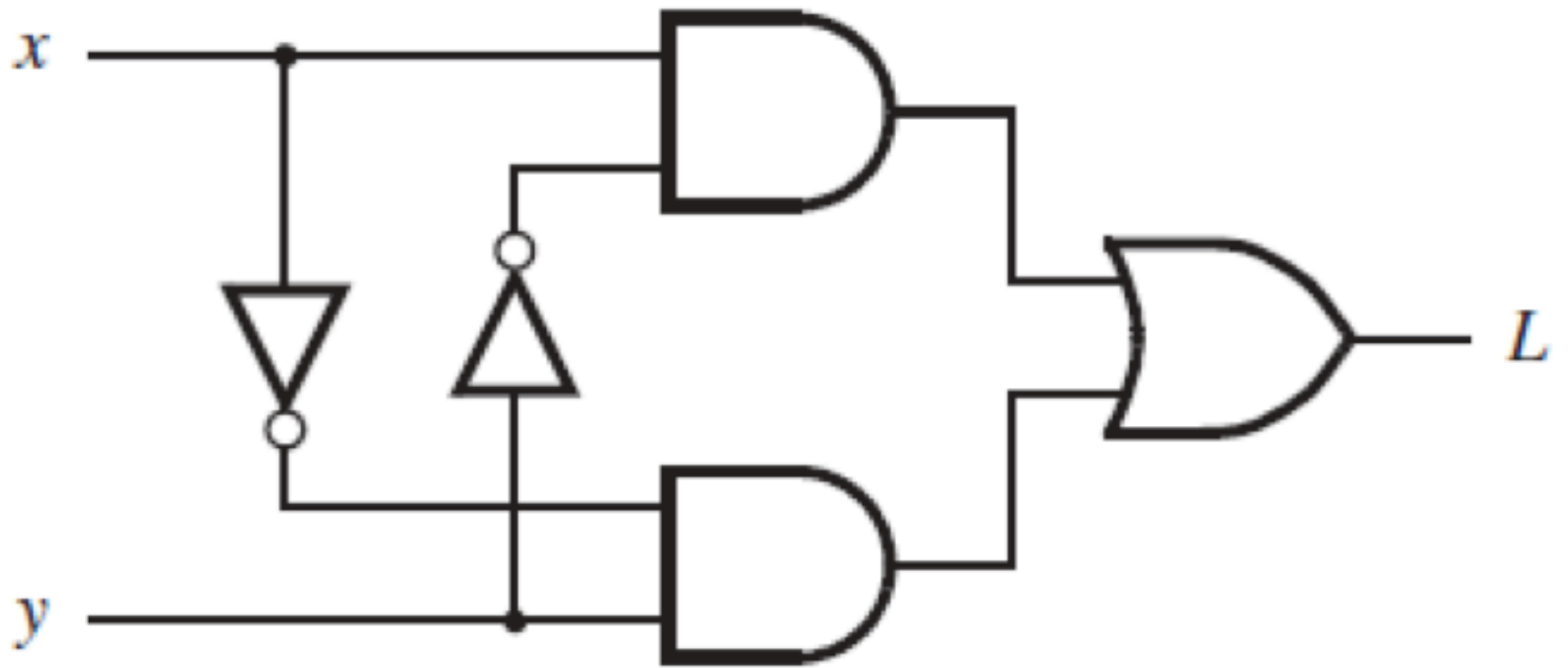
XOR Analysis (x=0, y=0)



XOR Analysis (x=0, y=0)

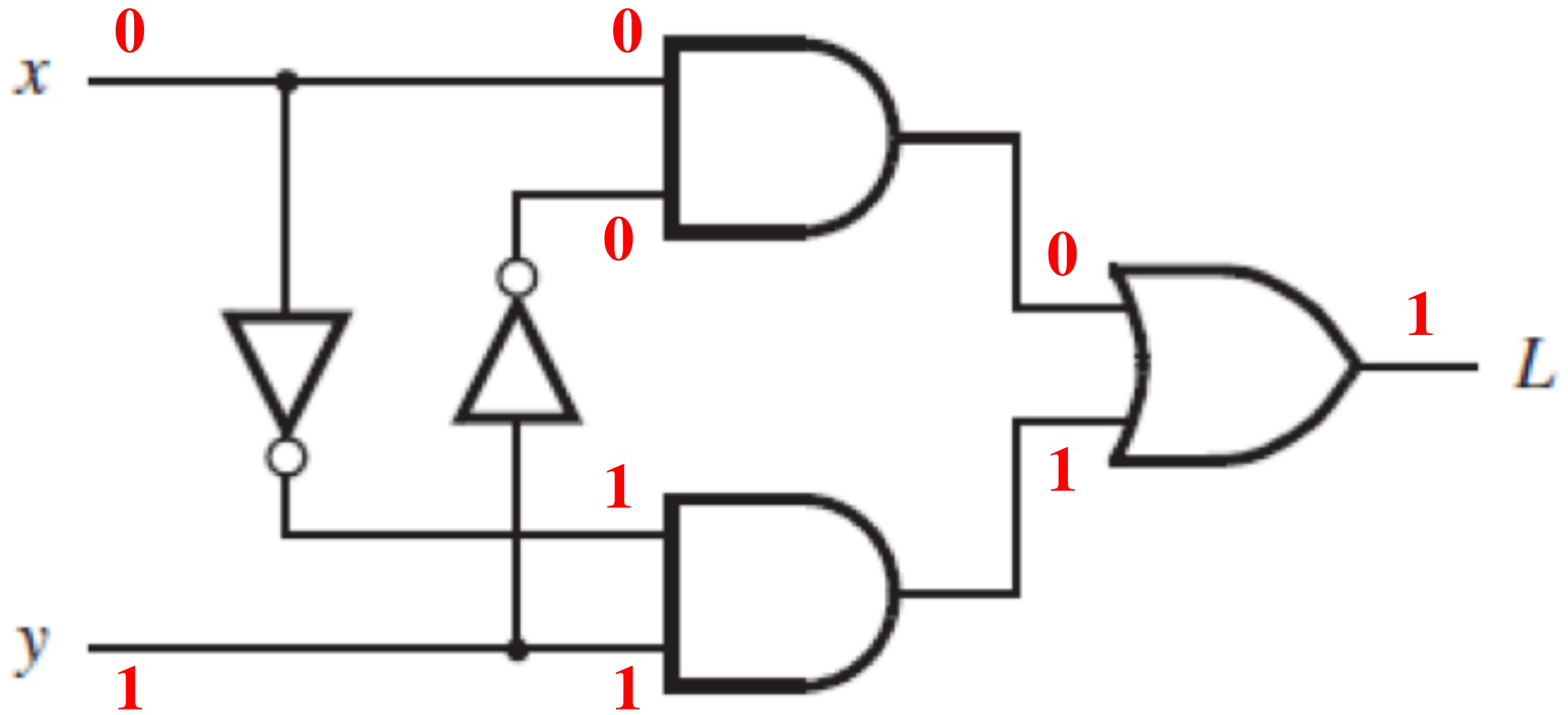


XOR Analysis

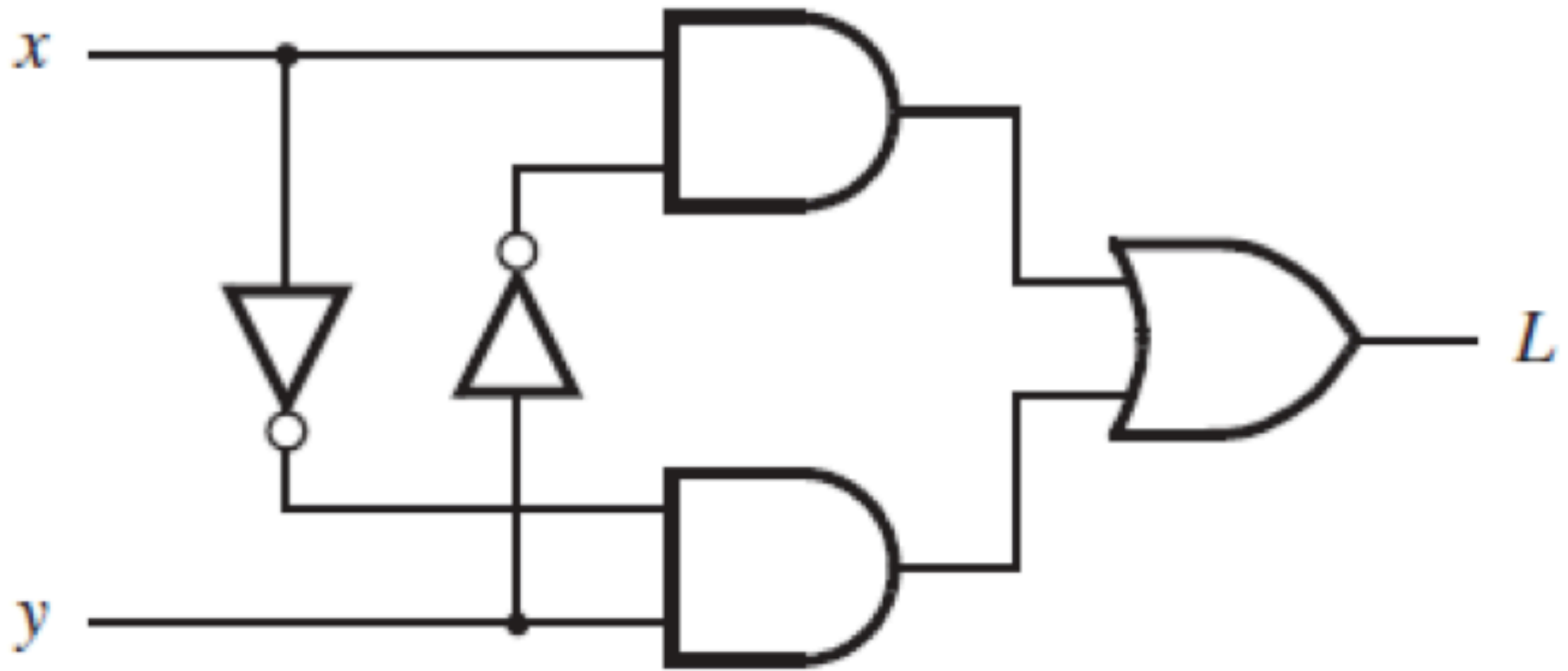


[Figure 2.11c from the textbook]

XOR Analysis (x=0, y=1)

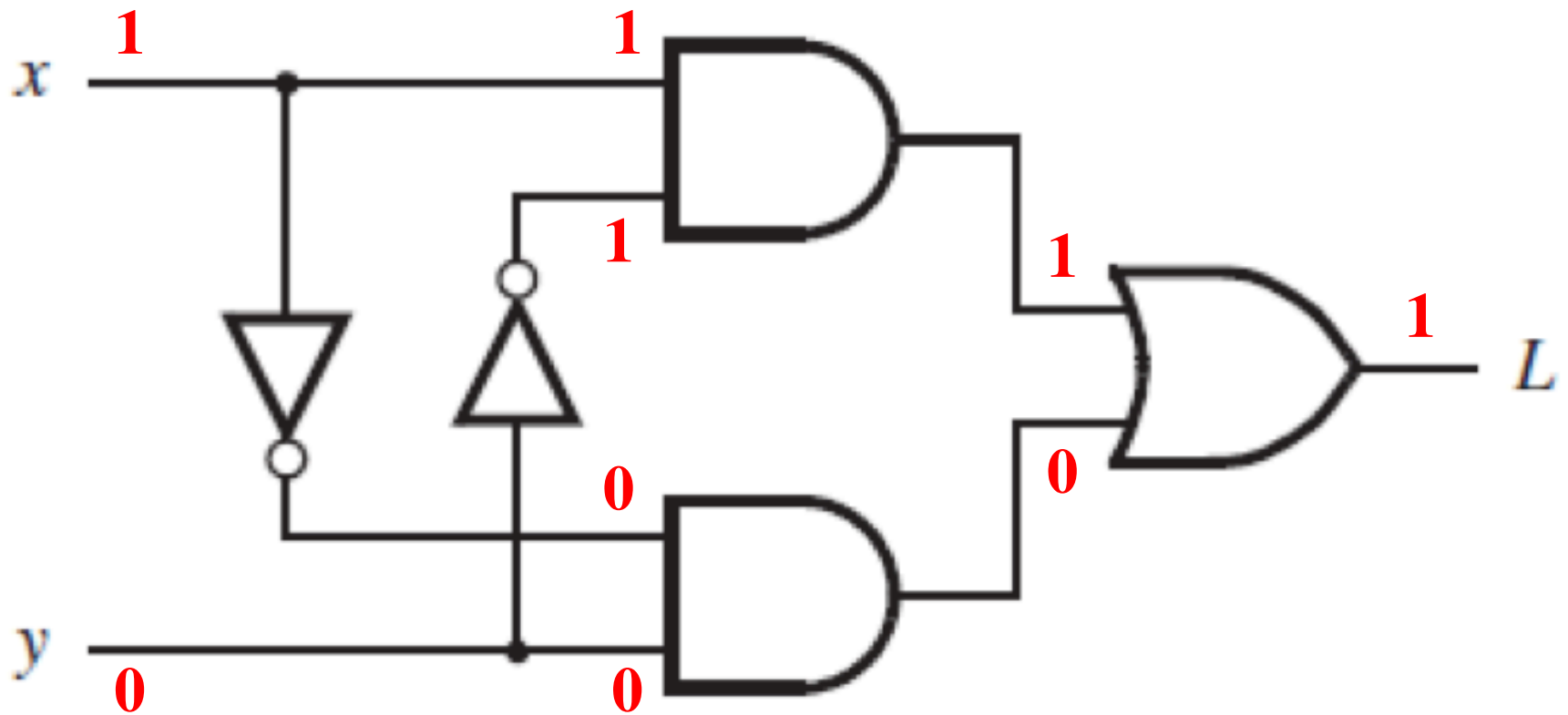


XOR Analysis

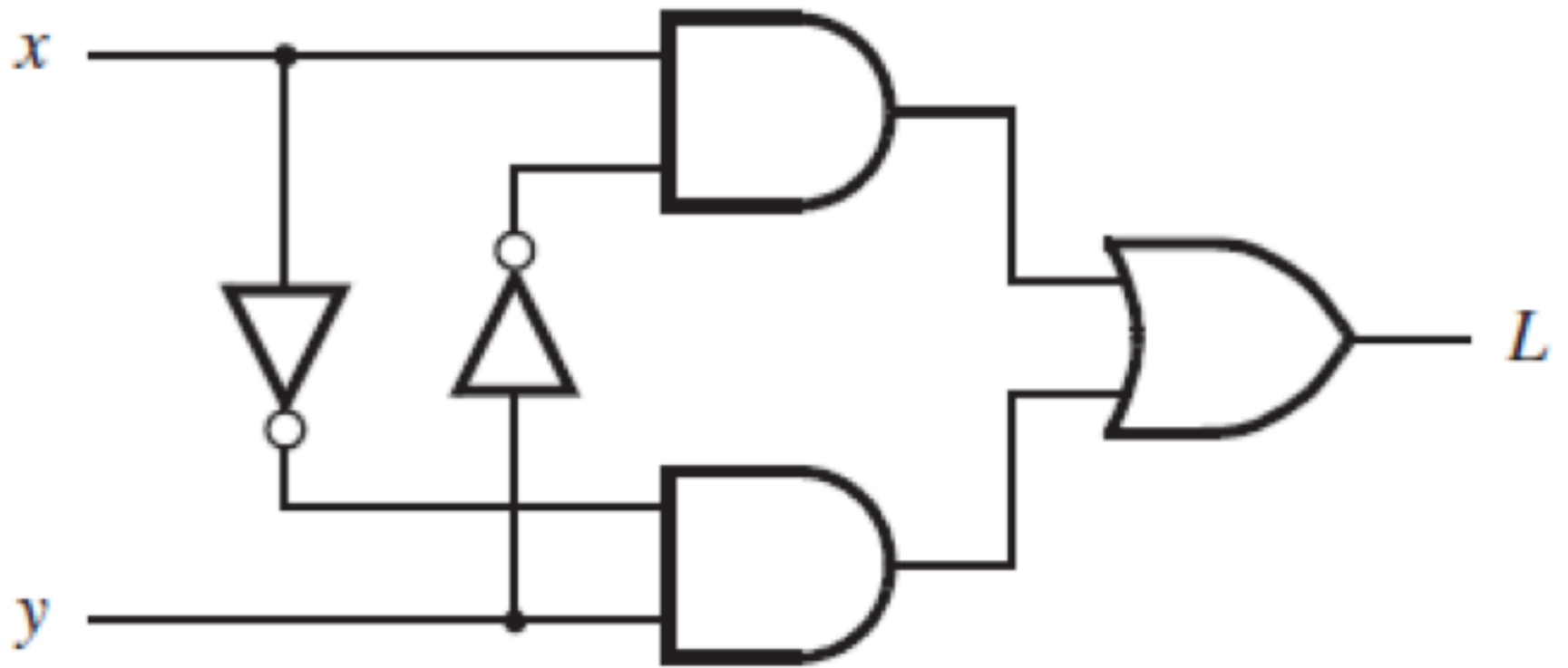


[Figure 2.11c from the textbook]

XOR Analysis (x=1, y=0)

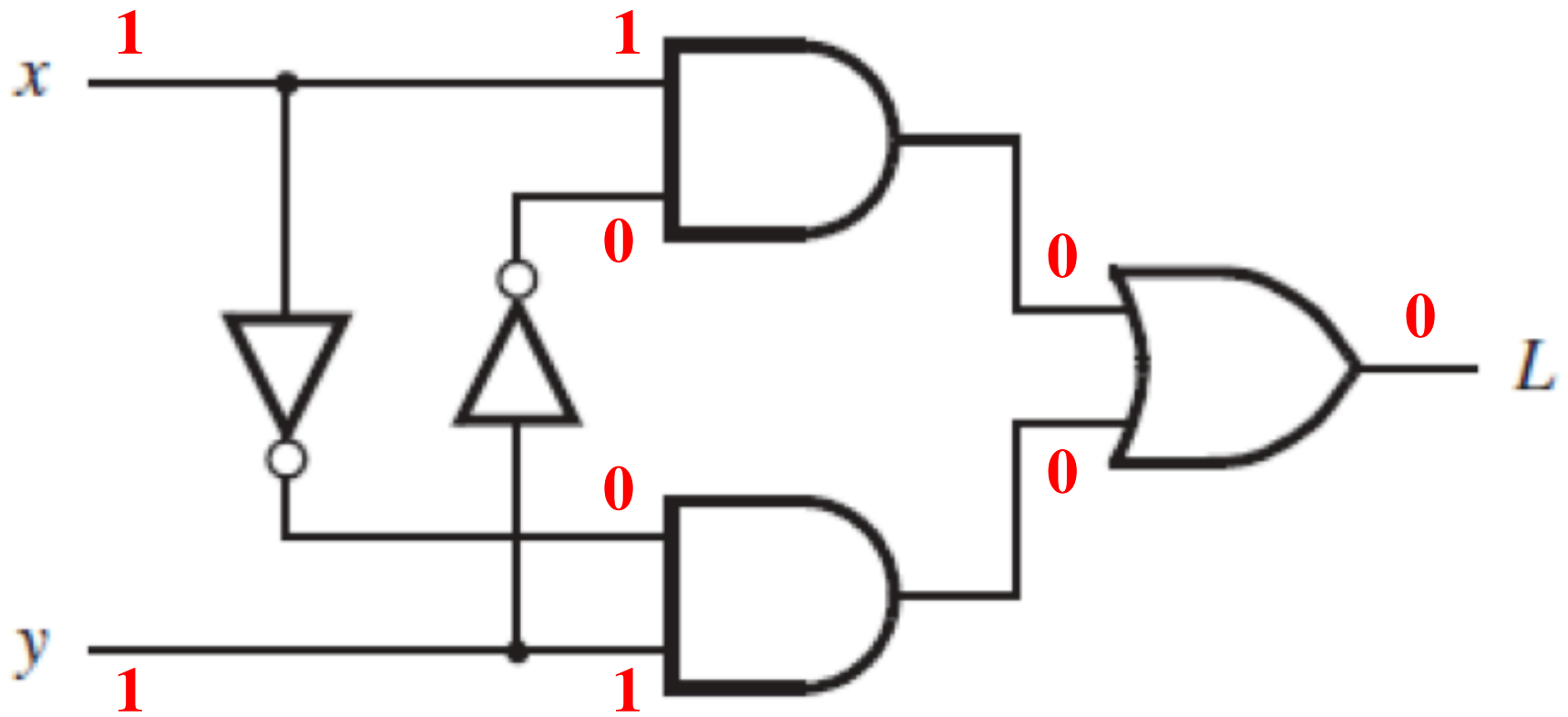


XOR Analysis



[Figure 2.11c from the textbook]

XOR Analysis (x=1, y=1)



Truth Table for XOR



| x | y | L |
|-----|-----|-----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Truth Table for XOR



| x | y | L |
|-----|-----|-----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The output is 1 only if both inputs are different.

Addition of Binary Numbers

| | | | | |
|-----------|-------|-------|-------|-------|
| a | 0 | 0 | 1 | 1 |
| $+b$ | $+0$ | $+1$ | $+0$ | $+1$ |
| <hr/> | <hr/> | <hr/> | <hr/> | <hr/> |
| $s_1 s_0$ | 0 0 | 0 1 | 0 1 | 1 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

| | | | | |
|---|------------|------------|------------|------------|
| <i>a</i> | 0 | 0 | 1 | 1 |
| <u>+ <i>b</i></u> | <u>+ 0</u> | <u>+ 1</u> | <u>+ 0</u> | <u>+ 1</u> |
| <i>s</i> ₁ <i>s</i> ₀ | 0 0 | 0 1 | 0 1 | 1 0 |

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

| | | | | |
|-----------|----------|----------|----------|----------|
| a | 0 | 0 | 1 | 1 |
| $+b$ | $+0$ | $+1$ | $+0$ | $+1$ |
| \hline | \hline | \hline | \hline | \hline |
| $s_1 s_0$ | 0 0 | 0 1 | 0 1 | 1 0 |

| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

| | | | | |
|---|------------|------------|------------|------------|
| <i>a</i> | 0 | 0 | 1 | 1 |
| <u>+ <i>b</i></u> | <u>+ 0</u> | <u>+ 1</u> | <u>+ 0</u> | <u>+ 1</u> |
| <i>s</i> ₁ <i>s</i> ₀ | 0 0 | 0 1 | 0 1 | 1 0 |

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

| | | | | |
|-----------|------|------|------|------|
| a | 0 | 0 | 1 | 1 |
| $+b$ | $+0$ | $+1$ | $+0$ | $+1$ |
| $s_1 s_0$ | 0 0 | 0 1 | 0 1 | 1 0 |

| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 \ 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 \ 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 \ 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 \ 0 \end{array}$$

| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 \ 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 \ 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 \ 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 \ 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 \boxed{s_0} \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 \boxed{0} \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 \boxed{1} \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 \boxed{1} \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 \boxed{0} \end{array}$$

| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

$$\begin{array}{r} a \\ + b \\ \hline s_1 s_0 \end{array} \quad \begin{array}{r} 0 \\ + 0 \\ \hline 0 0 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 0 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 1 0 \end{array}$$

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

?

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

AND

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

?

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

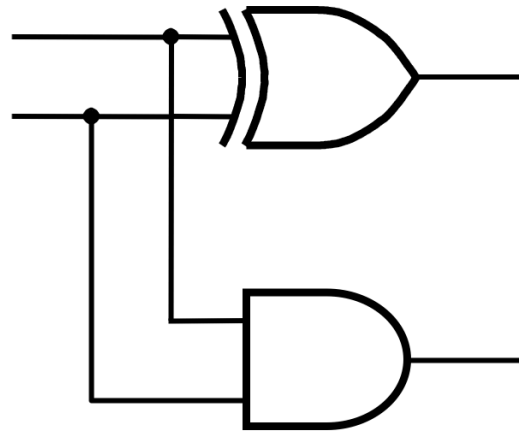
XOR

| <i>a</i> | <i>b</i> | <i>s</i> ₁ | <i>s</i> ₀ |
|----------|----------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers

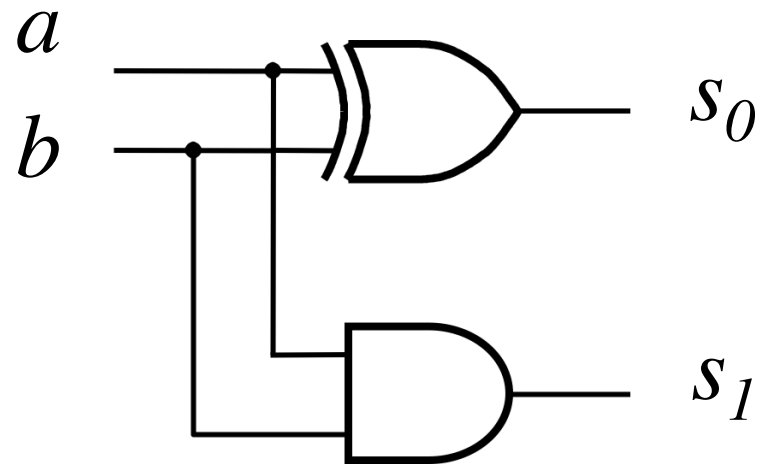
| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Addition of Binary Numbers



| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

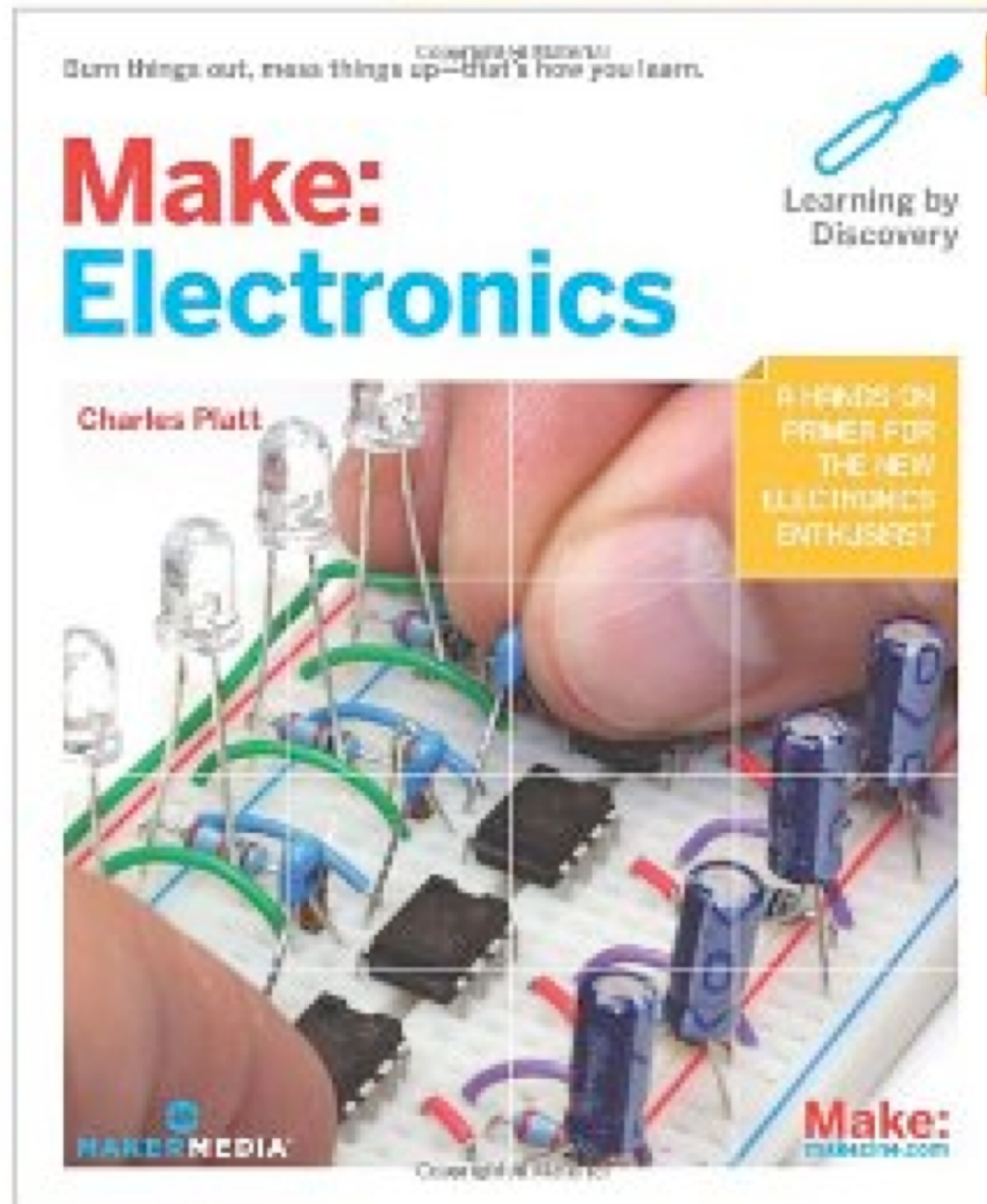
Addition of Binary Numbers

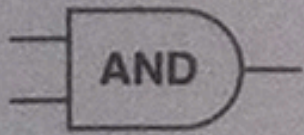


| a | b | s_1 | s_0 |
|-----|-----|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

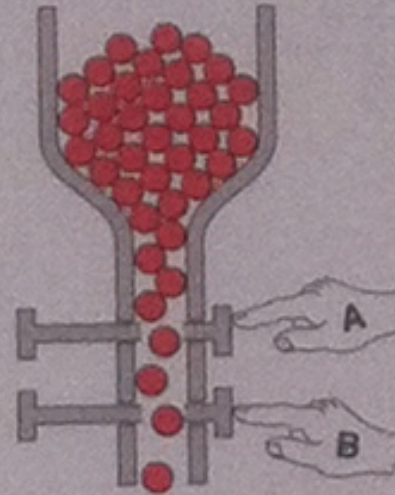
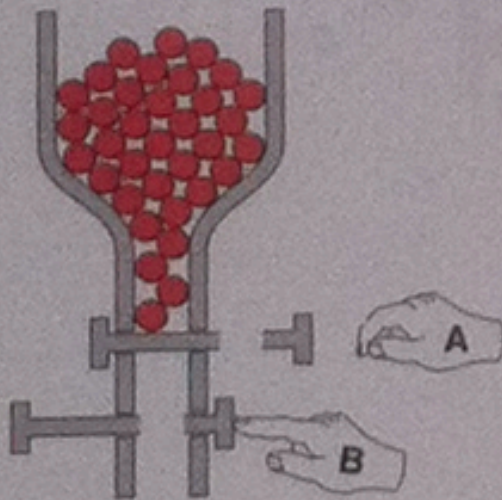
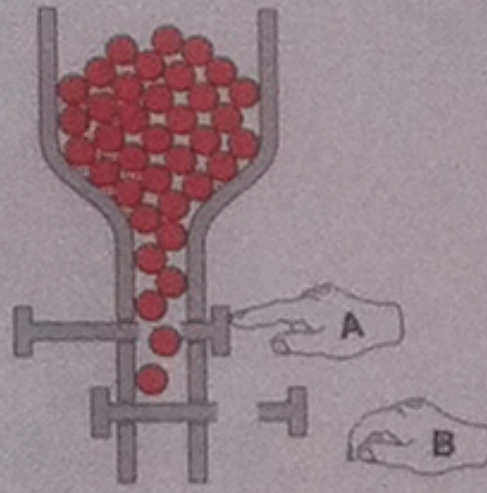
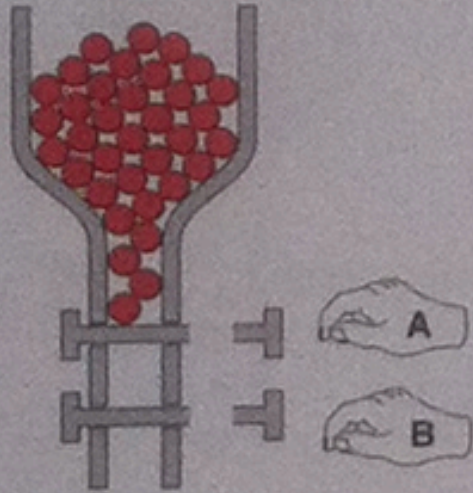
The following examples came from this book

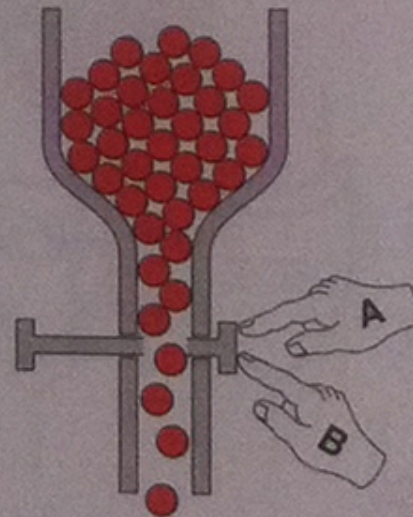
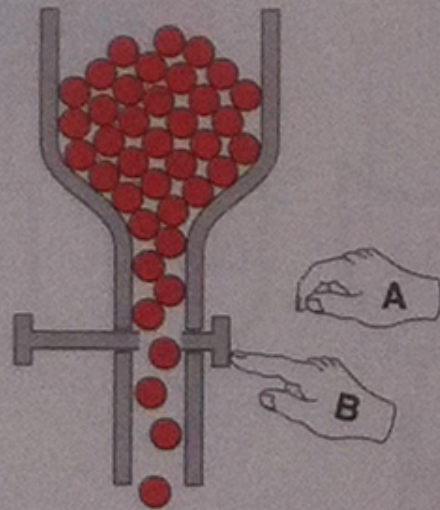
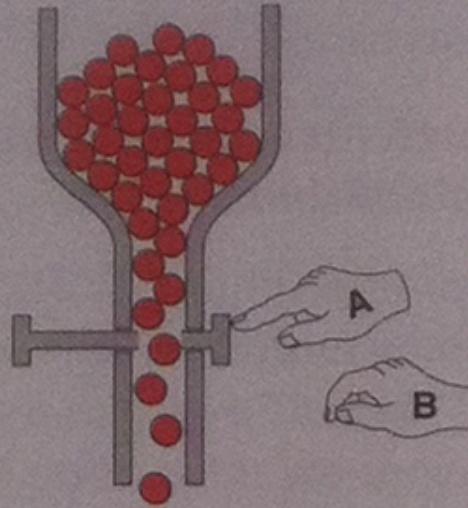
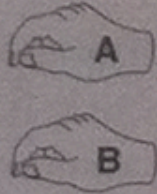
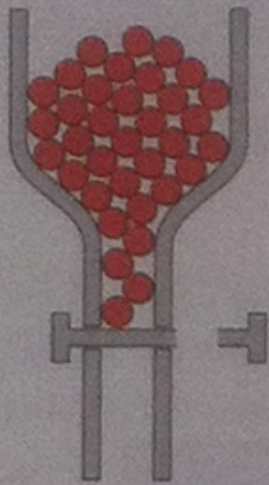
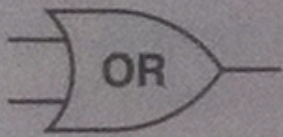
Click to **LOOK INSIDE!**



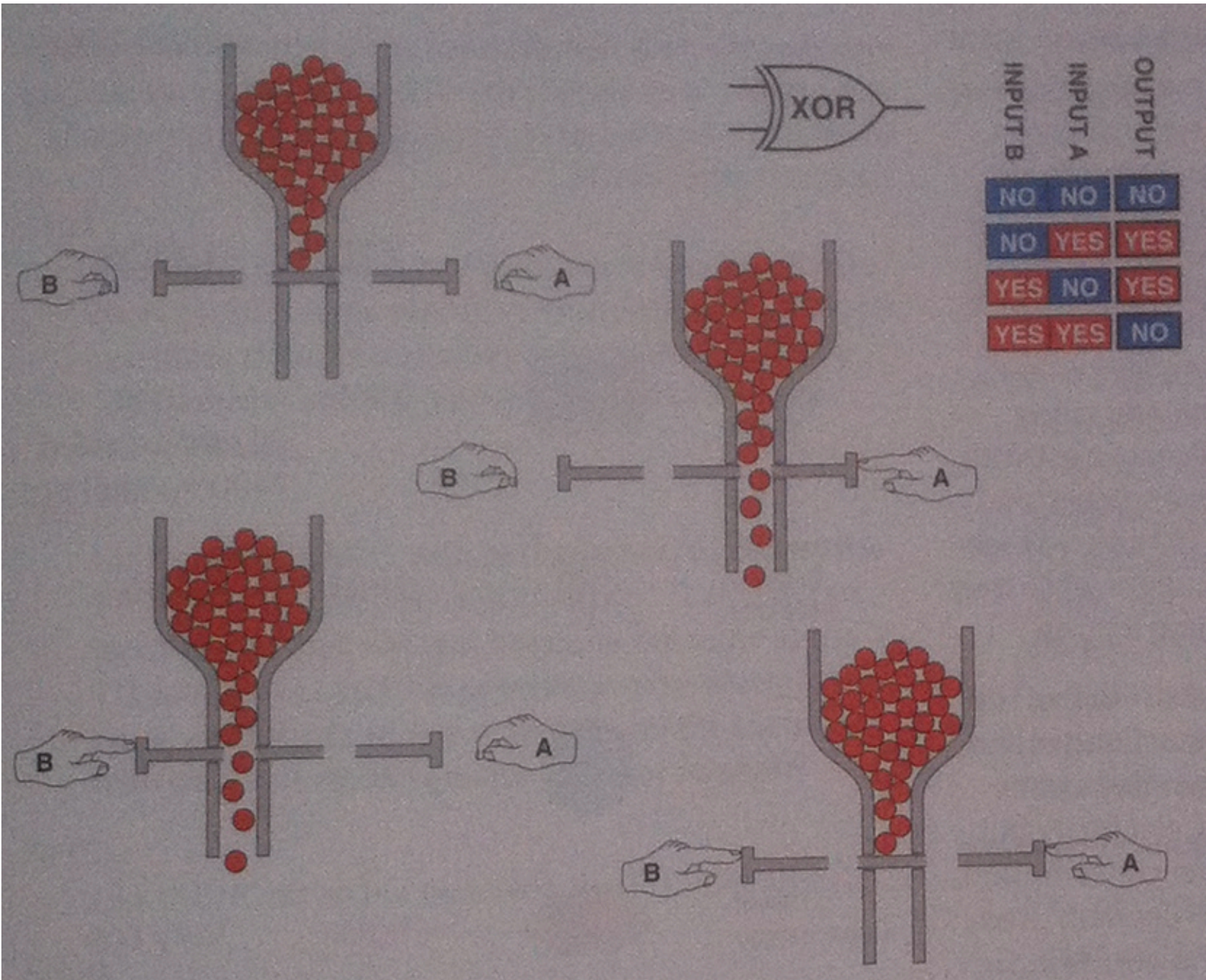


| INPUT B | INPUT A | OUTPUT |
|---------|---------|--------|
| NO | NO | NO |
| NO | YES | NO |
| YES | NO | NO |
| YES | YES | YES |





| INPUT B | INPUT A | OUTPUT |
|---------|---------|--------|
| NO | NO | NO |
| NO | YES | YES |
| YES | NO | YES |
| YES | YES | YES |



Questions?

THE END