CprE 281 HW7

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Multiplexers, Decoders, and Encoders
Assigned Date: Eighth Week
Finish by Oct. 17, 2022

P1 (10 points). Consider a 2-to-1 multiplexer:

a. Draw the gate level implementation using only 2 AND gates, 1 OR gate, and 1 NOT gate.
b. Write the **POS** expression for the multiplexer

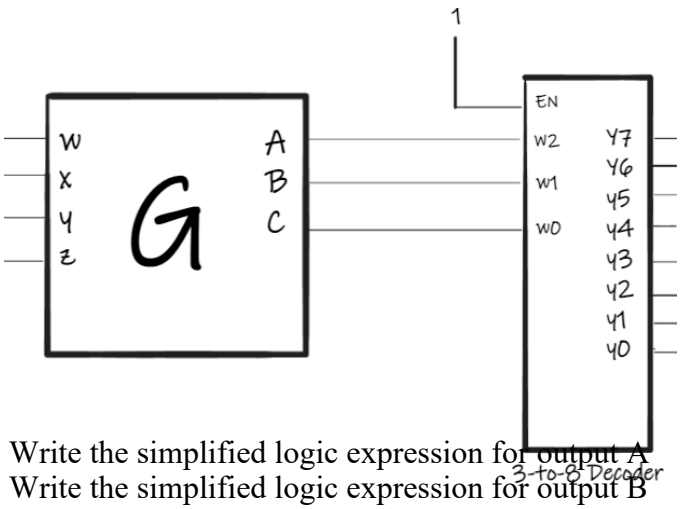
P2 (15 points). Using the specified circuit element(s), implement the following:

a. One 3 input OR gate using only two 2-to-1 multiplexers
b. One 2 input OR gate using only four 1-to-2 decoders (hint: Use the enable bit)
c. One 2 input NOR gate using only one 2-to-4 decoder

P3 (10points). Answer the following questions about decoders and MUXes:

a. How many 2-to-4 decoders are necessary to create a 4-to-16 decoder?
b. How many 3-to-8 decoders are necessary to create a 6-to-64 decoder?
c. How many 1-bit 2-to-1 MUXes are necessary to create a 1-bit 8-to-1 MUX?
d. How many 1-bit 2-to-1 MUXes are necessary to create an 8-bit 2-to-1 MUX?

P4 (20 points). Logic block G represents a 4-input logic circuit with 3 outputs controlling a decoder. Design G, such that the outputs match the truth table shown. Assume the decoder is active high and is always enabled.



A. Write the simplified logic expression for output A
B. Write the simplified logic expression for output B
C. Write the simplified logic expression for output C

w	x	y	z	Out
0	0	0	0	Y7
0	0	0	1	Y5
0	0	1	0	Y4
0	0	1	1	Y3
0	1	0	0	Y2
0	1	0	1	Y1
0	1	1	0	Y6
0	1	1	1	Y3
1	0	0	0	Y2
1	0	0	1	Y1
1	0	1	0	Y0
1	0	1	1	Y1
1	1	0	0	Y7
1	1	0	1	Y4
1	1	1	0	Y7
1	1	1	1	Y6

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P5 (20 points). Implement the following functions using a single 4-input multiplexer. Use the given variables for select lines. You may assume you have additional gates readily available, that is you may write an expression at the input of the multiplexer.
Hint: Use Shannon Expansion, then simplify gate expressions

a. $F(A,B,C,D) = \sum m(0,1,3,5,6,8,9,11,12,13)$ with select lines A and B
b. $F(A,B,C,D) = \sum m(0,7,8,9,10,11,15)$ with select lines B and C
c. $F(A,B,C,D) = \prod M(2,4,6,7,8,12)$ with select lines C and D
d. $F(A,B,C,D) = \prod M(0,2,3,4,5,6,7,10,11)$ with select lines A and D

P6 (10 points). Write Verilog code for an 8-to-3 priority encoder

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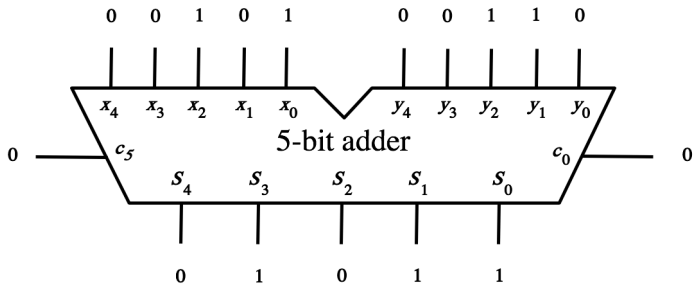
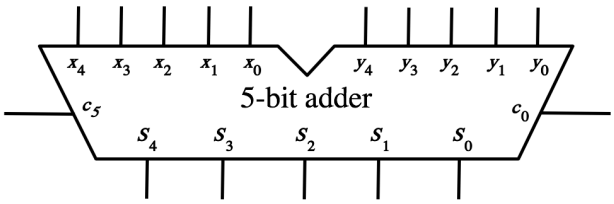
P7. (15 points) For each of the following, assign either a 0 or a 1 to each input and output of the 5-bit adder such that it computes the given expression. In all problems, the binary numbers are stored in 2's complement representation. The problem in a) is already solved.

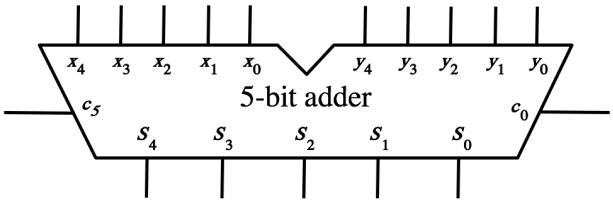
a) **(+5) + (+6) = +11**



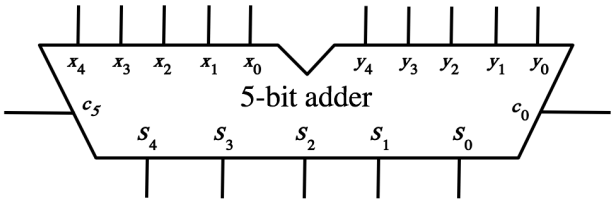
b) **(+12) + (+4) =**



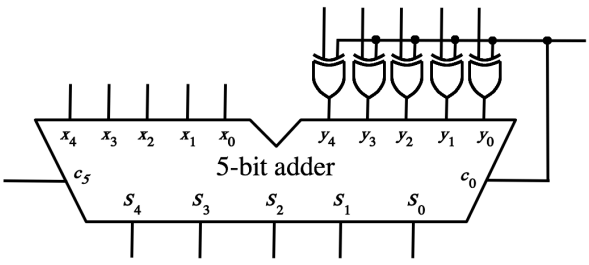
c) **(-15) + (+8) =**



d) **(+9) + (-6) =**



e) **(+4) + (-14) =**



f) **(-6) - (-5) =**