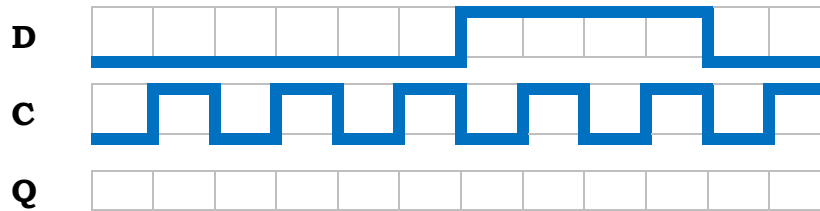
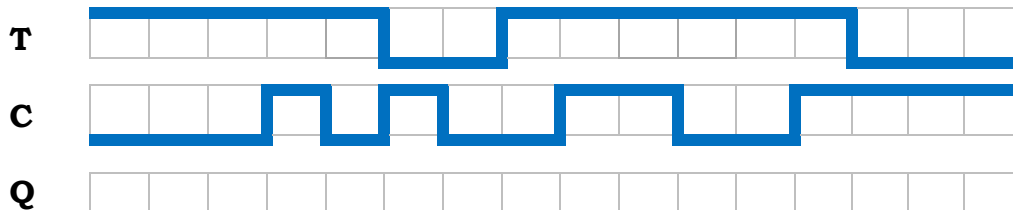


P1 (20 points): Complete the following timing diagrams for the specified components. The clock is C. You may assume that Q is initially at 0 unless specified otherwise.

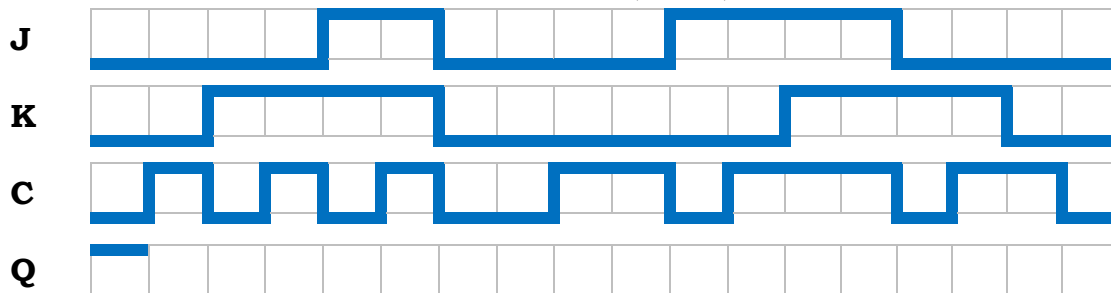
A: A positive-edge-triggered D Flip-Flop (DFF).



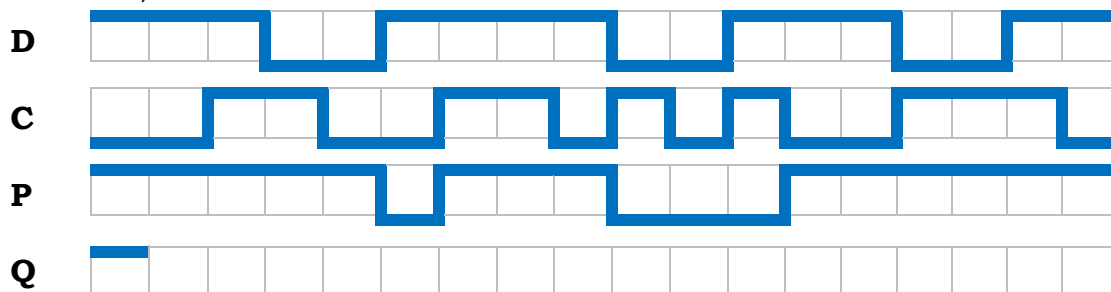
B: A negative-edge-triggered T Flip-Flop (TFF).



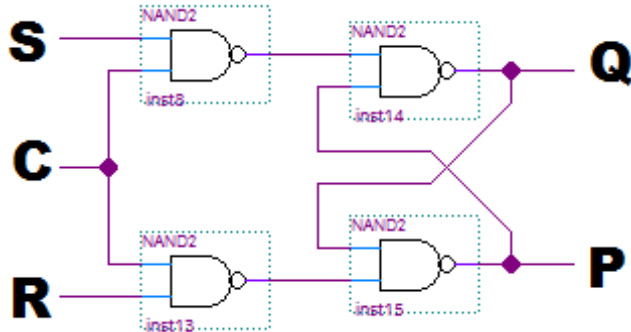
C: A positive-edge-triggered JK Flip-Flop (JKFF).



D: A negative-edge-triggered DFF with active-low Preset P (preset occurs when P=0).



P2 (15 points): Given the circuit below, answer the following questions:



A: What type of circuit is this?

B: Fill in the following characteristic table.

C	S	R	Q	P
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

C. For which input combinations is the circuit in a memory state? Which state is considered undesirable?

P3 (20 points): 1-to-8 demultiplexer

- a) Write the Boolean functions for the outputs of a 1-to-8 demultiplexer that an input F with select lines {A, B, C}.

- b) Implement the demultiplexer using AND, and NOT gates.

- c) Implement the demultiplexer using 1-to-2 demultiplexers and a minimal number of additional gates

- d) Implement the multiplexer using 1-to-4 demultiplexers and a minimal number of additional gates

Due Date: Oct. 24, 2022

P4 (10 Points) Complete the following circuits by drawing additional logic gates, components, or wires to implement the specified flip-flop given another flip-flop type. Label all inputs and outputs.

- a. Implement a T Flip-Flop using a D Flip-Flop
- b. Implement a D Flip-Flop using a T Flip-Flop
- c. Implement a T Flip-Flop using a JK Flip-Flop
- d. Implement a JK Flip-Flop using a D Flip-Flop
- e. Implement a JK Flip-Flop using a T Flip-Flop

Due Date: Oct. 24, 2022

P5 (15 points): Given a 3-bit input A, 1-bit input P, 1-bit input Q, a 6-bit adder, some 2-to-1 MUXes, some NOT gates, and some XOR gates:

- A. Design a circuit that produces a 6-bit integer X such that $B=6+2A$ if $P=0$ and produces $B=8-2A$ if $P=1$.
- B. Design a circuit that produces a 6-bit integer Y such that $C=5A$ if $P=0$ and produces $C=9A+1$ if $P=1$.
- C. Design a circuit that outputs 6-bit integer such that $D=B$ if $Q=0$ and $D=C$ if $Q=1$.

P6 (20 points): Answer the following questions about the Negative-Edge-Triggered Master-Slave DFF with PRESET_N and CLEAR_N connections, as shown in Figure 5.12 from the book. Suppose that $D=1$ and $CLK=0$. Answer the following questions about Q.

- a) Ignoring PRESET_N and CLEAR_N (assume that they are not connected), what effect does pulsing the clock have on Q in this circuit?
- b) What effect does pulsing PRESET_N have on this circuit?
- c) What effect does pulsing CLEAR_N have on this circuit?
- d) What will be the value of Q if PRESET_N=0 and CLEAR_N=1?
- e) What will be the value of Q if PRESET_N=0 and CLEAR_N=0?
- f) What will be the value of Q if the clock is pulsed while PRESET_N=0?
- g) What will be the value of Q if the clock is pulsed while CLEAR_N=0?
- h) What will be the value of Q if the clock is pulsed while CLEAR_N=1 and PRESET_N=1?