CprE 281 HW11 electrical and computer engineering iowa state university Basic Design Steps, State-Assignment Problems, Moore & Mealy Machines Assigned Date: Eleventh Week Finish by Nov. 16, 2022

P1 (20 points): Design and implement a Moore machine that detects the pattern 101 in its 1-bit serial input stream. Explain the logic behind your solution. Show your work for all steps discussed during the lectures: graph, state table, state-assigned table, truth tables, k-maps, expressions, circuit diagram.

P2 (15 points): The FSM state diagram below has two inputs  $x_1$  and  $x_0$ . In addition, it has two DFFs, three 4-to-1 MUXes, a single XOR gate, a single AND gate, and a single output bit Z. Answer the following questions about this FSM.



- A. Is this a Moore FSM or Mealy FSM?
- B. The state encodings are A=00, B=01, C=10, and D=11. Write a state-assigned table for this state diagram.
- C. Use K-maps to determine the expressions for the next-state variables.

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P3 (15 points): An FSM has two D flip-flops, an input w, and an output z. The circuit diagram is shown below.



- A. Find the logic expressions of  $Y_1$ ,  $Y_0$ , and the output z
- B. Show the state-assigned table of the FSM.
- C. Draw the state diagram of the FSM.

P4 (20 points): Draw a state diagram for a state machine that reads in a sequence of bits, one bit at a time, and outputs a 0 whenever the sequence 1010 is detected. It outputs a 1 otherwise. The machine keeps detecting the sequence and never stops.

- a. Using a Moore machine
- b. Using a Mealy machine

P5 (15 points): Consider the following state table for a FSM:

Present	Next State		Output
State	w=0	w=1	Z
А	А	В	0
В	В	С	1
С	С	D	0
D	D	А	1

- A. Draw the state diagram of the FSM
- B. Perform state minimization to minimize the number of states. Show your partitions in the procedure.
- C. Draw the new state diagram of the minimized FSM

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P6 (15 points): Reduce the state diagram below to use only 5 states:

