CprE 281: Digital Logic
Midterm 1: Friday Sep 23, 2022

Name: $\qquad$

Lab Section:
(circle one)

Tue 2-5 (\#9)
Wed 7-10 (\# 6)
Wed 11-2 (\#13)
Wed 6-9 (\#12)

## ID Number:

$\qquad$

Thur 8-11 (\#15)
Thur 11-2 (\#11)
Thur 2-5 (\# 8)
Thur 5-8 (\#7)

1. $\quad$ True/False Questions ( $10 \times 1 \mathrm{p}$ each $=10 \mathrm{p}$ )
(a) I forgot to write down my name, student ID number, and lab section. TRUE / FALSE
(b) The circuit in the CprE 281 class logo is called a "half-adder." TRUE / FALSE
(c) For the same function, the SOP expression is shorter than the POS. TRUE / FALSE
(d) A POS expression is easily implementable with NOR-NOR logic. TRUE / FALSE
(e) When converting from base 6 to base 3, each digit in base 6 can be TRUE / FALSE directly mapped to two digits in base 3 .
(f) The shape of a K-Map with 8 input variables will be $8 x 8$.

TRUE / FALSE
(g) For 2-variable functions it is always true that $\Sigma \mathrm{m}(1,3)=\Pi \mathrm{M}(0,2) . \quad$ TRUE / FALSE
(h) These are ordered from small to large: Bantha, Rancor, Sarlacc. TRUE / FALSE
(i) $\mathrm{A} \overline{\mathrm{B}} \overline{\mathrm{C}}+\mathrm{ABC}=\mathrm{A}$.

TRUE / FALSE
(j) Behavioral-Procedural Verilog uses assign statements in the modules. TRUE / FALSE

## 2. Three-Variable K-map (5p)

Derive the minimum-cost POS expression for $F(a, b, c)$ that is specified with this K-map.

3.Truth Table and Venn Diagram ( $5 p+5 p=10 p$ )
(a) Draw the truth table for the following Boolean function:

$$
f(x, y, z)=\bar{x}(y z+\bar{y})
$$

(b) Draw the Venn diagram that corresponds to this K-map:

| y $\mathbf{z}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| x | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

4. Number Conversions ( $5 \times 4 p$ each $=20 p$ )
(a) Convert 101011012 to decimal
(b) Convert $91_{10}$ to binary
(c) Convert $16510^{10}$ to hexadecimal
(d) Convert 3124 to octal
(e) Find the value of $X$ that satisfies: $10_{5}+106+10_{7}=X_{8}$
5. Verilog Code (10p)
a) Draw the circuit diagram that corresponds to the Structural Verilog module shown below. Clearly label all inputs, outputs and wires of your circuit
module mystery(A, B, F);
input $A, B$;
output F;
not(W, A);
$\operatorname{not}(X, B) ;$
$\operatorname{and}(\mathbf{Y}, \mathbf{A}, \mathbf{X})$;
and(Z, W, B);
$\operatorname{or}(\mathbf{F}, \mathbf{Y}, \mathbf{Z})$;
endmodule
b) Now write the Behavioral-Continuous Verilog code for the circuit above.
6. Waveform ( $3 \times 5 \mathrm{p}=15 \mathrm{p}$ )
(a) Given this Questa Sim waveform, draw the corresponding K-map for $F(A, B, C, D)$.



(b) Use the K-map from (a) to derive the minimum-cost Sum-of-Products (SOP) expression for $\mathbf{F}$.
(c) Draw the circuit for the minimum SOP expression. Label all inputs and outputs.
7. Derive the minimum POS expression using a K-map $(10 p+5 p=15 p)$
(a) Use a K-map to derive the minimum-cost POS expression for the following function $f(\mathrm{a}, \mathrm{b}, \mathrm{c}, \mathrm{d})=\Pi \mathrm{M}(1,4,6,7,9,10,12,14,15)+\mathrm{D}(3,5,13)$.
(b) Draw the circuit diagram for the minimum-cost Product-Of-Sums (POS) expression. Clearly label all inputs and outputs.
8. Redraw the Circuit ( $3 \times 5 p=15 p$ )
(a) Write the Boolean expression that corresponds to this circuit (do not simplify it yet).

(b) Use the theorems and axioms of Boolean algebra to simplify the expression that corresponds to the circuit form (a) into a minimum-cost SOP expression.
(c) Use the minimum-cost SOP expression to redraw the circuit using only basic logic gates with at most 2-inputs each (i.e., only AND, OR, NOT gates).
9. Minimization and NAND implementation ( $3 \times 5 p=15 p$ )
(a) Draw the K-map that corresponds to the following Boolean function:

$$
\mathbf{f}=\overline{\mathbf{a}} \mathbf{b} \mathbf{d}+\mathbf{a} \mathbf{b} \overline{\mathbf{c}} \mathbf{d}+\mathbf{b} \overline{\mathbf{c}} \overline{\mathbf{d}}+\mathbf{a} \mathbf{b} \mathbf{c}+\overline{\mathbf{b}} \mathbf{d}
$$

(b) Redraw the K-map from (a) and derive the minimum-cost SOP expression for f .
(c) Draw the circuit for the minimum-cost SOP expression using only NAND gates. Clearly label all inputs and outputs.
10. Boolean Algebra (15p)

Use the theorems and axioms of Boolean algebra to simplify the following expression:

$$
\mathbf{F}=\overline{\mathbf{A} B}(\overline{\mathbf{B}}+\mathbf{A B C})+\overline{\mathbf{C}} \overline{\overline{\mathbf{B}}} \overline{\mathbf{A}}+\overline{\overline{\mathbf{A B}} \mathbf{C}}+\overline{\mathbf{C}}(\overline{\mathbf{A}} \overline{\mathbf{B}}+\overline{\mathbf{A}} \mathbf{B}+\mathbf{A})
$$

| Question | Max | Score |
| :--- | ---: | ---: |
| 1. True/False | 10 |  |
| 2. Three-variable K-map | 5 |  |
| 3. Truth Table \& Venn D. | 10 |  |
| 4. Number Conversions | 20 |  |
| 5. Verilog Code | 10 |  |
| 6. Waveform | 15 |  |
| 7. POS with K-map | 15 |  |
| 8. Redraw the Circuit | 15 |  |
| 9. Minimization \& NAND | 15 |  |
| 10. Boolean Algebra | 15 |  |
| TOTAL: | 130 |  |

