CprE 281: Digital Logic
Midterm 1: Friday Sep 23, 2022

Sample Solutions

Name: ______________________________ **ID Number:** ______________

Lab Section:	**Tue 2-5 (#9)**	**Wed 7-10 (# 6)**	**Thur 8-11 (#15)**
(circle one)		**Wed 11-2 (#13)**	**Thur 11-2 (#11)**
		Wed 6-9 (#12)	**Thur 2-5 (# 8)**
			Thur 5-8 (# 7)

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name, student ID number, and lab section. TRUE / **FALSE**

(b) The circuit in the CprE 281 class logo is called a "half-adder." **TRUE** / FALSE

(c) For the same function, the SOP expression is shorter than the POS. TRUE / **FALSE**

(d) A POS expression is easily implementable with NOR-NOR logic. **TRUE** / FALSE

(e) When converting from base 6 to base 3, each digit in base 6 can be directly mapped to two digits in base 3. TRUE / **FALSE**

(f) The shape of a K-Map with 8 input variables will be 8x8. TRUE / **FALSE**

(g) For 2-variable functions it is always true that Σ m(1, 3) = Π M(0, 2). **TRUE** / FALSE

(h) These are ordered from small to large: Bantha, Rancor, Sarlacc. **TRUE** / FALSE

(i) $A \overline{B}\,\overline{C} + A B C = A$. TRUE / **FALSE**

(j) Behavioral-Procedural Verilog uses assign statements in the modules. TRUE / **FALSE**

2. Three-Variable K-map (5p)

Derive the minimum-cost POS expression for F(a,b,c) that is specified with this K-map.

c \ ab	00	01	11	10
0	1	0	1	0
1	0	0	0	1

$(a+\overline{b})$, $(\overline{a}+b+c)$, $(a+\overline{c})$, $(\overline{b}+\overline{c})$

$$F = (a+\overline{b}) \cdot (\overline{a}+b+c) \cdot (a+\overline{c}) \cdot (\overline{b}+\overline{c})$$

3.Truth Table and Venn Diagram (5p + 5p = 10p)

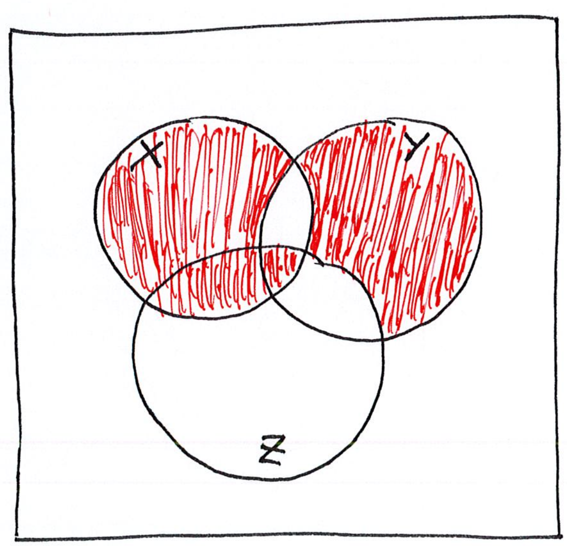
(a) Draw the truth table for the following Boolean function:

$$f(x, y, z) = \bar{x}\,(yz + \bar{y})$$

x y z	$\bar{x}$	yz	+	$\bar{y}$	f
0 0 0	1	0	1	1	1
0 0 1	1	0	1	1	1
0 1 0	1	0	0	0	0
0 1 1	1	1	1	0	1
1 0 0	0	0	1	1	0
1 0 1	0	0	1	1	0
1 1 0	0	0	0	0	0
1 1 1	0	1	1	0	0

(b) Draw the Venn diagram that corresponds to this K-map:

x \ yz	00	01	11	10
0	0	0	0	1
1	1	1	1	0



4. **Number Conversions (5 x 4p each = 20p)**

(a) Convert 101011101_2 to decimal

$1\times2^7 + 0\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0 =$

$= 128 + 32 + 8 + 4 + 1 = 128 + 40 + 5 = 168 + 5$

$= 173_{10}$

(b) Convert 91_{10} to binary

91/2 =	45	1
45/2 =	22	1
22/2 =	11	0
11/2 =	5	1
5/2 =	2	1
2/2 =	1	0
1/2 =	0	1

1011011_2

(c) Convert 165_{10} to hexadecimal

165 / 16 =	10	5
10 / 16 =	0	10 = A

$A5_{16}$

(d) Convert 312_4 to octal

11 01 10

11 0|1 10

6 6

Convert to binary, then to octal.

$312_4 = 66_8$

(e) Find the value of X that satisfies: $10_5 + 10_6 + 10_7 = X_8$

18 / 8 =	2	2
2/8 =	0	2

$5_{10} + 6_{10} + 7_{10}$

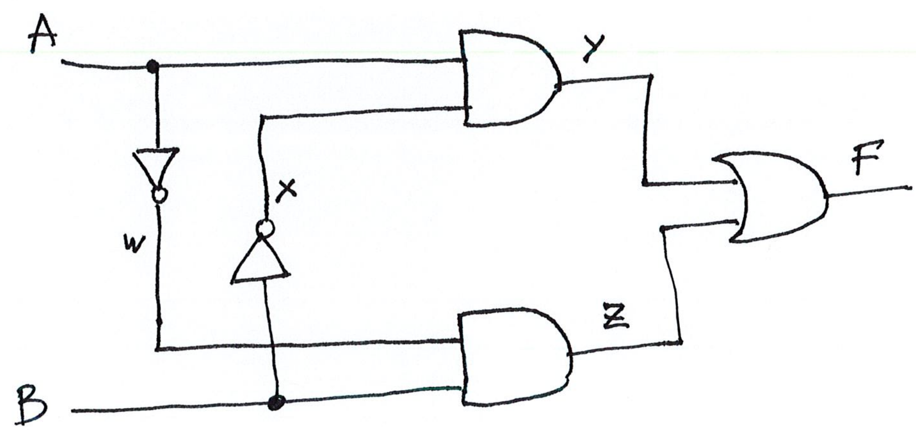
$18_{10} = 22_8$.

$\Rightarrow X = 22$

5. Verilog Code (10p)

a) Draw the circuit diagram that corresponds to the Structural Verilog module shown below. Clearly label all inputs, outputs and wires of your circuit

```
module mystery(A, B, F);
    input A, B;
    output F;
    not(W, A);
    not(X, B);
    and(Y, A, X);
    and(Z, W, B);
    or(F, Y, Z);
endmodule
```



$F = A\bar{B} + \bar{A}B$ This is an XOR.

b) Now write the Behavioral-Continuous Verilog code for the circuit above.

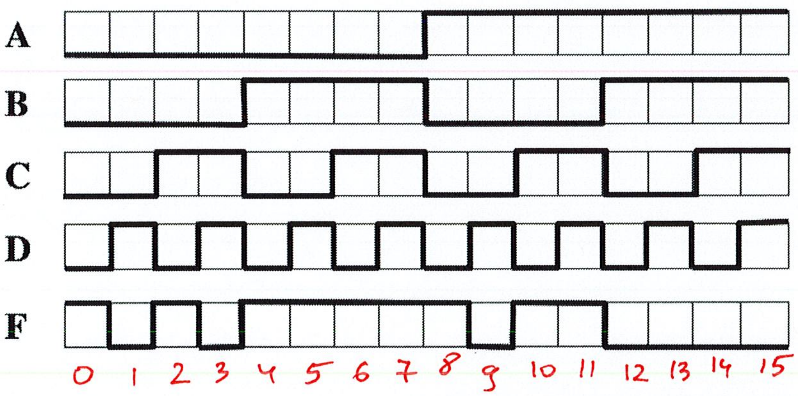
```
module mystery (A, B, F);
  input A, B;
  output F;
  assign F = (~A&B)|(A&~B);
endmodule
```

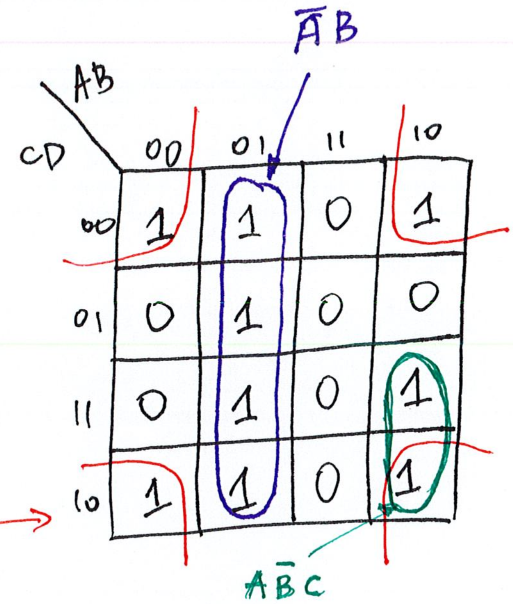
also OK

Note: assign F = A ^ B;

6. Waveform (3 x 5p = 15p)

(a) Given this Questa Sim waveform, draw the corresponding K-map for F(A, B, C, D).

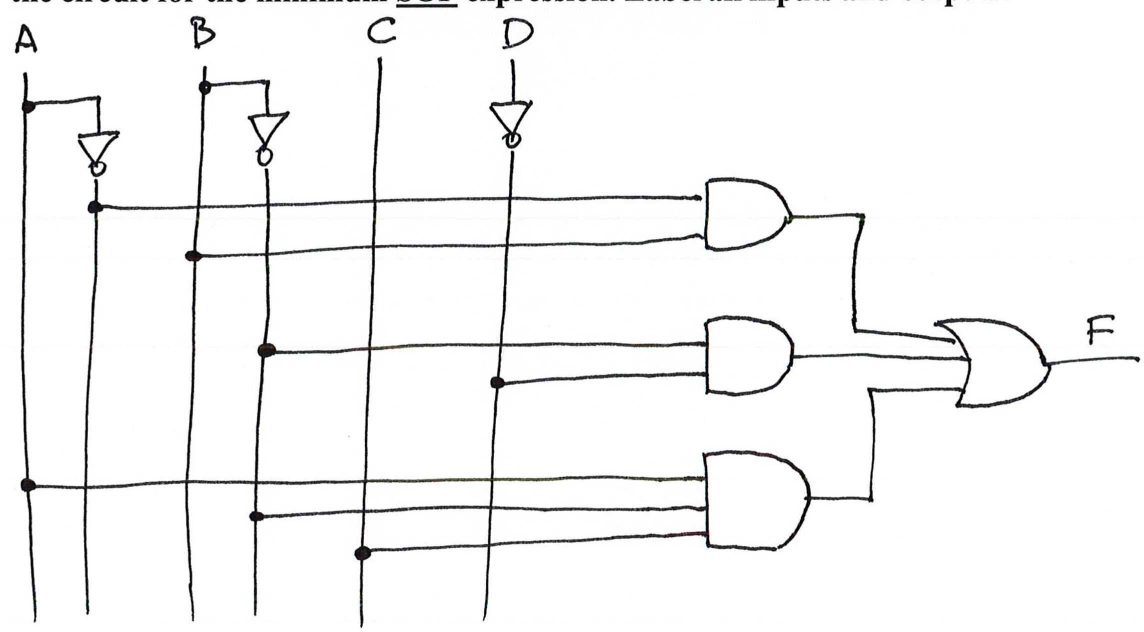




(b) Use the K-map from (a) to derive the minimum-cost Sum-of-Products (SOP) expression for F.

$$F = \bar{A}B + \bar{B}\bar{D} + A\bar{B}C$$

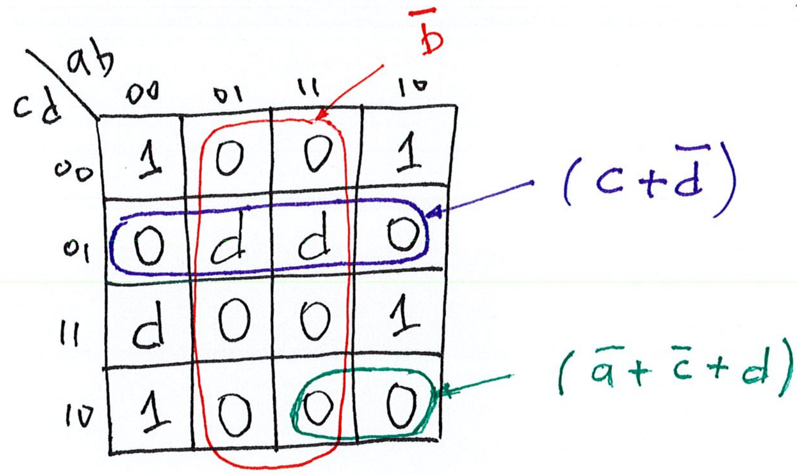
(c) Draw the circuit for the minimum SOP expression. Label all inputs and outputs.



7. Derive the minimum POS expression using a K-map (10p + 5p = 15p)

(a) Use a K-map to derive the minimum-cost POS expression for the following function

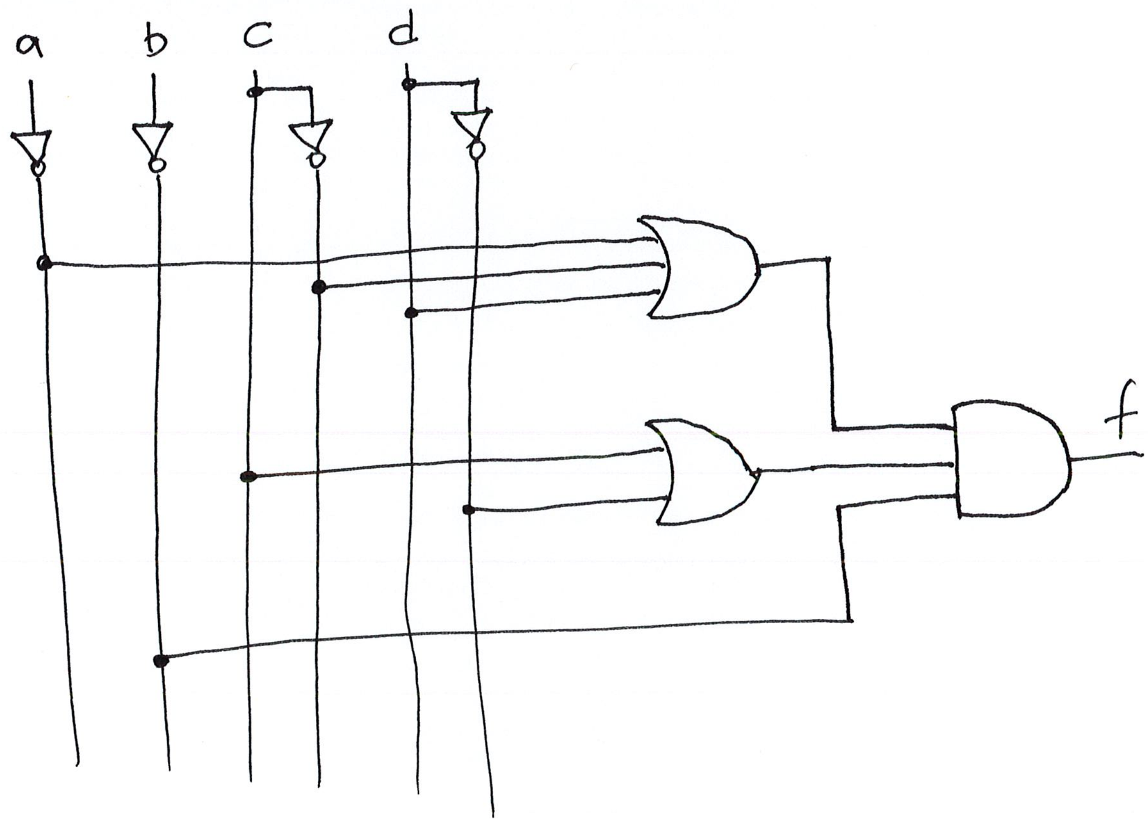
$$f(a,b,c,d) = \Pi M(1, 4, 6, 7, 9, 10, 12, 14, 15) + D(3, 5, 13).$$



cd \ ab	00	01	11	10
00	1	0	0	1
01	0	d	d	0
11	d	0	0	1
10	1	0	0	0

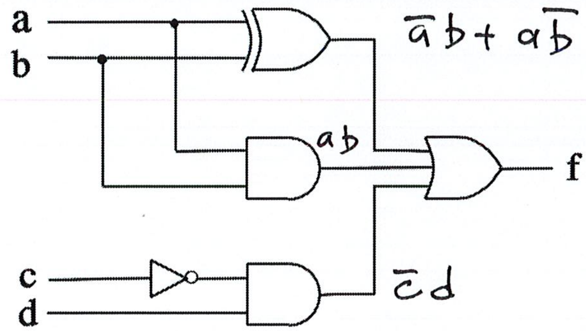
$$f = (\bar{a} + \bar{c} + d) \cdot (c + \bar{d}) \cdot \bar{b}$$

(b) Draw the circuit diagram for the minimum-cost Product-Of-Sums (POS) expression. Clearly label all inputs and outputs.



8. Redraw the Circuit (3 x 5p = 15p)

(a) Write the Boolean expression that corresponds to this circuit (do not simplify it yet).



$$f = \bar{a}b + a\bar{b} + ab + \bar{c}d$$

(b) Use the theorems and axioms of Boolean algebra to simplify the expression that corresponds to the circuit form (a) into a minimum-cost SOP expression.

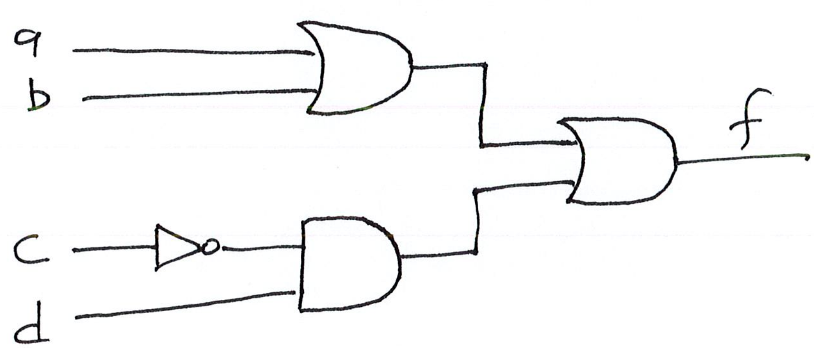
$$f = \bar{a}b + a\bar{b} + ab + \bar{c}d$$

$$= \bar{a}b + a(\bar{b} + b) + \bar{c}d \quad \text{// Theorem 8b}$$

$$= \bar{a}b + a + \bar{c}d \quad \text{// Theorem 16a}$$

$$= a + b + \bar{c}d.$$

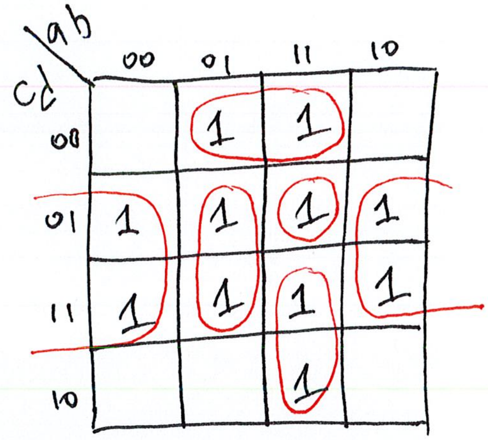
(c) Use the minimum-cost SOP expression to redraw the circuit using only basic logic gates with <u>at most 2-inputs</u> each (i.e., only AND, OR, NOT gates).



9. Minimization and NAND implementation (3 x 5p = 15p)

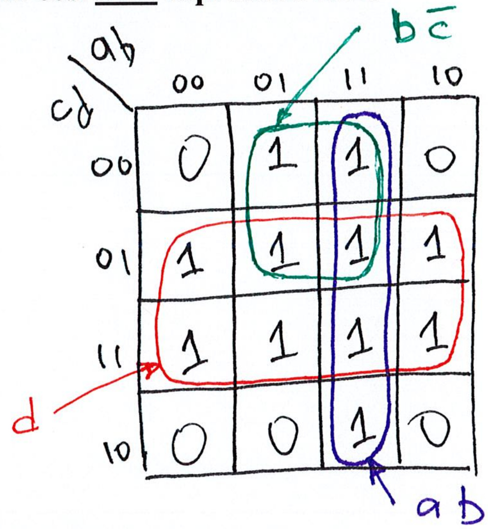
(a) Draw the K-map that corresponds to the following Boolean function:

$$f = \bar{a}\,b\,d + a\,b\,\bar{c}\,d + b\,\bar{c}\,\bar{d} + a\,b\,c + \bar{b}\,d$$

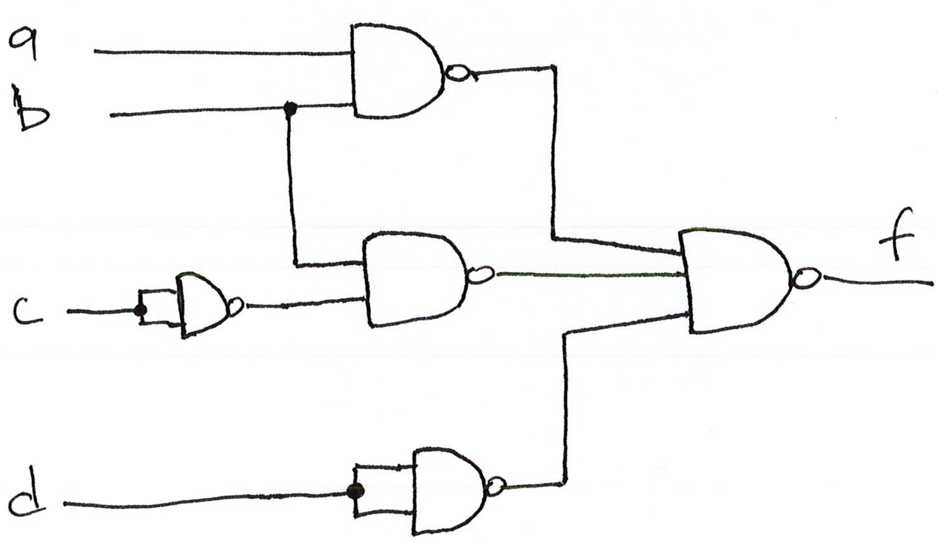


(b) Redraw the K-map from (a) and derive the minimum-cost SOP expression for f.

$f = ab + b\bar{c} + d$



(c) Draw the circuit for the minimum-cost SOP expression using only NAND gates. Clearly label all inputs and outputs.



10. Boolean Algebra (15p)

Use the theorems and axioms of Boolean algebra to simplify the following expression:

$$F = \overline{\bar{A}B(\bar{B}+ABC) + \overline{C\bar{B}}\,\bar{A} + \overline{\overline{AB}C} + \bar{C}(\bar{A}\bar{B}+\bar{A}B+A)} = \overline{\alpha+\beta+\gamma+\delta},$$

where

$$\alpha = \bar{A}B(\bar{B}+ABC) = \bar{A}\underbrace{B\bar{B}}_{0} + \underbrace{\bar{A}BA}_{0}BC = 0,$$

$$\beta = \overline{C\bar{B}}\,\bar{A} = (\bar{C}+\bar{\bar{B}})\bar{A} = \bar{C}\bar{A} + \bar{A}B,$$

$$\gamma = \overline{\overline{AB}C} = \overline{\overline{AB}} + \bar{C} = AB + \bar{C},$$

$$\delta = \bar{C}(\bar{A}\bar{B}+\bar{A}B+A) = \bar{C}(\bar{A}\underbrace{(\bar{B}+B)}_{1}+A) = \bar{C}\underbrace{(\bar{A}+A)}_{1} = \bar{C}.$$

$$F = \overline{\alpha+\beta+\gamma+\delta}$$

$$= \overline{0+\bar{C}A+\bar{A}B+AB+\underbrace{\bar{C}+\bar{C}}_{\bar{C}}}$$

$$= \overline{\bar{C}A+\underbrace{(\bar{A}+A)}_{1}B+\bar{C}}$$

$$= \overline{\bar{C}(A+1)+B}$$

$$= \overline{\bar{C}+B}$$

$$= \bar{\bar{C}}\cdot\bar{B}$$

$$= \bar{B}C.$$

Question	Max	Score
1. True/False	10	
2. Three-variable K-map	5	
3. Truth Table & Venn D.	10	
4. Number Conversions	20	
5. Verilog Code	10	
6. Waveform	15	
7. POS with K-map	15	
8. Redraw the Circuit	15	
9. Minimization & NAND	15	
10. Boolean Algebra	15	
TOTAL:	130	