

Instructions

Complete the questions below to the best of your ability. Do this on paper.
Once you are finished, upload a scanned PDF of your work to canvas.

Questions

P1. (10 points) Define the following terms in no more than 2 sentences each.

- A. ASIC
- B. ASCII
- C. FPGA
- D. VHDL

P2. (10 points) In the development process initial design-simulation-verification is one loop and prototype implementation-testing-verification is another loop. Answer the following in 4-5 sentences.

- A. Which loop is relatively more expensive, and why?
- B. Can any of these loops be avoided? If not, why not? If yes, what is the penalty?

P3. (10 points) Convert the following numbers to decimal:

- A. 1010110_2
- B. 1011_2
- C. 175_8
- D. 149_{16}
- E. $ACDC_{16}$

P4. (10 points) Convert the following numbers to binary:

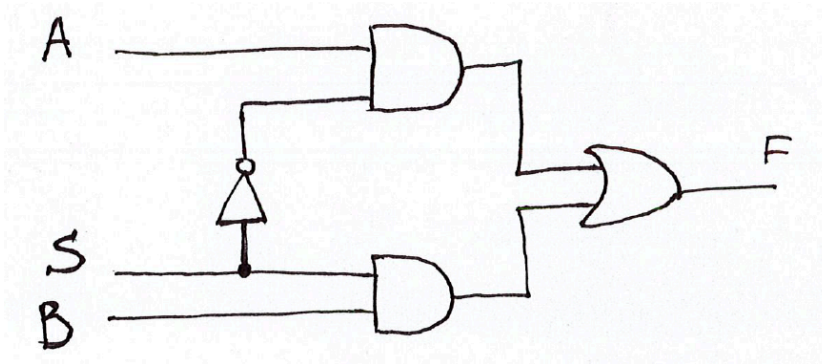
- A. 47
- B. 241
- C. 118
- D. 157_8
- E. $BAAD_{16}$

P5. (10 points) Consider this array of bytes: $[53_{16} 74_{16} 61_{16} 72_{16} 57_{16} 61_{16} 72_{16} 73_{16}]$.

- A. Convert each byte of the array to a binary number (e.g $32_{16} = 00110010_2$).
- B. Convert each binary number to an ASCII character (Refer to section 1.5.3 on pgs 14 - 16). What does it spell?

P6. (10 points) Consider the circuit below. Name the three inputs as A, B, and S and name the output as F.

- Write the logic expression for it.
- Write the truth table for the circuit.



P7. (20 points) Consider the logic function $f(x, y) = (x + \bar{y}) \cdot (\bar{x} + \bar{y})$

- (8 points) Draw the circuit diagram for $f(x, y)$.
- (8 points) Write the truth table for $f(x, y)$.
- (4 points) By looking at the truth table in (b), what observation can you make about $f(x, y)$.

P8. (20 points) Given the following logic expression:

$$F(A, B, C) = (A + B + C) (A + \bar{B} + C) (B + C)$$

- (10 points) Draw the circuit diagram for $F(A, B, C)$.
- (10 points) Draw the truth table for $F(A, B, C)$.