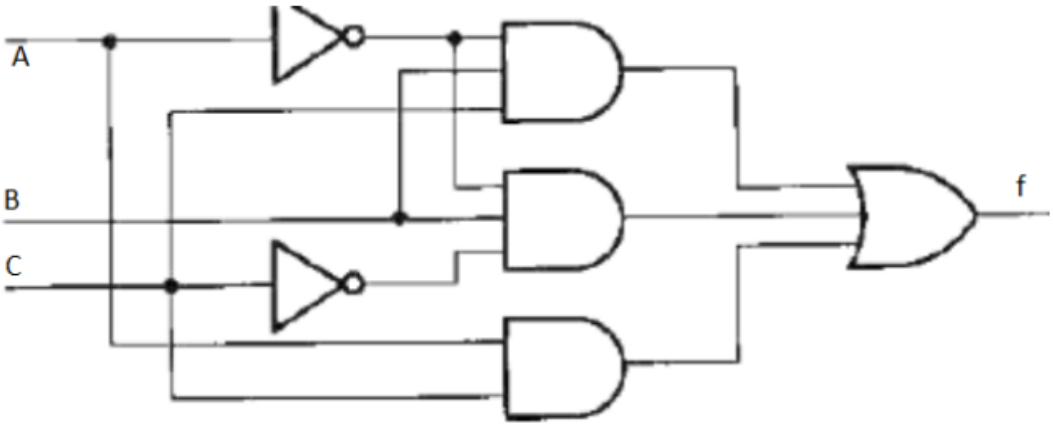
CprE 281 HW03
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Design Examples, Intro to Verilog
Assigned Date: Third Week
Finish by: Sep. 11, 2023

P1. (10 points) Write the following expressions as Verilog behavioral assign statements:
E.g., $F = \bar{A}$ as a Verilog assign statement would be "assign F = ~A":

A. $F = (\bar{A} + B) \cdot (A + \bar{B})$
B. $F = \overline{(A \cdot B \cdot C)} + (\overline{A \cdot B} \cdot \bar{C})$

P2. (10 points) Give the structural Verilog code for the circuit shown below:



P3. (10 points) Examine the following Verilog code and fix any problems. Explain.

```
module P3(F, a, b, c)
     output f;
     input a, b, c;

     always@(*)
          if (c=0)
               f=a;
          else
               f=b

end module
```

P4. (10 points) Multiplexers.

A. Consider a 4-to-1 multiplexer (4-1 MUX) that takes four data inputs w0, w1, w2, w3, two control inputs s0, s1, and has one output f. Derive the Boolean expression for the output f in terms of s0, s1, w0, w1, w2, w3.
B. Now do the same for an 8-to-1 multiplexer. How many data inputs does it have? How many control lines? How many outputs? Derive the Boolean expression for the 8-to-1 multiplexer.

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P5. (15 points) Consider a 3-input XOR gate with inputs A, B, C.

A. Derive the truth table for $A \oplus B \oplus C$ based on the truth table for $A \oplus B$ in the lecture notes.
B. Derive the canonical SOP expression for the function from part A. Do not simplify it. Then, draw the corresponding circuit diagram.
C. Draw a logic circuit that implements the function from part A using only two 2-input XOR gates. Is there another solution that meets these constraints?

P6. (25 points) A seven-segment display is commonly used for displaying decimal digits as we have discussed in the class. Each of the seven segments can be illuminated separately to form different digits. The segments are labeled with a,b,c,d,e,f,g. You are also given a 2-bit binary input s1, s0. The 2-bit input is connected to the seven-segment display which can display the corresponding decimal digit (**from 0 to 3**)

A. **(5 points)** Draw the truth table for all seven segments (from a to g) based on the 2-bit input s1, s0 .
B. **(10 points)** Derive the canonical SOP Boolean expressions for each segment (from a to g) based on the truth table.
C. **(10 points)** Simplify the seven expressions that you got in part B.

P7. (20 points):

A. Given the expression $\mathrm{F(A, B, C)} = \sum m(0,1,2,5)$. Write the expression as a simplified SOP expression.
B. Given the expression $\mathrm{F(A, B, C)} = \sum \mathrm{M}(3,4,6,7)$. Write the expression as a simplified POS expression.
C. Prove that the answer in B is equivalent to the answer in A.
D. You have to implement a Boolean expression using either only NAND gates or only NOR gates. Which of these options would be more efficient for a Product-of-Sums (POS) expression, and which would be more efficient for a Sum-of-Products (SOP) expression? Why?