Cpr E 281 HW08

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Building Blocks

Due Date: Oct. 23, 2023

P1 (10 points): Draw the circuit for the basic SR latch with inputs S, R, and outputs Qa, Qb. Then answer the following:

a) For which values of S and R is Qa the inverse of Qb?

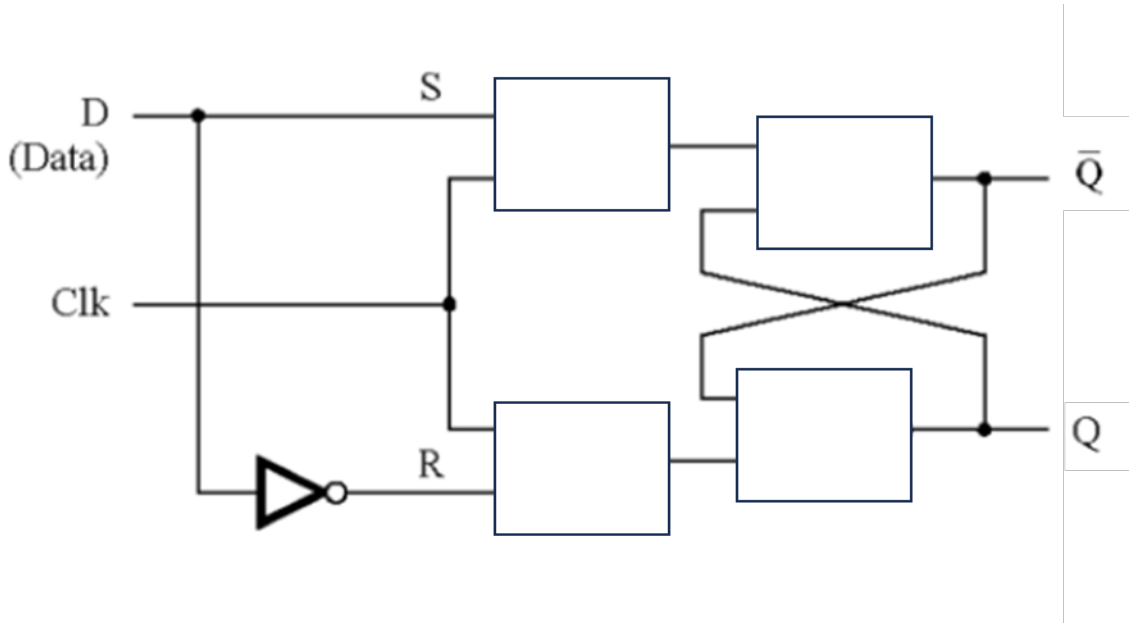
b) If both Qa and Qb outputs are 0s, does this indicate a basic latch with NOR Gates or NAND Gates? Explain.

P2 (10 points): Draw the circuit for a gated SR latch with NAND gates. Then answer these questions:

a) What are the outputs $Q, \bar{Q}$ when the inputs S, R, CLK are all 1s?

b) What are the outputs $Q, \bar{Q}$ when S=1, R=0, CLK=1?

P3 (5 points): Consider the figure below for a Gated D latch. Fill in the rectangular blocks in the figure with the correct logic gates.



P4. (10 points)
The following table can be used to construct a T flip-flop using a D flip-flop.

T	Output		D
	Q(t)	Q(t+1)	
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

a) (5 points) Write the simplified SOP expression for D using T and Q(t) for inputs.

b) (5 points) Draw the circuit for a T flip-flop using a D flip-flop and other necessary gates. Make sure you connect the flip-flop to a clock signal.

P5 (20 points):

Construct a JK flip-flop using a T flip-flop.

a) (10 points) Complete the following table.

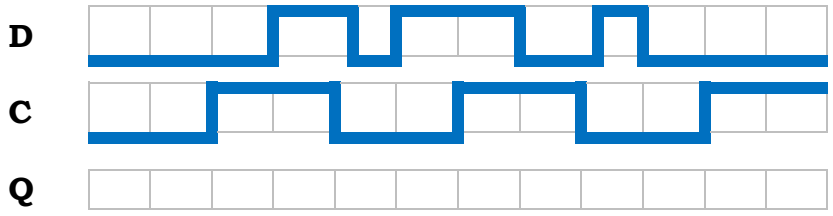
J	K	Output		T
		Q(t)	Q(t+1)	
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

b) (5 points) Write down the simplified SOP expression for T using J, K, and Q(t) for inputs.

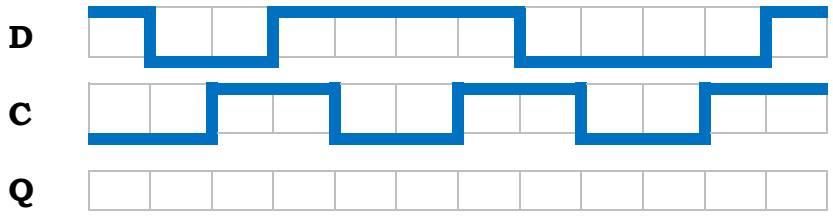
c) (5 points) Draw the circuit for a JK flip-flop using a T flip-flop and other necessary gates. Make sure that you connect the flip-flop to a clock signal.

P6 (20 points): Complete the following timing diagrams for the specified component. The Clk or Clock signal is labeled C. You may assume that Q is initially at 0 unless specified otherwise.

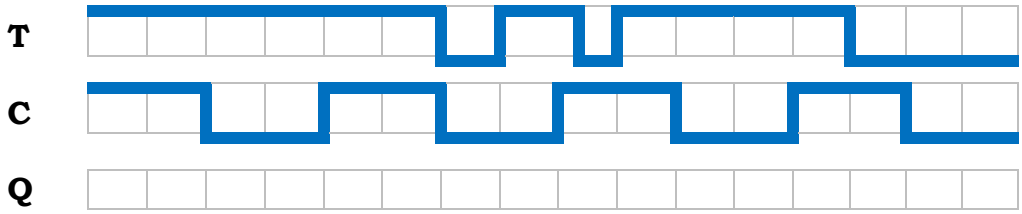
A: Gated D latch.



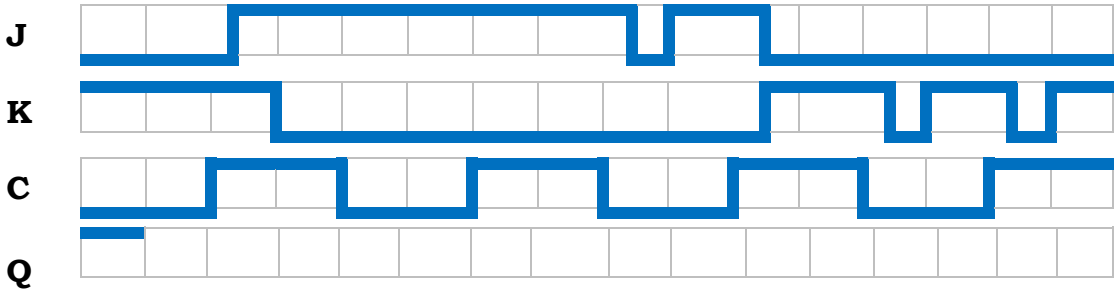
B: A negative-edge-triggered D Flip-Flop (DFF).



C: A positive-edge-triggered T Flip-Flop (TFF).



D: A negative-edge-triggered JK Flip-Flop (JKFF).



P7 (10 points) Draw the complete circuit diagram for a positive-edge triggered master-slave T flip-flop using only NAND gates. Label all inputs and outputs.

P8 (15 points): Answer the following questions about the Negative-Edge Triggered Master-Slave D flip-flop with PRESET_N and CLEAR_N connections, as shown in Figure 5.12 from the book. Suppose that D=1 and CLK=0. Answer the following questions about Q.

a) What effect does pulsing PRESET_N have on this circuit?

b) What effect does pulsing CLEAR_N have on this circuit?

c) What will be the value of Q if PRESET_N=0 and CLEAR_N=1?

d) What will be the value of Q if PRESET_N=0 and CLEAR_N=0?

e) What will be the value of Q if the clock is pulsed while CLEAR_N=1 and PRESET_N=1?