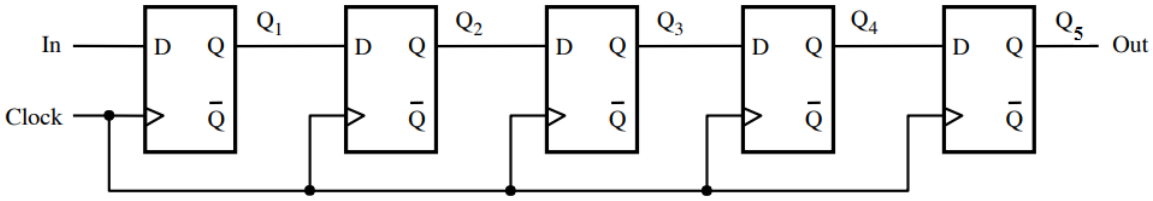
CprE 281 HW10
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Registers & Counters
Finish by Nov. 8, 2023

P1. (**15 points**) Let $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ be two **unsigned** integers.

a) (**10 points**)Design and draw a circuit with 5 outputs (called EQ, NEQ, LT, LE, GE) that checks these $A = B$, $A \neq B$, $A < B$, $A \leq B$, and $A \geq B$. An output is 1 if its corresponding condition is true, Otherwise, it is 0. Clearly label all inputs, outputs, and pins of your circuit.
b) (**5 points**) Explain your solution with a couple of sentences.

P2. (10 points): Complete the following table for the shift register shown below. Assume that each row represents one clock cycle.



Time	In	Q_1	Q_2	Q_3	Q_4	Q_5
t=0	0	0	1	0	0	1
t=1	1					
t=2	0					
t=3	0					
t=4	1					
t=5	0					
t=6	1	0	1	0	0	1

P3. (10 points)
For each subproblem draw a circuit and prove your solution using Boolean algebra.

- **a)** Implement a 3-input NAND gate with only 2-input NAND gates.
- **b)** Implement a 4-input NOR gate with only 2-input NOR gates.

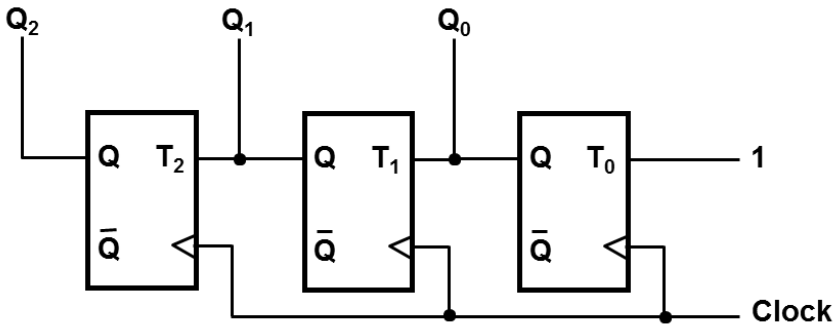
P4. (10 points)
Redraw the circuit from Figure 5.31 in the textbook. Then, explain how this circuit works and draw its characteristic table. Do you agree that it does what the figure caption says?

P5. (**15 points**) Complete the following circuit diagram to implement a 4-bit register that has both parallel load and shift left/right functionality. The register has two control inputs (C_1 and C_0), four parallel input lines (I_3, I_2, I_1, and I_0), and four output lines (Q_3, Q_2, Q_1, and Q_0). Depending on the values of C_1 and C_0, the register performs one of the following four operations:

C_1	C_0	Operation
0	0	**Hold the current value (i.e., Q_3 Q_2 Q_1 Q_0 are not changed)**
0	1	**Shift left (i.e., new Q_3=Q_2, new Q_2=Q_1, new Q_1=Q_0, new Q_0=I_0)**
1	0	**Shift right (i.e., new Q_3=I_3, new Q_2=Q_3, new Q_1=Q_2, new Q_0=Q_1)**
1	1	**Load new data (i.e., new Q_3=I_3, new Q_2=I_2, new Q_1=I_1, new Q_0=I_0)**

Clearly label all inputs, outputs, and pins.

P6. (10 points)
What is the counting sequence of the following counter?
Assuming that the counter starts from $Q_2Q_1Q_0 = 000$.



P7. (20 points)
Draw the following circuits and indicated the counting sequence for each:

a) (5 points) Draw a circuit for a 4-bit asynchronous up-counter using T flip-flops.
b) (5 points) Draw a circuit for a 4-bit synchronous up-counter using T flip-flops.
c) (5 points) Draw a circuit for a 4-bit synchronous up-counter using **D** flip-flops.
d) (5 points) Draw a circuit for a 4-bit Johnson counter using **T** flip-flops.

P8. (10 points)
Figure 5.25 in textbook shows the design of a modulo-6 counter with reset synchronization. Modify the circuit and make it a modulo-5 counter instead? That is, the counting sequence will be: 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 0, 1, and so on. Explain your solution.